

USB-OTG Full-speed Transceiver

Feature summary

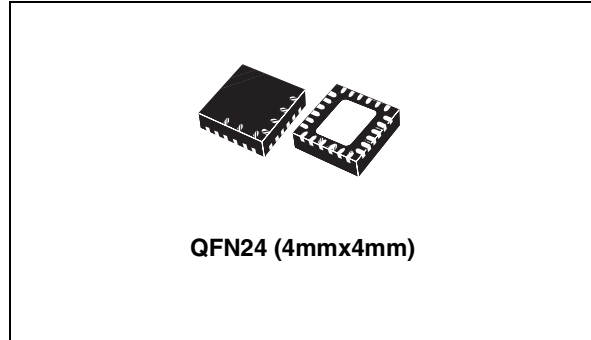
- Meets USB specification Rev. 2.0 And on-the-go supplement to the USB 2.0 specification
- Analog car kit-compatible
- Four operating modes: USB, I²C, UART and Audio
- Configurable using I²C serial interface
- Capable of 12Mbit/s full-speed and 1.5Mbit/s low-speed modes of operation
- Standard digital interface compliant with the OTG transceiver specification
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 35mA typical V_{BUS} charge pump output current for 3.3V supply voltage
- Ability to control external charge pump for higher VBUS currents
- Integrated pull-up/-down resistors
- ±6kV ESD Protection on all USB pins (contact discharge)
- +1.6V to +3.6V Digital power supply and +2.7V to +5.5V analog supply voltage range
- Power-down mode with very low power consumption for battery powered devices

Applications

- Mobile phones
- PDAs
- MP3 players
- Digital cameras
- Printers

Order code

| Part number | Package | Packaging |
|-------------|-------------------|---------------------|
| STOTG04EQTR | QFN24 (4mm x 4mm) | 4000 parts per reel |



Description

The STOTG04 is a USB On-The-Go full-speed transceiver. It provides complete physical layer (PHY) solution for any USB-OTG device. It contains V_{BUS} charge pump and comparators, ID line detector and interrupt generator, and the USB differential driver and receivers. The STOTG04 transceiver is suitable for mobile and battery powered devices because of its low power consumption and power-down operating mode.

The transceiver is capable of operation in several different modes. It can operate in basic USB-OTG mode, as an I²C and UART transceiver, or in audio mode. Behavior of the transceiver is fully configurable through the two-wire I²C serial bus. The transceiver supports session request protocol and host negotiation protocol.

The applications are mobile phones, PDAs, MP3 players, printers and digital cameras.

Contents

| | | |
|----------|------------------------------------|-----------|
| 1 | Pin configuration | 3 |
| 2 | Maximum ratings | 5 |
| 3 | Electrical characteristics | 6 |
| 4 | Charge pump characteristics | 10 |
| 5 | Timing diagrams | 11 |
| 6 | Block description | 14 |
| 6.1 | Charge pump | 14 |
| 6.2 | V _{BUS} Comparators | 14 |
| 6.3 | Voltage regulator | 14 |
| 6.4 | ID Line detector | 14 |
| 6.5 | Driver and receivers | 14 |
| 6.6 | Control logic | 15 |
| 6.7 | Modes of operation | 15 |
| 6.7.1 | Power modes | 15 |
| 6.7.2 | USB Modes | 15 |
| 6.7.3 | UART and I ² C modes | 16 |
| 6.7.4 | Audio mode | 17 |
| 6.8 | Registers | 17 |
| 6.9 | I ² C Bus interface | 19 |
| 6.10 | Device address | 19 |
| 6.11 | Bus protocol | 19 |
| 6.12 | External charge pump switch | 21 |
| 7 | Package mechanical data | 22 |
| 8 | Revision history | 25 |

1 Pin configuration

Figure 1. Pin connections (Bottom View)

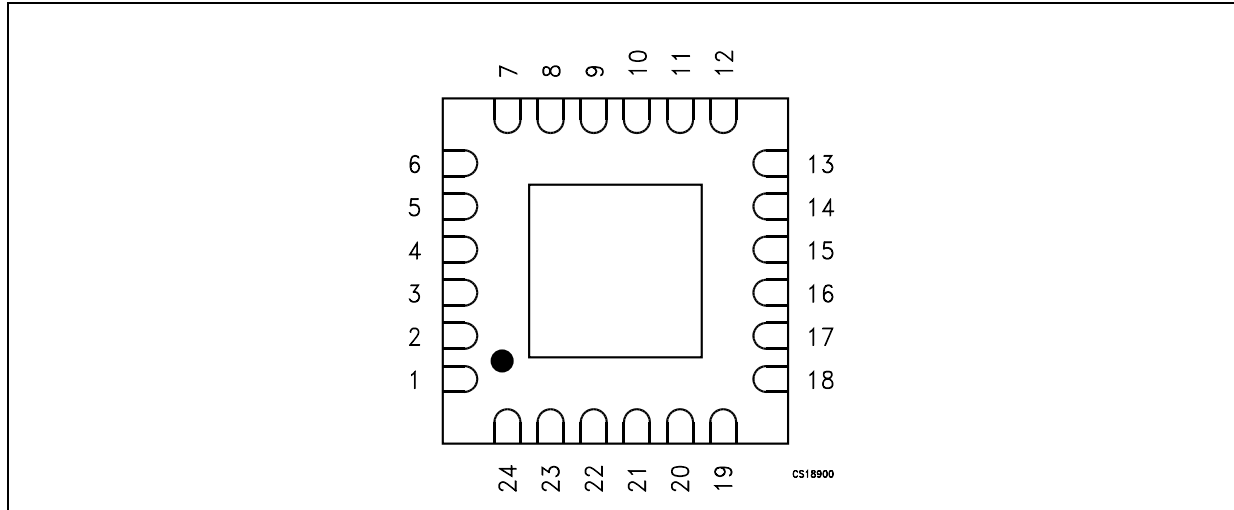


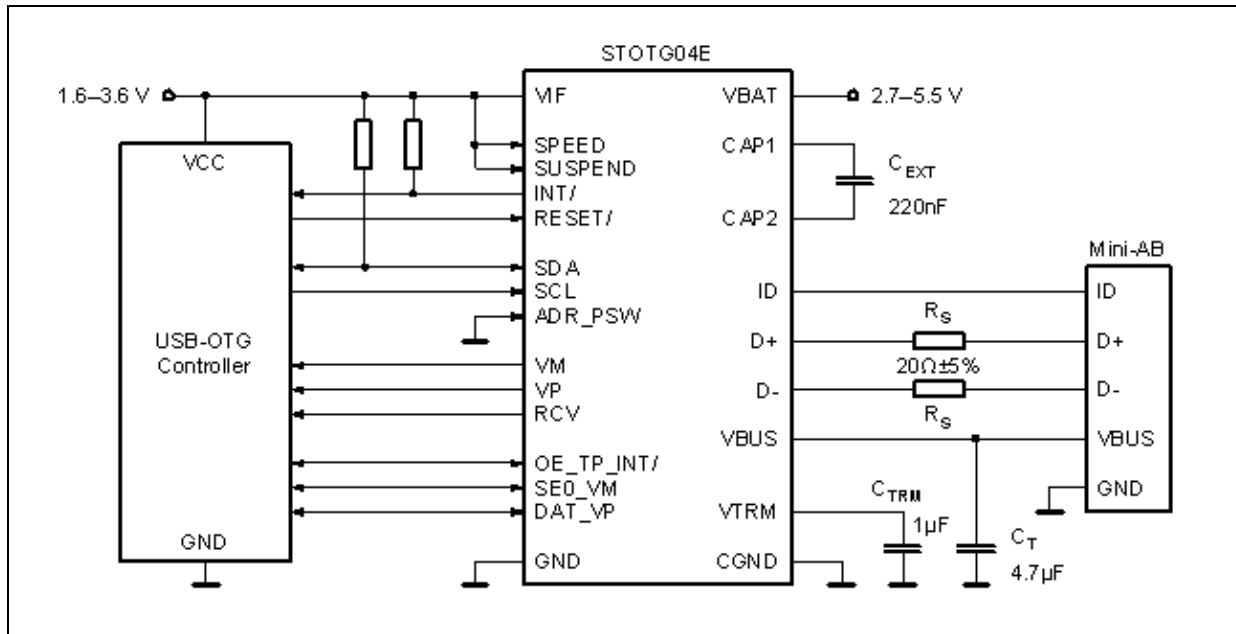
Table 1. Pin description

| PIN N° | SYMBOL | I/O | NAME AND FUNCTION |
|--------|------------------|-------|---|
| 1 | ADR_PSW | I/O | Least significant bit of the I ² C address of the transceiver input latched on reset; PSW output enabling or disabling an external charge pump |
| 2 | SDA | I/O | I ² C serial data (1) |
| 3 | SCL | I | I ² C clock |
| 4 | RESET/ | I | Active low logic reset |
| 5 | INT/ | O | Active low interrupt signal (open-drain) |
| 6 | SPEED | I | Mode of the transceiver (0 = low-speed, 1 = full-speed) (2) |
| 7 | V _{TRM} | Power | Internal voltage regulator output; an external decoupling capacitor should be connected (3) |
| 8 | SUSPEND | I | Power down input (0 = active mode, 1 = power down) (See Table 8) |
| 9 | OE_TP_INT/ | I/O | Output enable of the differential driver in the USB mode, I ² C data enable in the I ² C mode or interrupt output |
| 10 | VM | O | D- single-ended receiver output |
| 11 | VP | O | D+ single-ended receiver output |
| 12 | RCV | O | Differential receiver output |
| | ExpPad | - | Not Connected |
| 13 | SE0_VM | I/O | Single-ended zero input/output in the DAT_SE0 transmit mode, negative data input/output in the single-ended transmit mode or TXD in the UART mode |
| 14 | DAT_VP | I/O | Data input/output in the DAT_SE0 transmit mode, positive data input/output in the single-ended transmit mode or RXD in the UART mode |
| 15 | D- | I/O | Negative data line in the USB mode, I ² C clock output in the I ² C mode or serial data output in the UART mode |
| 16 | D+ | I/O | Positive data line in the USB mode, I ² C serial data in the I ² C mode or serial data input in the UART mode |
| 17 | GND | Power | Common analog and digital ground |
| 18 | ID | I/O | ID pin of the USB connector used for protocol identification |
| 19 | V _{BUS} | I/O | V _{BUS} line of the USB interface – it needs an external capacitor of 4.7μF |

| PIN N° | SYMBOL | I/O | NAME AND FUNCTION |
|--------|------------------|-------|--|
| 20 | V _{BAT} | Power | Analog power supply voltage (+2.7V to +5.5V) |
| 21 | CAP1 | I/O | External capacitor pin for the charge pump |
| 22 | CAP2 | I/O | External capacitor pin for the charge pump |
| 23 | CGND | Power | Ground for the charge pump |
| 24 | V _{IF} | Power | Logic power supply (+1.6V to 3.6V) |

- (1) Input and open-drain output
- (2) Input with internal pull-up resistor
- (3) Internal regulator can be bypassed by connecting V_{BAT} to this pin when the V_{BAT} is in range of 2.7V to 3.6V

Figure 2. Functional diagram



2 Maximum ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------------|---|-----------------------|------|
| V _{IF} | Logic Supply Voltage | -0.5 to + 4.5 | V |
| V _{BAT} | Analog Supply Voltage | -0.5 to + 6.5 | V |
| V _{DCCDIG} | DC Input Voltage on any logic interface pin | -0.5 to + 4.5 | V |
| T _{STG} | Storage Temperature Range | -65 to + 150 | °C |
| V _{ESD} | Electrostatic discharge voltage on USB pins | Human Body Model | ± 8 |
| | | Contact Discharge (*) | ± 6 |

(*) In accordance to IEC61000-4-2, level 3.

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional Operation under these conditions is not implied.

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|-------------------|-------------------------------------|-------|------|
| R _{thJA} | Thermal Resistance Junction-Ambient | 59 | °C/W |

Table 4. Recommended operating condition

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|--|------|------|------|------|
| V _{IF} | Logic Supply Voltage | 1.6 | 1.8 | 3.6 | V |
| V _{BAT} | Analog Supply Voltage | 2.7 | 3.3 | 5.5 | V |
| T _A | Operating Temperature Range | -40 | | +85 | °C |
| C _{EXT} | Charge pump external capacitor | 100 | 220 | 470 | nF |
| C _T | Charge pump tank capacitor | 1 | 4.7 | 6.5 | µF |
| C _{TRM} | Voltage regulator external capacitor | | 1 | | µF |
| R _S | Data lines impedance matching resistor | | 20 | | Ω |

Table 5. ESD Performance

| Symbol | Parameter | Value | Unit |
|--------|----------------------------------|-------------------------------|------|
| ESD | IEC-61000-4-2 (D+, D-, VBUS, ID) | Air discharge (10 pulses) | ± 8 |
| | | Contact discharge (10 pulses) | ± 6 |
| | IEC-61000-4-2 (other pins) | Air discharge (10 pulses) | ± 2 |
| | | Contact discharge (10 pulses) | ± 2 |

3 Electrical characteristics

Table 6. Electrical characteristics

Characteristics measured over recommended operating conditions unless otherwise is noted. All typical values are referred to $T_A = 25^\circ\text{C}$, $V_{IF} = 1.8\text{V}$, $V_{BAT} = 3.3\text{V}$, $R_S = 20\Omega$, $C_{EXT} = 220\text{nF}$, $C_T = 4.7\mu\text{F}$ and $C_{TRM} = 1\mu\text{F}$

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------------------------|---|---|---------------|------|-------------|---------------|
| I_{IF} | Digital Part Supply Current | Active mode (1,2) | | 0.6 | 1.6 | mA |
| | | Power down mode | | | 1 | μA |
| I_{BAT} | Operating Supply Current | Transceiver current while transmitting and receiving (1, 2) | | 4.5 | 7 | mA |
| | | Charge pump current, $I_{LOAD} = 8\text{mA}$ | | 17 | 25 | |
| | | Power down mode (4) | | | 1 | μA |
| LOGIC INPUTS AND OUTPUTS | | | | | | |
| V_{OH} | HIGH level output voltage | $I_{OH} = -100\mu\text{A}$ | $V_{IF}-0.15$ | | | V |
| | | $I_{OH} = -2\text{mA}$ | $V_{IF}-0.40$ | | | V |
| V_{OL} | LOW level output voltage | $I_{OL} = 100\mu\text{A}$ | | | 0.15 | V |
| | | $I_{OL} = 2\text{mA}$ | | | 0.40 | V |
| V_{IH} | HIGH level input voltage | | $0.7V_{IF}$ | | | V |
| V_{IL} | LOW level input voltage | | | | $0.3V_{IF}$ | V |
| I_{LKG} | Input leakage current | | -1 | | 1 | μA |
| I_{OZ} | Off-state output current | | -5 | | 5 | μA |
| V_{BUS} | | | | | | |
| V_{BUS} | V_{BUS} output voltage | $I_{LOAD} = 8\text{mA}$ | 4.4 | 4.9 | 5.25 | V |
| V_{BUS_LKG} | V_{BUS} leakage voltage | No Load | | 3 | 200 | mV |
| V_{BUS_RIP} | V_{BUS} output ripple | $I_{LOAD} = 8\text{mA}$, $C_T = 4.7\mu\text{F}$ | | 30 | 60 | mV |
| f_{CP} | Charge-pump switching frequency (2) | | 0.5 | 0.8 | 1.5 | MHz |
| R_{VBUS} | V_{BUS} input impedance | | 40 | 76 | 100 | k Ω |
| I_{VBUS} | Maximum V_{BUS} source current | $C_{EXT} = 220\text{ nF}$, $V_{BUS} > 4.4\text{V}$ | 20 | 35 | | mA |
| V_{BUS_VLD} | V_{BUS} valid comparator threshold | Low to high transition | 4.40 | | | V |
| | | High to low transition | 4.40 | | | |
| V_{SES_VLD} | Session valid comparator threshold for both A and B devices | Low to high transition | 0.8 | | 2.0 | V |
| | | High to low transition | 0.8 | | 2.0 | |
| R_{VBUS_PU} | V_{BUS} charge pull-up resistance | | 281 | 640 | | Ω |
| R_{VBUS_PD} | V_{BUS} discharge pull-down resistance | | 656 | 1260 | | Ω |
| ID | | | | | | |
| V_{ID_BIAS} | ID pin bias voltage | $R_{CP_ID} = 140\text{k}\Omega$, $V_{BAT} \leq 5\text{V}$ | 1.3 | 1.9 | 3.0 | V |
| R_{ID_PU} | ID pin pull-up resistance | | 70 | 105 | 130 | k Ω |
| R_{ID_GND} | ID line short resistance to detect id_gnd state | | | | 10 | Ω |
| R_{ID_FLOAT} | ID line short resistance to detect id_float state | | 800 | | | k Ω |

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|-------|------|------|------------|
| DIFFERENTIAL DRIVER | | | | | | |
| Z_{DRV} | Output Impedance | Excluding external R_S | 8 | 16 | 24 | Ω |
| V_{OH_DRV} | HIGH level output voltage | $R_{LH} = 14.25k\Omega$, $V_{TRM} = 3.3V$ | 2.8 | | 3.6 | V |
| | | $R_{LH} = 14.25k\Omega$, $V_{TRM} = 2.7V$ | 2.6 | | 3.0 | V |
| V_{OL_DRV} | LOW level output voltage | $R_{LL} = 1.425k\Omega$ | 0 | | 0.3 | V |
| V_{CRS} | Driver crossover voltage | $C_{LOAD} = 50$ to $600pF$ | 1.3 | 1.67 | 2.0 | V |
| DIFFERENTIAL AND SINGLE-ENDED RECEIVERS | | | | | | |
| V_{DI} | Differential receiver input sensitivity ($V_{D+} - V_{D-}$) | $V_{CM} = 0.8$ to $2.5V$ | -200 | | 200 | mV |
| V_{SE-TH} | SE receivers switching threshold | Low to high transition | 0.8 | 1.6 | 2.0 | V |
| | | High to low transition | 0.8 | 1.1 | 2.0 | |
| R_{IN} | Input resistance | PU/PD resistor deactivated | 1.5 | | | M Ω |
| C_{IN} | Input capacitance | | | 10 | 30 | pF |
| R_{PU_D+} | Data line pull-up resistance on pin D+ | Bus Idle | 900 | 1300 | 1575 | Ω |
| | | Receiving mode | 1425 | 2200 | 3090 | |
| R_{PU_D-} | Data line pull-up resistance on pin D- | | 900 | 1300 | 1575 | Ω |
| R_{PD} | Data line pull-down resistance | | 14.25 | 17.0 | 24.8 | k Ω |
| V_{DT_LKG} | Data line leakage voltage | $R_{PU_EXT} = 300k\Omega$ | | 200 | 342 | mV |
| CAR KIT INTERRUPT DETECTOR | | | | | | |
| $V_{CR_INT_TH}$ | Car kit Interrupt threshold | | 0.4 | | 0.6 | V |
| I²C AND UART MODES – D+ AND D- PINS | | | | | | |
| V_{OH} | HIGH level output voltage (3) | $I_{OH} = -2mA$ | 2.4 | | 3.6 | V |
| V_{OL} | LOW level output voltage | $I_{OL} = 2mA$ | 0 | | 0.4 | V |
| V_{IH} | HIGH level input voltage | | 2.0 | | | V |
| V_{IL} | LOW level input voltage | | | | 0.8 | V |
| R_{DP_I2C} | SDA line internal pull-up resist. | | 1425 | 2200 | 3090 | Ω |
| VOLTAGE REGULATOR | | | | | | |
| V_{TRM} | Internal power supply voltage | $V_{BAT} = 3.3$ to $5V$, no load; $2V7en=0$ | 3.0 | 3.3 | 3.6 | V |
| | | $V_{BAT} = 2.8$ to $5V$, no load; $2V7en=1$ | 2.6 | 2.75 | 2.9 | V |
| I_{TRM} | Voltage regulator output current | $V_{BAT} = 3.6V$, $V_{TRM} > 3V$; $2V7en=0$ | | | 20 | mA |
| | | $V_{BAT} = 3.0V$, $V_{TRM} > 2.6V$; $2V7en=1$ | | | 10 | mA |

(1) Transmitting and receiving at 12Mbit/s, loads of 50pF on D+ and D- pins, no capacitive loads on VP and VM pins

(2) Not tested in production; characterization only

(3) Except D+ pin in the I2C mode where this pin is open-drain with internal pull-up resistor

(4) See paragraph 6.7.1

Table 7. Switching characteristics

Over recommended operating conditions unless otherwise is noted. All the typical values are referred to $T_A = 25^\circ\text{C}$, $V_{IF} = 1.8\text{V}$, $V_{BAT} = 3.3\text{V}$, $R_S = 20\Omega$, $C_{EXT} = 220\text{nF}$, $C_T = 4.7\mu\text{F}$, and $C_{TRM} = 1\mu\text{F}$

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|--|---|------|------|--------|---------------|
| T_{VBUS_RISE} | V_{BUS} rise time | $I_{LOAD} = 8\text{mA}$, $C_T = 10\mu\text{F}$ | | 1 | 100 | ms |
| DIFFERENTIAL DRIVER | | | | | | |
| t_R | Data signal rise time | Full-speed mode, $C_{LOAD} = 50\text{pF}$ | 4 | 8.5 | 20 | ns |
| | | Low-speed mode, $C_{LOAD} = 600\text{pF}$ | 75 | 110 | 300 | |
| t_F | Data signal rise time | Full-speed mode, $C_{LOAD} = 50\text{pF}$ | 4 | 8.5 | 20 | ns |
| | | Low-speed mode, $C_{LOAD} = 600\text{pF}$ | 75 | 110 | 300 | |
| $t_{P_DRV_R}$ | Propagation delay of the driver, rising edge; DAT_SE0 mode | Full-speed mode, $C_{LOAD} = 50\text{pF}$ | | | 38 | ns |
| | | Low-speed mode, $C_{LOAD} = 600\text{pF}$ | | | 280 | |
| $t_{P_DRV_R}$ | Propagation delay of the driver, rising edge; VP_VM mode | Full-speed mode, $C_{LOAD} = 50\text{pF}$ | | | 55 | ns |
| | | Low-speed mode, $C_{LOAD} = 600\text{pF}$ | | | 300 | |
| $t_{P_DRV_F}$ | Propagation delay of the driver, falling edge; DAT_SE0 mode | Full-speed mode, $C_{LOAD} = 50\text{pF}$ | | | 38 | ns |
| | | Low-speed mode, $C_{LOAD} = 600\text{pF}$ | | | 280 | |
| $t_{P_DRV_F}$ | Propagation delay of the driver, rising edge; VP_VM mode | Full-speed mode, $C_{LOAD} = 50\text{pF}$ | | | 55 | ns |
| | | Low-speed mode, $C_{LOAD} = 600\text{pF}$ | | | 300 | |
| t_{RFM} | Rise and fall time matching (t_R/t_F) excluding the first transition from the idle state | Full-speed mode | 90 | | 111.11 | % |
| | | Low-speed mode | 80 | | 125 | |
| SINGLE-ENDED RECEIVERS | | | | | | |
| $t_{P_SE_R}$ | Propagation delay of the SE receiver, rising edge | Full-speed mode, input slope 15ns | | | 18 | ns |
| | | Low-speed mode, input slope 150ns | | | 18 | |
| $t_{P_SE_F}$ | Propagation delay of the SE receiver, falling edge | Full-speed mode, input slope 15ns | | | 18 | ns |
| | | Low-speed mode, input slope 150ns | | | 18 | |
| DIFFERENTIAL RECEIVER | | | | | | |
| $t_{P_DIF_R}$ | Propagation delay of the SE receiver, rising edge | Full-speed mode, input slope 15ns | | | 24 | ns |
| | | Low-speed mode, input slope 150ns | | | 24 | |
| $t_{P_DIF_F}$ | Propagation delay of the SE receiver, falling edge | Full-speed mode, input slope 15ns | | | 24 | ns |
| | | Low-speed mode, input slope 150ns | | | 24 | |
| DIGITAL INTERFACE | | | | | | |
| t_{SET_OE} | Output enable setup time | | 50 | | | ns |
| t_{TA_OI} | Output to input bus turnaround time (1, 2) | | 0 | | 5 | ns |
| t_{TA_IO} | Output to input bus turnaround time (1, 2) | | 0 | | 5 | ns |
| I²C BUS (3) | | | | | | |
| f_{SCL} | SCL clock frequency | | | | 100 | kHz |
| t_{LOW} | Low period of the SCL clock | | 4.7 | | | μs |
| t_{HIGH} | High period of the SCL clock | | 4.0 | | | μs |
| t_{ICR} | Rise time of both SDA and SCL signals | | | | 1000 | ns |

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------|---|-----------------|------|------|------|---------------|
| t_{ICF} | Fall time of both SDA and SCL signals | | | | 300 | ns |
| $t_{\text{SU_STA}}$ | Setup time for a repeated START condition | | 4.7 | | | μs |
| $t_{\text{HD_STA}}$ | Hold time for the START and repeated START conditions | | 4.0 | | | μs |
| $t_{\text{SU_DAT}}$ | Data setup time | | 250 | | | ns |
| $t_{\text{HD_DAT}}$ | Data hold time | | 0 | | | μs |
| $t_{\text{SU_STO}}$ | Setup time for the STOP condition | | 4.0 | | | μs |
| t_{BUF} | Bus free time between a STOP and START condition | | 4.7 | | | μs |

NOTE 1: Parameter applies to the OE_TP_INT/, DAT_VP, and SE0_VM signals

NOTE 2: Not tested in production; characterization only

NOTE 3: Requirements defined by the I2C-Bus Specification, version 2.1

4 Charge pump characteristics

Figure 3. Output characteristics

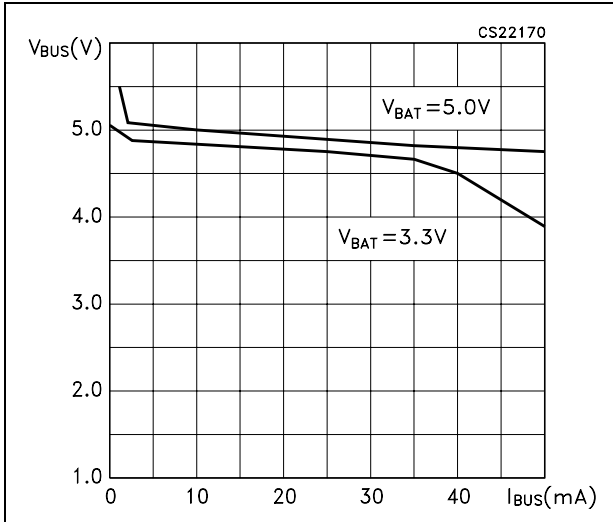
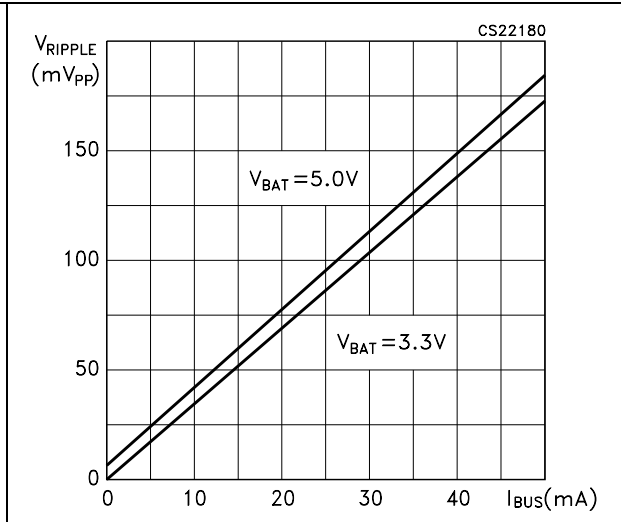


Figure 4. Output ripple



5 Timing diagrams

Figure 5. Rise and fall times

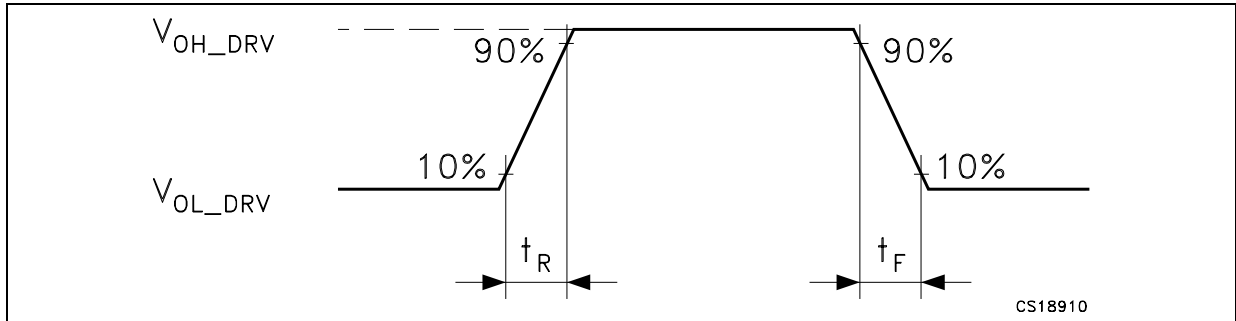


Figure 6. Differential driver propagation delay

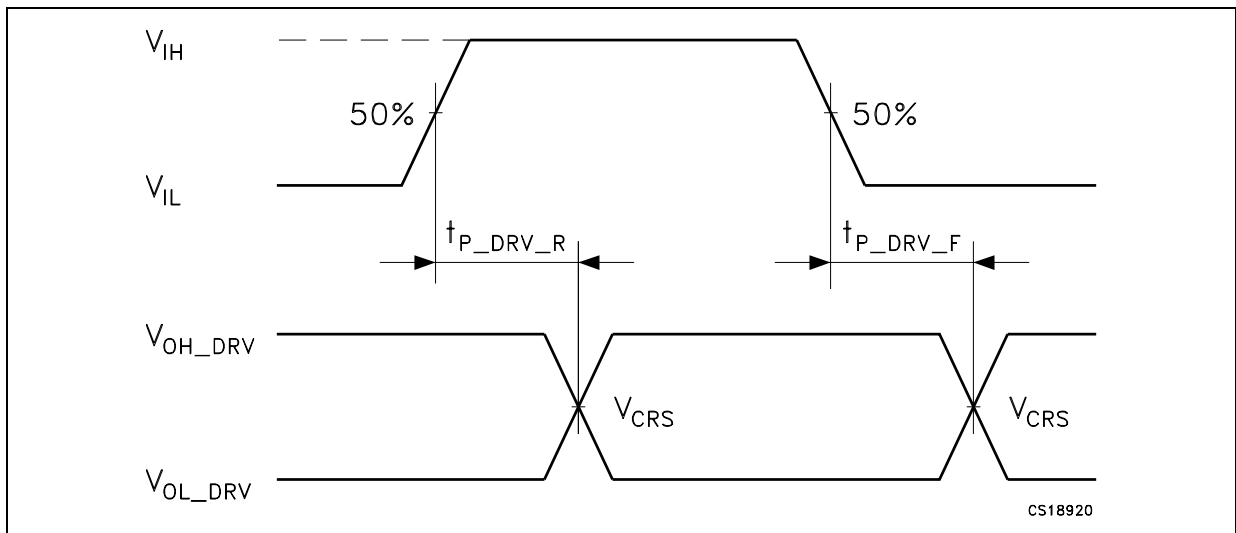


Figure 7. Differential receiver propagation delay

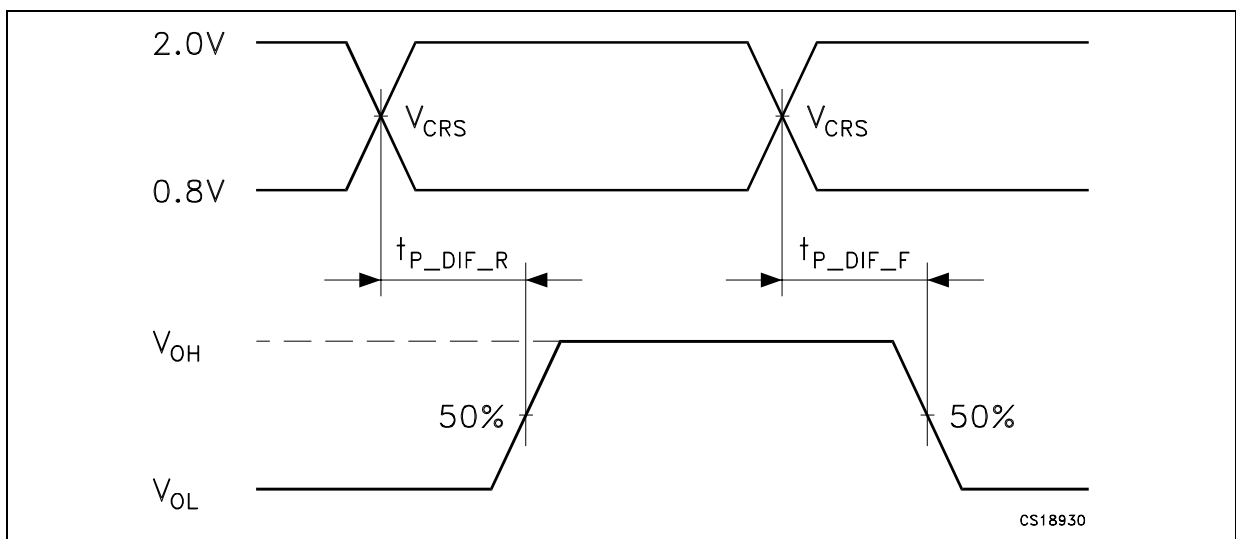


Figure 8. Output enable setup time

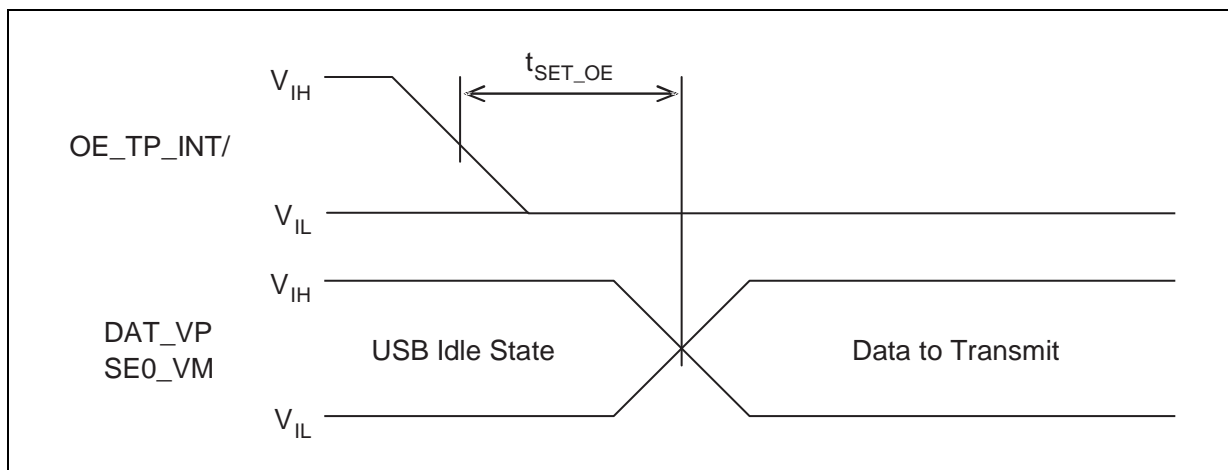


Figure 9. Bus turnaround time

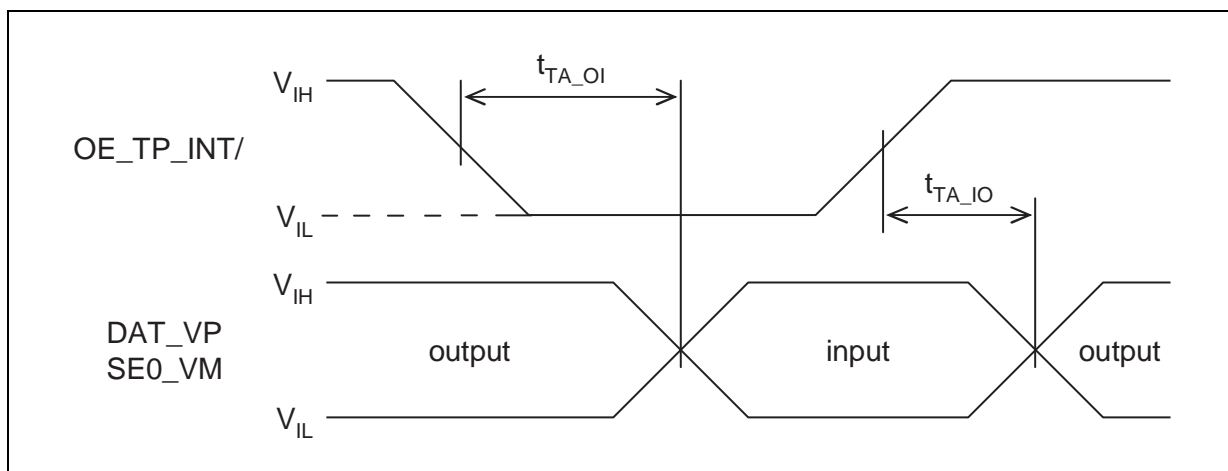


Figure 10. I²C BUS timing

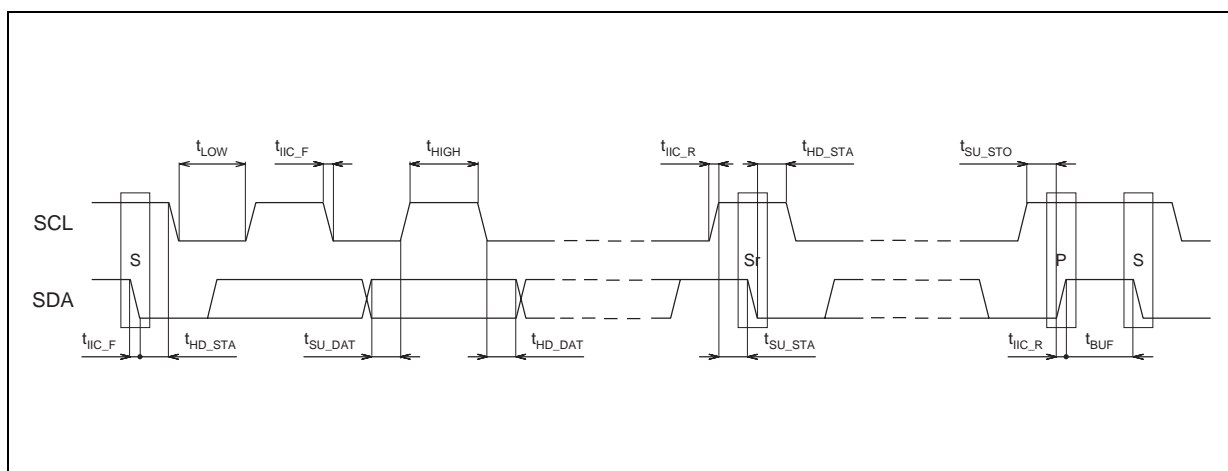
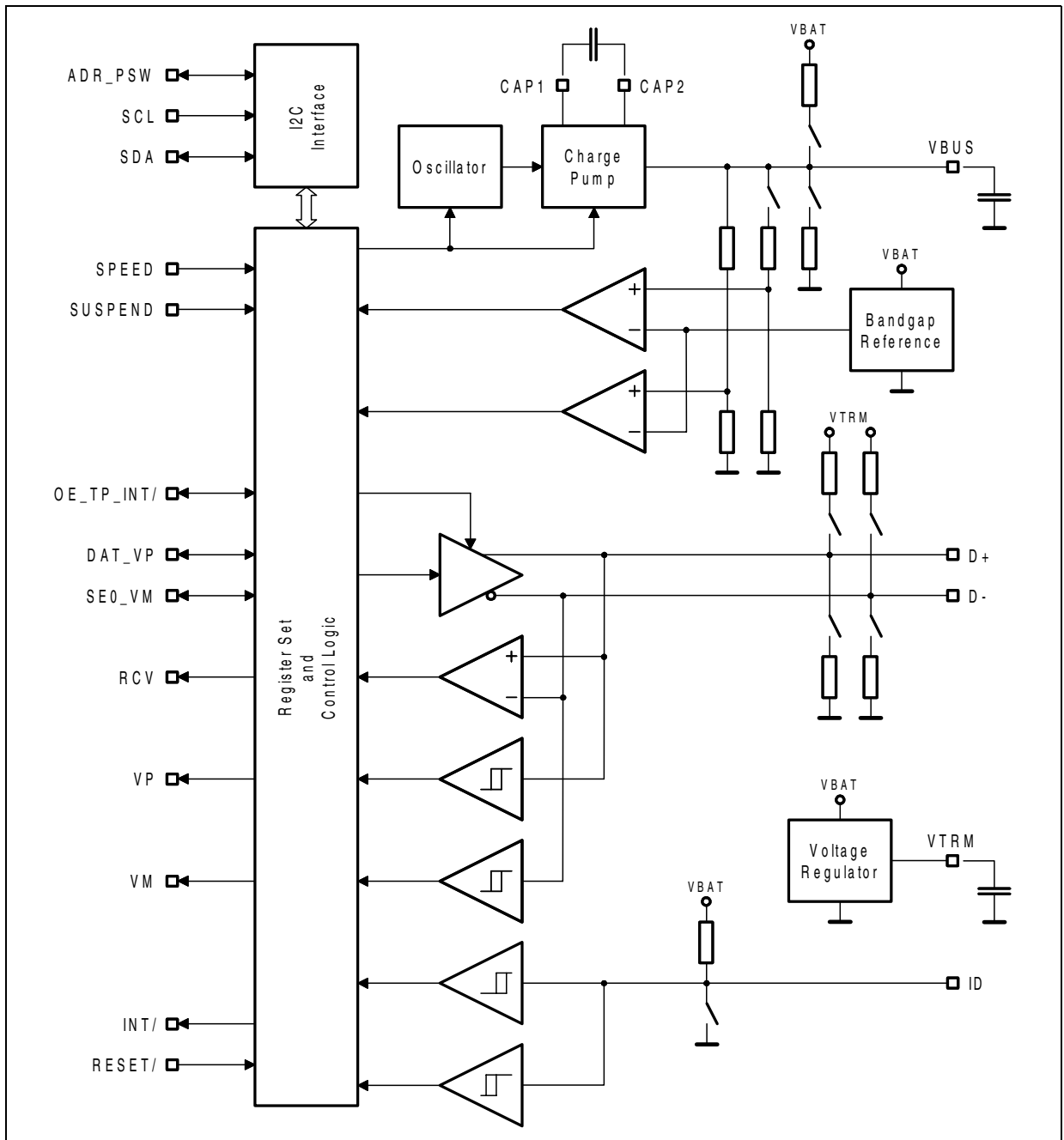


Figure 11. Block diagram



6 Block description

The STOTG04 integrates a charge pump and comparators for the V_{BUS} , ID line detector and interrupt switch, differential data driver, differential and single-ended receivers, low dropout voltage regulator and control logic. The STOTG04 provides a complete solution for connection of a digital USB OTG controller to the physical Universal Serial Bus.

6.1 Charge pump

The V_{BUS} line voltage is provided using the internal charge pump. It is capable of sourcing up to 35mA load current. The charge pump can be powered by voltage from 2.7V to 5.5V. It needs two capacitors for its operation: an external capacitor of 220nF connected between the CAP1 and CAP2 pins and a 4.7 μ F decoupling tank capacitor on the V_{BUS} . If an application needs current that is higher than 35mA, an external charge pump or a switch controlled by the ADR_PSW pin may be used.

6.2 V_{BUS} Comparators

These comparators monitor the V_{BUS} voltage. They provide current status information for the V_{BUS} line. V_{BUS} valid status means that the voltage is above V_{BUS_VLD} . Session valid status means that the V_{BUS} voltage is above V_{SES_VLD} level.

6.3 Voltage regulator

An internal low-dropout voltage regulator provides power for the bus drivers and receivers. The regulator needs an external capacitor of 1 μ F on the V_{TRM} pin for proper operation. The regulator can provide 3.3V or 2.75V output voltages according to 2V7_en bit in Control Register 3.

The regulator can be bypassed by tying the V_{TRM} pin to the V_{BAT} power supply voltage when the analog supply voltage is in the range of 3.0V (or 2.7V) to 3.6V.

6.4 ID Line detector

This block senses ID line status. It is capable of detecting three different line states:

- pin floating;
- pin tied to ground;
- pin grounded via a 140k Ω resistor.

The ID detector can also generate an interrupt by shorting the pin to ground.

6.5 Driver and receivers

The driver can operate in several different modes. It can act as a simple low-speed and full-speed differential USB driver, as two independent single-ended drivers in the UART mode, or as an open-drain driver in the I²C mode.

This block contains one differential receiver for the USB operation mode and two single-ended receivers for USB signaling as well as UART and I²C receivers.

6.6 Control logic

This block controls the behavior of whole chip. It communicates with the external environment via the I²C serial bus. The control logic block consists of I²C slave interface, configuration and status registers, and some glue logic.

6.7 Modes of operation

The STOTG04 can operate in two different power modes and in three operating modes. They can be controlled by logic signals and control registers.

6.7.1 Power modes

When there is no need for the USB function, the STOTG04 reduces power consumption by implementing the Power-down mode. The power modes can be controlled by the Suspend Bit of Control Register 1 or/ and the SUSPEND pin (see Table 8).

Table 8. Power modes

| SUSPEND BIT | SUSPEND PIN | Power Mode |
|-------------|-------------|------------------|
| 0 | X | normal operation |
| X | 0 | |
| 1 | 1 | power-down |

Although in power down mode all analog blocks should be switched off, some of them could be turned on by bits in the control registers having higher priority than suspend bit. In order to obtain minimum power consumption in power down mode the device must be configured as shown in Table 9. The digital part is fully static so that it almost does not consume power. All of the interrupts (except BDIS_ACON) are fully operational in Power-down mode, as is the I²C interface.

Table 9. Power down mode setup

| SUSPEND BIT | SUSPEND PIN | Control register 1 | Control register 2 | Control register 3 |
|-------------|-------------|--------------------|--------------------|--------------------|
| 1 | 1 | X1X0XX0- | 00XX00X0 | -XXXX0XX |

X = Don't care

- = Reserved

Bit order: 0...7

6.7.2 USB Modes

The STOTG04 transceiver has two basic USB operational modes. These modes define how the digital IO pins of the transceiver will be used. Independently of USB operating mode, some signals always have the same function (see Table 10).

Table 10. Digital interface signals

| Signal | Function |
|------------|---|
| RCV | Differential receiver output |
| VP | D+ single-ended receiver output |
| VM | D- single-ended receiver output |
| OE_TP_INT/ | Output enable signal of the differential driver |

The RCV signal is active in the VP_VM mode only. Its output driver is controlled by the OE_TP_INT/ signal. Operating modes are described below. The meanings of the DAT_VP and SE0_VM signals depend on the mode of operation. Both of these signals can be bidirectional or unidirectional. The



direction is controlled by `bidi_en` Bit of Control Register 3 (described later). When these signals are bidirectional, the direction is controlled by the `OE_TP_INT/` signal (see Tables 11 and 12).

The actual mode of operation is controlled by the `dat_se0` Bit of Control Register 1 (see Tables 11 and 12)

Table 11. DAT_SE0 (dat_se0 = 1)

| <code>bidi_en</code> | <code>OE/*</code> | <code>DAT_VP</code> | <code>SE0_VM</code> |
|----------------------|-------------------|------------------------------|---------------------|
| 1 | 0 | Differential driver input | SE0 driver input |
| | 1 | Differential receiver output | SE0 detector output |
| 0 | X | Differential driver input | SE0 driver input |

Table 12. VP_VM (dat_se0 = 0)

| <code>bidi_en</code> | <code>OE/*</code> | <code>DAT_VP</code> | <code>SE0_VM</code> |
|----------------------|-------------------|---------------------|---------------------|
| 1 | 0 | D+ driver input | D- driver input |
| | 1 | D+ receiver output | D- receiver output |
| 0 | X | D+ driver input | D- driver input |

* State of the `OE_TP_INT/` signal.

In the USB mode of operation it is necessary to control the rise and fall times of the transmission driver. These times are different for low-speed and full-speed USB settings. Selection of actual USB speed can be done using the bit speed of Control Register 1 or/and the SPEED pin (see table 13).

Table 13. USB Speed selection

| speed bit | SPEED Pin | USB Mode |
|-----------|-----------|------------|
| 0 | X | low-speed |
| X | 0 | |
| 1 | 1 | full-speed |

6.7.3 UART and I²C modes

The actual mode of operation is selectable by the `transp_en` and `uart_en` Bits of Control Register 1 (see table 14).

Table 14. Transceiver modes

| <code>transp_en</code> | <code>uart_en</code> | STOTG04 Mode |
|------------------------|----------------------|------------------|
| 0 | 0 | USB |
| 0 | 1 | UART |
| 1 | 0 | I ² C |
| 1 | 1 | UART (1) |

(1) In reality, it is not possible to set both these bits at the same time. In this case, only `uart_en` bit will remain set.

In the I²C mode the D+ and D- lines act respectively as I²C SDA and SCL signals when the `OE_TP_INT/` signal is low. The transceiver automatically enables the pull-up resistor on the SDA line in this mode. The internal I²C slave interface of the transceiver does not react to commands from the master. Communication addressed to the STOTG04 device is mirrored to the D+ pin and responses from this pin are mirrored back to the SDA pin. The D- pin mirrors the SCL clock.

In the UART mode it is possible to select driver direction on both the D+ and D- pins. The selection is done using the `bdir[1]` and `bdir[0]` Bits of Control Register 3 (see table 15).

Table 15. UART Drivers direction

| bdir[1] | bdir[0] | DAT_VP ↔ D+ | SE0_VM ↔ D- |
|----------------|----------------|--------------------|--------------------|
| 0 | 0 | → | → |
| 0 | 1 | → | ← |
| 1 | 0 | ← | → |
| 1 | 1 | ← | ← |

6.7.4 Audio mode

In this mode the transceiver has to release all of its drivers and pull-up/pull-down resistors on the D+, D- and ID pins, leaving them in a high impedance state. This allows these lines to be used for transmission of audio signals. The transceiver should not provide voltage on its V_{BUS} output in this mode. Conditions described in Table 16 force the transceiver into the audio mode.

Table 16. Audio mode setup

| transp_en bit | uart_en bit | OE_TP_INT/ signal | Control Register 2 |
|----------------------|--------------------|--------------------------|---------------------------|
| 0 | 0 | 1 | 00000000 |

6.8 Registers

The STOTG04 transceiver device is controlled using register settings (see Table 17). These registers can be set and read via the I²C bus.

Table 17. Register set

| Register | Size (bits) | Acc⁽¹⁾ | Addr⁽²⁾ | Description |
|----------------------|--------------------|--------------------------|---------------------------|--|
| Vendor ID | 16 | r | 00h | STMicroelectronics ID (0483h) - LSB first |
| Product ID | 16 | r | 02h | ID of the STOTG04 (A0C4h) - LSB first |
| Control 1 | 8 | r/s/c | 04h 05h | First Control Register |
| Control 2 | 8 | r/s/c | 06h 07h | Second Control Register |
| Control 3 | 8 | r/s/c | 12h 13h | Third Control Register |
| Interrupt Source | 8 | r | 08h | Current state of signals generating interrupts |
| Interrupt Latch | 8 | r/s/c | 0Ah 0Bh | Latched source that generated interrupt |
| Interrupt Mask False | 8 | r/s/c | 0Ch 0Dh | Enables interrupts on falling edge |
| Interrupt Mask True | 8 | r/s/c | 0Eh 0Fh | Enables interrupts on rising edge |

(1) Access type can be: read (r), set (s), clear (c).

(2) The first address is to set, the second one to clear bits.

When writing to the set address, any “1” will set the associated Bit to logic “1”. When writing to the clear address, any “1” will set the associated Bit to logic “0”. It is possible to read from any address, whether it is a set or clear address. See Tables 18, 19, 20, 21 for bit setting details.

Table 18. Control register 1

| Name | Bit | R ⁽¹⁾ | Description |
|--------------|-----|------------------|--|
| Speed | 0 | 1 | 0 = low-speed mode 1 = full-speed mode |
| Suspend | 1 | 1 | 0 = normal operation 1 = power-down mode |
| dat_se0 | 2 | 0 | 0 = VP_VM mode 1 = DAT_SE0 mode |
| transp_en | 3 | 0 | Enable transparent I ² C mode |
| bdis_acon_en | 4 | 0 | Enable A-device to connect if B-device disconnect detected |
| oe_int_en | 5 | 0 | When set and suspend = 1, then OE_TP_INT/ becomes interrupt output |
| uart_en | 6 | 0 | Enable UART mode (higher priority than transp_en bit) |
| | 7 | | Reserved |

(1) State of the bit after reset.

Setting the bdis_acon_en bit enables automatic switching of the D+ pull-up resistor when the device receives an SE0 longer than half of the bit period. This function should not be used in low-speed operation.

Table 19. Control register 2

| Name | Bit | R | Description |
|--------------|-----|---|---|
| dp_pull-up | 0 | 0 | Connect D+ pull-up |
| dm_pull-up | 1 | 0 | Connect D- pull-up |
| dp_pull-down | 2 | 1 | Connect D+ pull-down |
| dm_pull-down | 3 | 1 | Connect D- pull-down |
| id_gnd_drv | 4 | 0 | Connect ID pin to ground |
| vbus_drv | 5 | 0 | Provide power to V _{BUS} |
| vbus_dischrg | 6 | 0 | Discharge V _{BUS} through a resistor to ground |
| vbus_chrg | 7 | 0 | Charge V _{BUS} through a resistor |

It is not possible to set vbus_drv, vbus_dischrg and vbus_chrg at the same time; the bit having higher priority will remain set while the others will be cleared. Vbus_drv has higher priority than vbus_dischrg which has higher priority than vbus_chrg.

Table 20. Control register 3

| Name | Bit | R | Description |
|-------------|-----|---|---|
| | 0 | 0 | Reserved |
| rec_bias_en | 1 | 0 | Enables transmitter bias even during USB receive |
| bidi_en | 2 | 1 | When set, then DAT_VP and SE0_VM pins become bidirectional otherwise they are inputs only |
| bdir[0] | 3 | 0 | Direction of the drivers between DAT_VP↔DP and |
| bdir[1] | 4 | 1 | SE0_VM↔DM in the UART mode |
| audio_en | 5 | 0 | Enables car-kit interrupt detector |
| psw_en | 6 | 0 | Enables external charge pump control on the ADR_PSW pin. Disables internal charge pump. |
| 2V7_en | 7 | 0 | Enables 2.7V voltage regulation instead of 3.3V |

Table 21. Interrupt registers (*)

| Name | Bit | R | Description |
|-----------|-----|---|---|
| vbus_vld | 0 | 0 | A-device V _{BUS} valid comparator |
| sess_vld | 1 | 0 | Session valid comparator |
| dp_hi | 2 | 0 | D+ pin is asserted high during SRP |
| id_gnd | 3 | 0 | ID pin grounded |
| dm_hi | 4 | 0 | D- pin is asserted high |
| id_float | 5 | 0 | ID pin floating |
| bdis_acon | 6 | 0 | Set when bdis_acon_en bit is set and transceiver asserts dp_pull-up after detecting B-device disconnect |
| cr_int | 7 | 0 | Car-kit interrupt |

(*) Bit order is the same for all four interrupt related registers. Meaning of each register is described in Table 17.

6.9 I²C Bus interface

All of the STOTG04 transceiver registers are accessible through the I²C bus (see Figure 12). The device contains a slave controller which provides communication with an external master. The I²C interface consists of three pins:

- SDA (Serial Data);
- SCL (Serial Clock);
- ADR_PSW (is the LSB of the device address).

6.10 Device address

The USB-OTG transceiver has following 7-bit I²C device address:

| | | | | | | |
|---|---|---|---|---|---|-----|
| 0 | 1 | 0 | 1 | 1 | 0 | adr |
|---|---|---|---|---|---|-----|

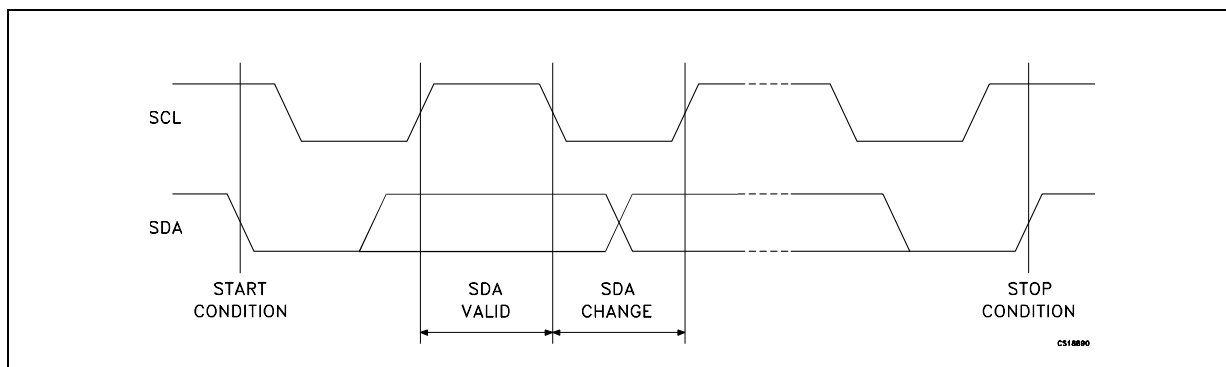
The adr bit represents current state of the ADR_PSW device pin. It means that the address can be either 2Ch or 2Dh according to the ADR_PSW pin.

6.11 Bus protocol

Any device that sends data to the bus is defined as the transmitter. Any device that reads the data is the receiver. The device that controls data transfers is the bus master, while the transmitter or receiver is the slave device. The master initiates data transfers and provides the serial clock. The STOTG04 is always the slave device.

Operation of the I²C bus is described by following figure 12.

Figure 12. Basic operation of the I²C Bus



Start condition is identified by a falling edge of the SDA signal while the SCL is stable at high level. The start condition must precede any data transfer on the bus.

Stop condition is identified by a rising edge of the SDA signal while the SCL is stable at high level. The stop condition terminates any communication between device and master.

The **acknowledge bit** is used to indicate a successful byte transfer. The bus transmitter releases the SDA line after sending eight data bits. During the ninth clock period the receiver pulls the SDA line low to acknowledge the receipt of the eight data bits. If the receiver is a slave device and it does not generate acknowledge bit then the bus master can generate the stop condition in order to abort the transfer.

Below is described format of I²C commands. All tables use common format and symbols. Every data word consists of eight bits with most significant bit first and least significant bit last.

Symbols used in the tables are:

- S – start condition
- P – stop condition
- A – acknowledge bit
- N – negative acknowledge

WRITE Command to the transceiver device is described by following table. It is possible to write into several consecutive registers during one write command.

| | | | | | | | |
|----------|----------------|------------|---|----------------|------------|---|---|
| S | Device address | 0 | A | Reg. address K | A | | |
| Data (K) | A | Data (K+1) | A | .. | Data (K+N) | A | P |

READ command consists of dummy write to set proper address of a register followed by real read sequence.

| | | | | | | | |
|------------|----------------|------------|---|----------------|------------|---|---|
| S | Device address | 0 | A | Reg. address K | A | P | |
| S | Device address | 1 | A | Data (K) | A | | |
| Data (K+1) | A | Data (K+2) | A | ... | Data (K+N) | N | P |

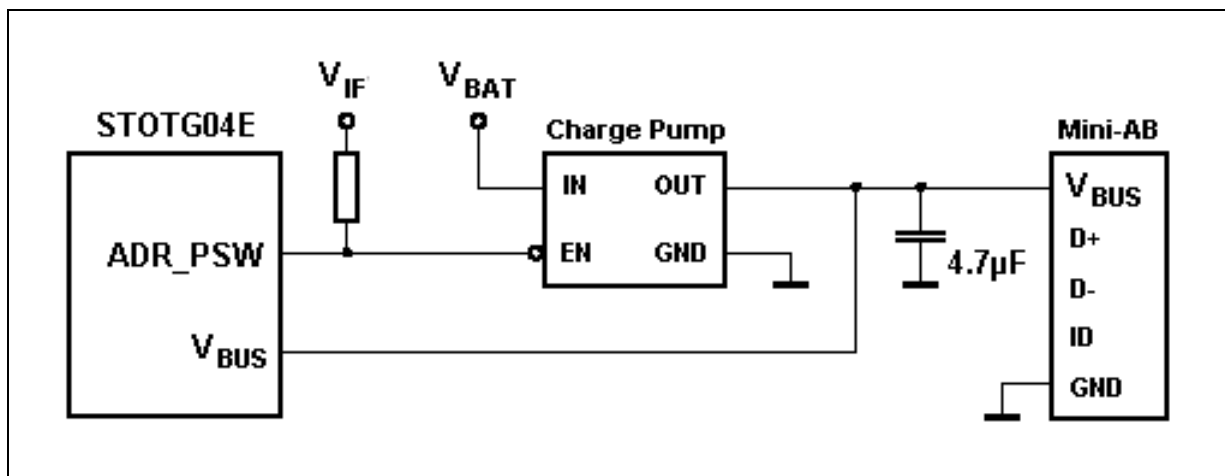
6.12 External charge pump switch

The ADR_PSW pin has two functions. State of this pin is always latched into a register on the rising edge of the RESET/ signal. The latched value is used as a least significant bit of the I²C address. After the address is latched, this pin can be set as an output by setting the PSW_EN bit of the Control Register 3. Output value of the pin can be controlled by the VBUS_DRV bit of the Control Register 2. The output is active low when the pin is high during reset; otherwise the output is active high.

When the PSW_EN bit is set the internal charge pump is switched off.

Example connection of an external charge pump is shown in following figure. When the charge pump control signal would be active high, the ADR_PSW pin should be pulled down instead of high.

Figure 13. External charge pump application

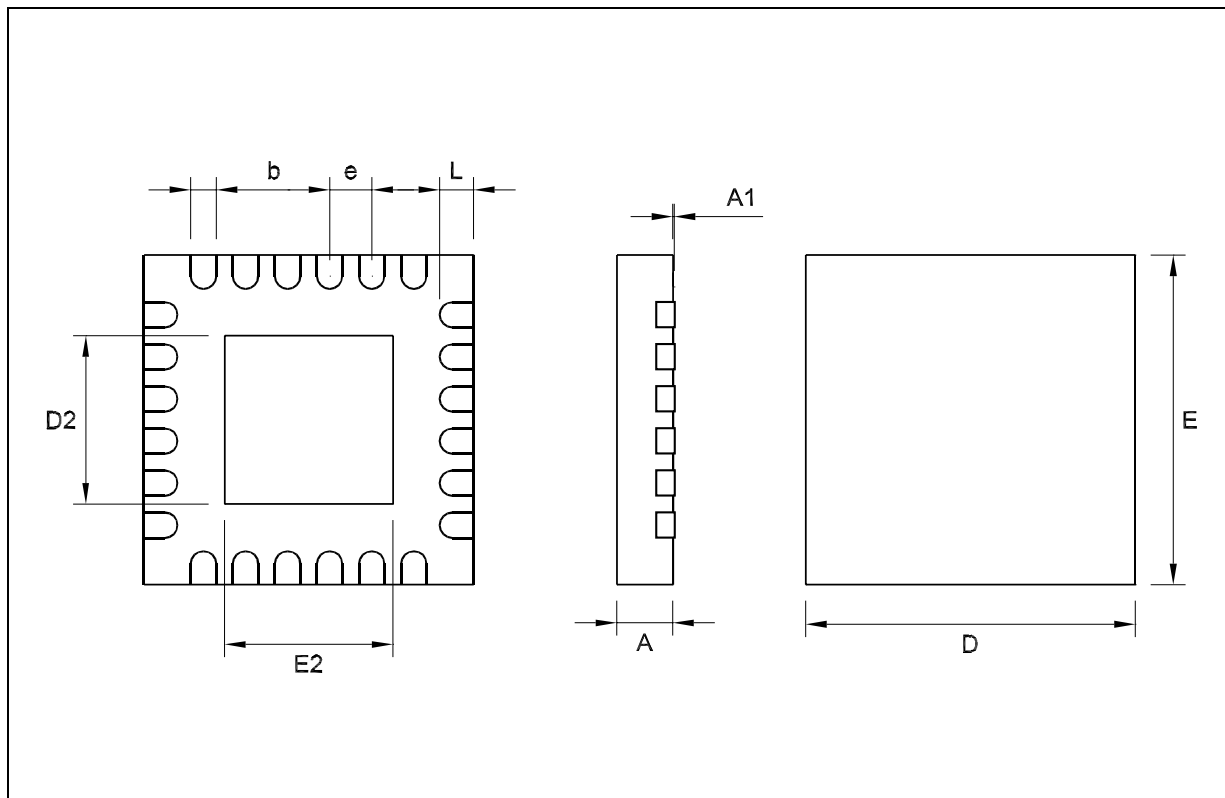


7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

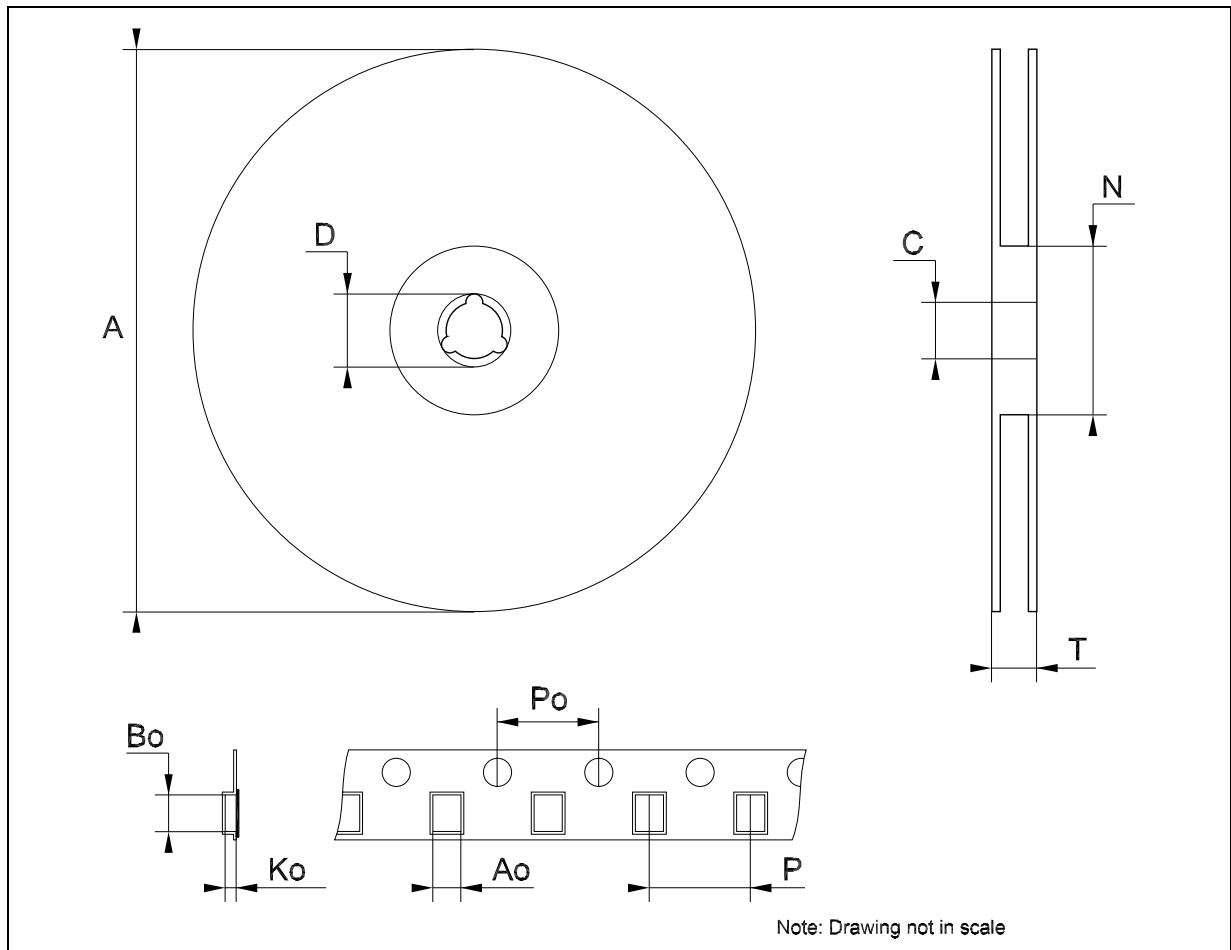
QFN24 (4x4) MECHANICAL DATA

| DIM. | mm. | | | mils | | |
|------|------|------|------|-------|------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.00 | | | 39.4 |
| A1 | 0.00 | | 0.05 | 0.0 | | 2.0 |
| b | 0.18 | | 0.30 | 7.1 | | 11.8 |
| D | 3.9 | | 4.1 | 153.5 | | 161.4 |
| D2 | 1.95 | | 2.25 | 76.8 | | 88.6 |
| E | 3.9 | | 4.1 | 153.5 | | 161.4 |
| E2 | 1.95 | | 2.25 | 76.8 | | 88.6 |
| e | | 0.50 | | | 19.7 | |
| L | 0.40 | | 0.60 | 15.7 | | 23.6 |



Tape & Reel QFNxx/DFNxx (4x4) MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|------|------|-------|-------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 99 | | 101 | 3.898 | | 3.976 |
| T | | | 14.4 | | | 0.567 |
| Ao | | 4.35 | | | 0.171 | |
| Bo | | 4.35 | | | 0.171 | |
| Ko | | 1.1 | | | 0.043 | |
| Po | | 4 | | | 0.157 | |
| P | | 8 | | | 0.315 | |



8 Revision history

Table 22. Revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 13-Jan-2006 | 1 | First Release. |
| 01-Feb-2006 | 2 | Mistake on Table 1. |
| 17-Oct-2006 | 3 | Added details in paragraph 6.7.1, comments to table 19 and description in paragraph 6.12. |

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