

# SN54LS540, SN54LS541, SN74LS540, SN74LS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SDLS180 – AUGUST 1979 – REVISED MARCH 1988

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins
- Data Flow-thru Pinout (All Inputs on Opposite Side from Outputs)

## description

These octal buffers and line drivers are designed to have the performance of the popular SN54LS240/SN74LS240 series and, at the same time, offer a pinout having the inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

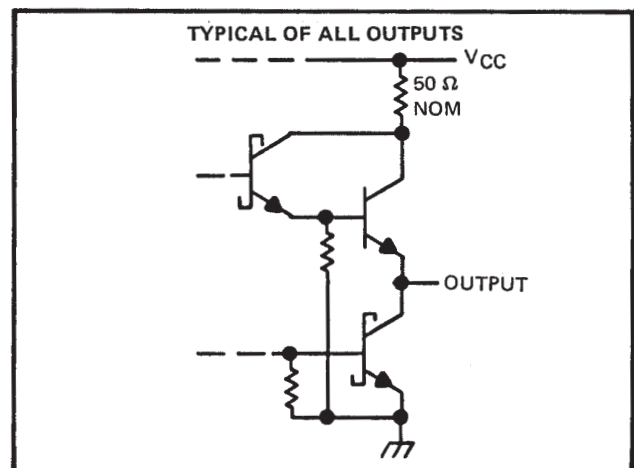
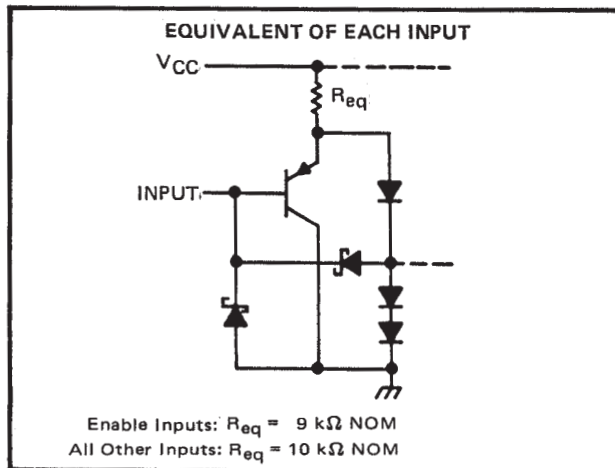
The three-state control gate is a 2-input NOR such that if either  $\overline{G1}$  or  $\overline{G2}$  are high, all eight outputs are in the high-impedance state.

The 'LS540 offers inverting data and the 'LS541 offers true data at the outputs.

The SN54LS540 and SN54LS541 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS540 and SN74LS541 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

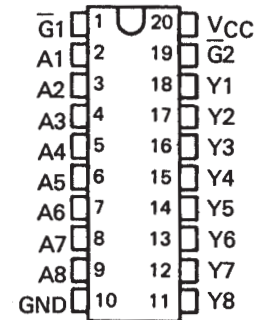
TYPE	RATED $I_{OL}$ (SINK CURRENT)	RATED $I_{OH}$ (SOURCE CURRENT)	TYPICAL POWER DISSIPATION (ENABLED)	
			'LS540	'LS541
SN54LS'	12 mA	-12 mA	92.5 mW	120 mW
SN74LS'	24 mA	-15 mA	92.5 mW	120 mW

## schematics of inputs and outputs



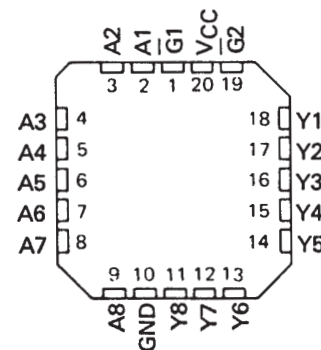
SN54LS540, SN54LS541 . . . J OR W PACKAGE  
SN74LS540, SN74LS541 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS540, SN54LS541 . . . FK PACKAGE

(TOP VIEW)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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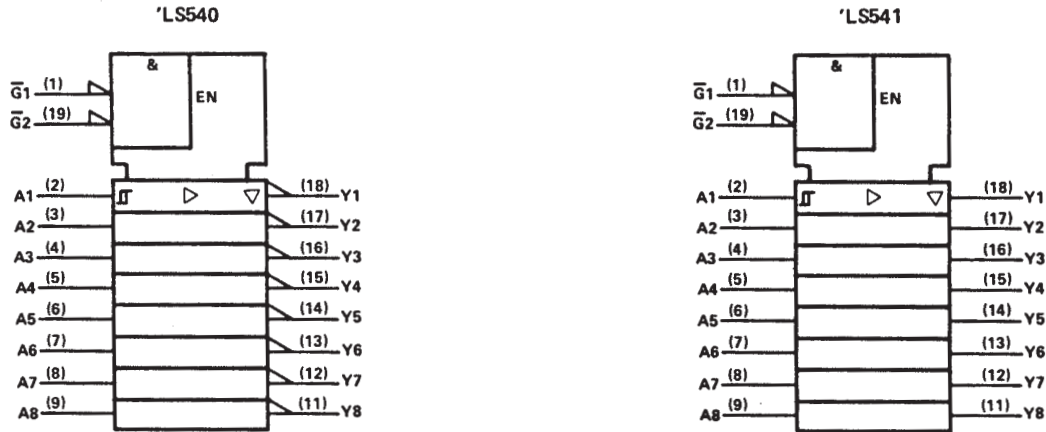
# SN54LS540, SN54LS541, SN74LS540, SN74LS541

## OCTAL BUFFERS AND LINE DRIVERS

### WITH 3-STATE OUTPUTS

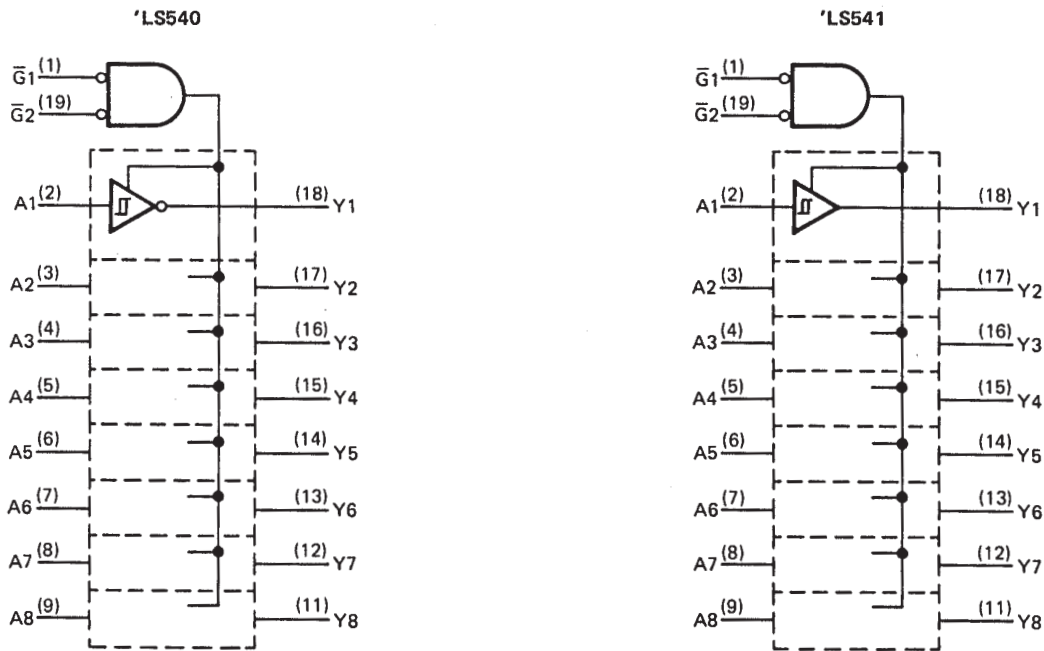
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#### logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage .....	7 V
Operating free-air temperature range: SN54LS540, SN54LS541 .....	$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$
SN74LS540, SN74LS541 .....	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature range .....	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

NOTE 1: Voltage values are with respect to the network ground terminal.



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# SN54LS540, SN54LS541, SN74LS540, SN74LS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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## recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$ (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-12			-15	mA
Low-level output current, $I_{OL}$			12			24	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
$V_{IH}$ High-level input voltage		2			2			V	
$V_{IL}$ Low-level input voltage		0.6			0.6			V	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V	
Hysteresis ( $V_{T+} - V_{T-}$ )	$V_{CC} = \text{MIN}$	0.2	0.4		0.2	0.4	V		
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4	V		
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.5 \text{ V}, I_{OH} = \text{MAX}$	2			2				
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V	
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 24 \text{ mA}$					0.35	0.5		
$I_{OZH}$ Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 2.7 \text{ V}$			20			20	$\mu\text{A}$	
$I_{OZL}$ Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_{IL} = V_{IL \text{ max}}, V_O = 0.4 \text{ V}$			-20			-20		
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA	
$I_{IH}$ High-level input current, any input	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	$\mu\text{A}$	
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.2			-0.2	mA	
$I_{OS}$ Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$			-40			-225	mA	
$I_{CC}$ Supply current	Outputs high	$V_{CC} = \text{MAX},$ Outputs open	'LS540	13	25		13	25	mA
			'LS541	18	32		18	32	
	Outputs low		'LS540	24	45		24	45	
			'LS541	30	52		30	52	
	All outputs disabled		'LS540	30	52		30	52	
			'LS541	32	55		32	55	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.



**SN54LS540, SN54LS541, SN74LS540, SN74LS541**  
**OCTAL BUFFERS AND LINE DRIVERS**  
**WITH 3-STATE OUTPUTS**

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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	'LS540			'LS541			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$ Propagation delay time, low-to-high-level output	$C_L = 45\text{ pF}$ , $R_L = 667\ \Omega$ , See Note 2		9	15		9	15	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output			9	15		10	18	ns
$t_{PZL}$ Output enable time to low level			25	38		25	38	ns
$t_{PZH}$ Output enable time to high level			15	25		20	32	ns
$t_{PLZ}$ Output disable time from low level	$C_L = 5\text{ pF}$ , $R_L = 667\ \Omega$ , See Note 2		10	18		10	18	ns
$t_{PHZ}$ Output disable time from high level			15	25		18	29	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
84155012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
8415501RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
8415501RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
8415501SA	OBSOLETE			20		TBD	Call TI	Call TI
8415501SA	OBSOLETE			20		TBD	Call TI	Call TI
84156012A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
84156012A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
8415601SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
8415601SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32404B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32404B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32404BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32404BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32405B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32405B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32405BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32405BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32405BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/32405BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SN54LS540J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54LS540J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54LS541J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54LS541J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN74LS540DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LS540DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS540N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS540N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS540N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS540NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS540NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS540NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS540NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS541DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS541DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS541DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS541DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS541DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS541DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS541N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS541N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS541N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS541N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS541NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS541NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS541NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS541NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS541NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS541NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54LS540FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SNJ54LS540FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS540J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS540J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS540W	OBSOLETE			20		TBD	Call TI	Call TI
SNJ54LS540W	OBSOLETE			20		TBD	Call TI	Call TI
SNJ54LS541FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS541FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS541J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS541J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS541W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS541W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



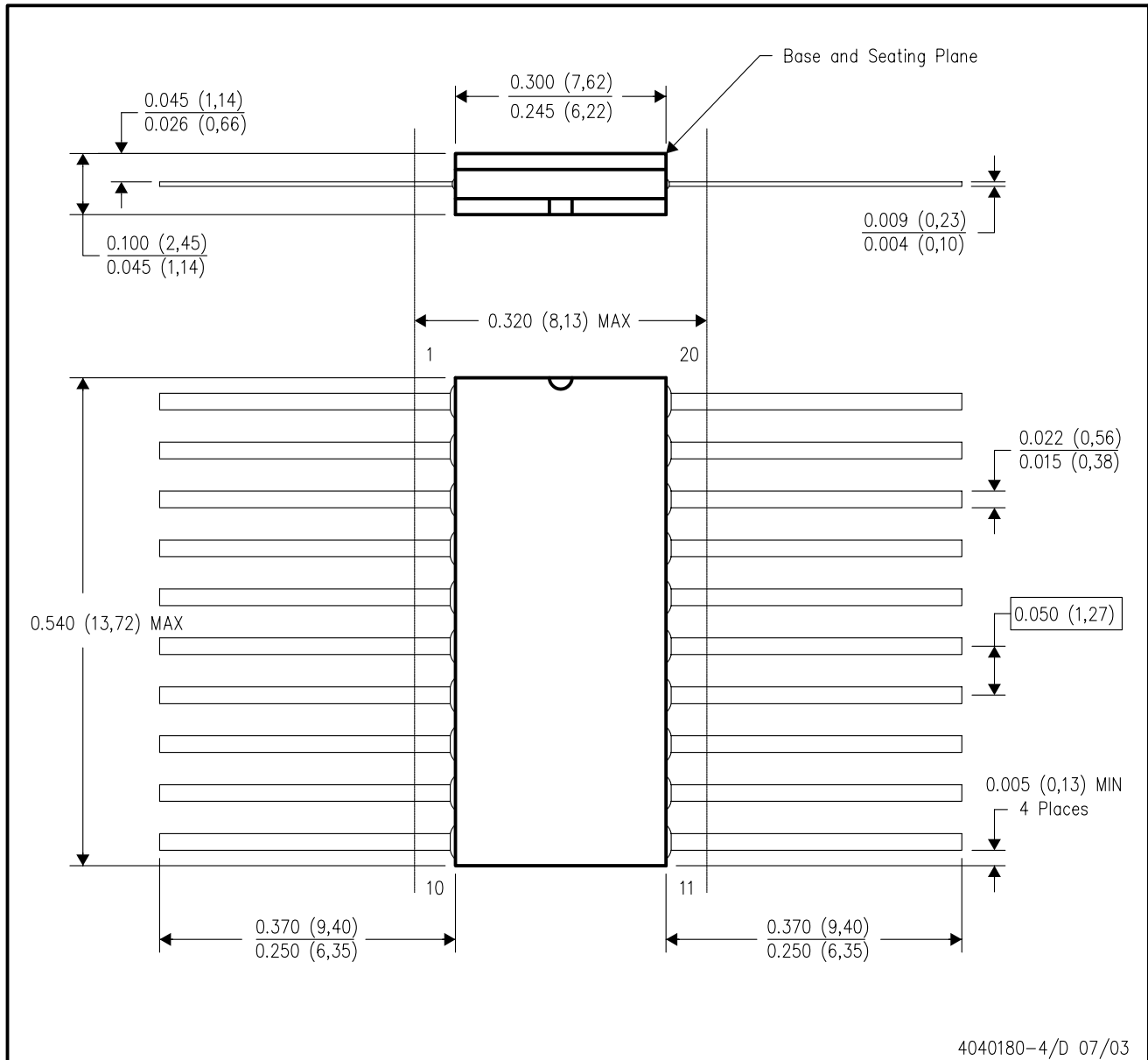
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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