



LVDS 4x4 CROSSPOINT SWITCH

FEATURES

- Signaling Rates >1.5 Gbps per Channel
- Supports Telecom/Datacom and HDTV Video Switching
- Non-Blocking Architecture Allows Each Output to be Connected to Any Input
- Compatible With ANSI TIA/EIA-644-A LVDS Standard
- 25 mV of Input Voltage Threshold Hysteresis
- Propagation Delay Times, 900 ps Typical
- Inputs Electrically Compatible With LVPECL, CML and LVDS Signal Levels
- Operates From a Single 3.3-V Supply
- Integrated 110-Ω Line Termination Resistors Available With SN65LVDT125A

APPLICATIONS

- Clock Buffering / Clock Muxing
- Wireless Base Stations
- High-Speed Network Routing
- HDTV Video Switching

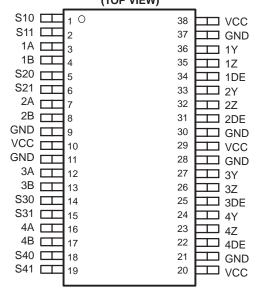
DESCRIPTION

The SN65LVDS125A and SN65LVDT125A are 4x4 nonblocking crosspoint switches. Low-voltage differential signaling (LVDS) is used to achieve signaling rates of 1.5 Gbps per channel. Each output driver includes a 4:1 multiplexer to allow any input to be routed to any output. Internal signal paths are fully differential to achieve the high signaling speeds while maintaining low signal skews. The SN65LVDT125A incorporates 110- Ω termination resistors for those applications where board space is a premium.

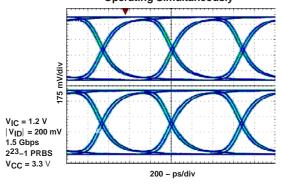
Designed to support signaling rates up to 1.5 Gbps for OC-12 clocks (622 MHz). The 1.5-Gbps signaling rate allows use in HDTV systems, including SMPTE 292 video applications requiring signaling rates of 1.485 Gbps.

The SN65LVDS125A and SN65LVDT125A are characterized for operation from –40°C to 85°C.

SN65LVDS125ADBT (Marked as LVDS125A) SN65LVDT125ADBT (Marked as LVDT125A) (TOP VIEW)



Eye Pattern of Two Outputs Operating Simultaneously





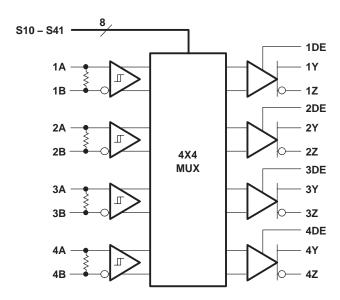
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LOGIC DIAGRAM

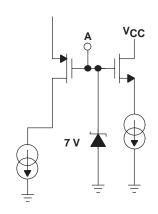


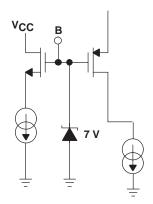
Integrated 110- Ω Termination on LVDT Only

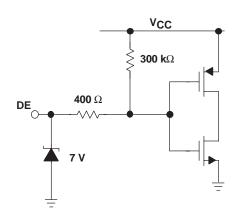


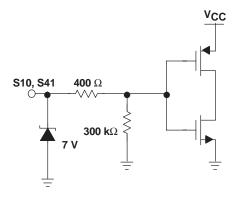
EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

INPUT LVDS125A

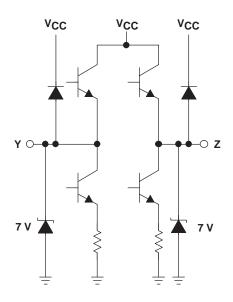








OUTPUT LVDS125A





CROSSPOINT LOGIC TABLES

OL	OUTPUT CHANNEL 1			JTPUT C	HANNEL 2	OUTPUT CHANNEL 3		Ol	JTPUT C	HANNEL 4	
CONTROL PINS				TROL NS	INPUT SELECTED	CON		INPUT SELECTED		TROL NS	INPUT SELECTED
S10	S11	1Y/1Z	S20	S21	2Y/2Z	S30	S31	3Y/3Z	S40	S41	4Y/4Z
0	0	1A/1B	0	0	1A/1B	0	0	1A/1B	0	0	1A/1B
0	1	2A/2B	0	1	2A/2B	0	1	2A/2B	0	1	2A/2B
1	0	3A/3B	1	0	3A/3B	1	0	3A/3B	1	0	3A/3B
1	1	4A/4B	1	1	4A/4B	1	1	4A/4B	1	1	4A/4B

PACKAGE DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	$T_{\mbox{A}} \le 25^{\circ}\mbox{C POWER}$ RATING	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 85°C POWER RATING
TSSOP (DBT)	High-K(2)	1772 mW	15.4 mW/°C	847 mW

⁽¹⁾ This is the inverse of the junction-to-ambient thermal resistance when board-mounded and with no air flow.

THERMAL CHARACTERISTICS

PARAMETER			TEST CONDITIONS	VALUE	UNITS
θЈВ	Junction-to-board thermal resista	nce		40.3	0000
θЈС	θ _{JC} Junction-to-case thermal resistance			8.5	°C/W
	Typical		V _{CC} = 3.3 V, T _A = 25°C, 750 MHZ	356	mW
P_{D}	Device power dissipation	Maximum	V _{CC} = 3.6 V, T _A = 85°C, 750 MHZ	522	mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

				UNITS	
Supply voltage range, v _{CC}				–0.5 V to 4 V	
	S, DE			–0.5 V to 4 V	
Malta na na an	(A, B)	(A, B)			
Voltage range	$ V_A - V_B $ (LVDT only)			1 V	
	(Y, Z)			–0.5 V to 4 V	
Electronic d'estre de cons	Human body model ⁽³⁾	All pins		±3 kV	
Electrostatic discharge	Charged-device model ⁽⁴⁾	All pins		±500 V	
Continuous power dissipation				See Dissipation Rating Table	
Storage temperature range				−65°C to 150°C	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ In accordance with the High-K thermal metric definitions of EIA/JESD51-6

⁽²⁾ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

⁽³⁾ Tested in accordance with JEDEC Standard 22, Test Method A114-A.

⁽⁴⁾ Tested in accordance with JEDEC Standard 22, Test Method C101.



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		3	3.3	3.6	V
High-level input voltage, VIH	S10-S41, 1DE-4DE	2			V
Low-level input voltage, V _{IL}	S10-S41, 1DE-4DE			0.8	V
	LVDS	0.1			V
Magnitude of differential input voltage V _{ID}	LVDT	0.1		0.8	V
Input voltage (any combination of commo	n-mode or input signals)	0		3.3	V
Junction temperature, T _J				140	°C
Operating free-air temperature, T _A (1)		-40		85	°C

⁽¹⁾ Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

TIMING SPECIFICATIONS

	ı	PARAMETER	MIN	NOM	MAX	UNIT
tSET	Input to select setup time			0.6		ns
tHOLD	Input to select hold time	See Figure 7		0.2		ns
†SWITCH	Select to switch output			1.2	1.6	ns

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{IT+}	Positive-going differential input voltage threshold		See Figure 1			100	mV	
V _{IT} -	Negative-going differential input voltage threshold		See Figure 1	-100			mV	
VID(HYS)	Differential input voltage hysteres	sis			25		mV	
l	1DE-4DE		V _{IH} = 2 V			-10		
liH	High-level input current	S10-S41	VIH = 2 V			20	μΑ	
1	Low level input ourrent	1DE-4DE	V 0.8 V			-10		
^¹ IL	Low-level input current	S10-S41	V _{IL} = 0.8 V			20	μΑ	
lį	Input current		V _I = 0 V or 3.3 V, second input at 1.2 V (other input open for LVDT)	-20		20	μА	
I _I (OFF)	Input current		$V_{CC} \le 1.5 \text{ V}, V_I = 0 \text{ V or } 3.3 \text{ V},$ second input at 1.2 V (other input open for LVDT)	-20		20	μА	
lio	Input offset current (I _{IA} - I _{IB}) ('L	LVDS)	$V_{IA} = V_{IB}$, $0 \le V_{IA} \le 3.3 \text{ V}$	-6		6	μΑ	
D_	Termination resistance ('LVDT)		$V_{ID} = 300 \text{ mV}, V_{IC} = 0 \text{ V to } 3.3 \text{ V}$	90	110	132	0	
RT	Termination resistance('LVDT with power-off)		$V_{ID} = 300 \text{ mV}, \ V_{IC} = 0 \text{ V to } 3.3 \text{ V}, \ V_{CC} = 1.5 \text{ V}$	90	110	132	Ω	
CT	Differential input capacitance				0.6		pF	

⁽¹⁾ All typical values are at 25°C and with a 3.3 V supply.



OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OD}	Differential output voltage magnitude	See Figure 2	247	350	454	mV
ΔIV _{OD} I	Change in differential output voltage magnitude between logic states	V _{ID} = ±100 mV	-50		50	mV
Voc(ss)	Steady-state common-mode output voltage		1.125		1.375	V
ΔVOC(SS)	Change in steady-state common-mode output voltage between logic states	See Figure 3	-50		50	mV
VOC(PP)	Peak-to-peak common-mode output voltage			50	150	mV
ICC	Supply current	$R_L=100\Omega$, $C_L=1$ pF		107	145	mA
los	Short-circuit output current	V_{OY} or $V_{OZ} = 0$ V	-27		27	mA
IOSD	Differential short circuit output current	V _{OD} = 0 V	-12		12	mA
loz	High-impedance output current	$V_O = 0 V \text{ or } V_{CC}$	-1		±1	μΑ
CO	Differential output capacitance			1.2		pF

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
^t PLH	Propagation delay time, low-to-high-level output		700	900	1200	
tPHL	Propagation delay time, high-to-low-level output		700	900	1200	
t _r	Differential output signal rise time (20%–80%)	See Figure 4		210	280	ps
t _f	Differential output signal fall time (20%–80%)			210	280	
tsk(p)	Pulse skew (tpHL - tpLH)(1)			0	50	ps
tsk(o)	Channel-to-channel output skew(2)				150	ps
t _{sk(pp)}	Part-to-part skew(3)				150	ps
^t jit(per)	Period jitter, rms (1 standard deviation) ⁽⁴⁾	750 MHz clock input ⁽⁵⁾ (see Figure 6)		0.4	3	ps
^t jit(cc)	Cycle-to-cycle jitter (peak) ⁽⁴⁾	750 MHz clock input ⁽⁶⁾ (see Figure 6)		4.7	13	ps
^t jit(pp)	Peak-to-peak jitter ⁽⁴⁾	1.5 Gbps 2 ²³ –1 PRBS input ⁽⁷⁾ (see Figure 6)		65	110	ps
^t jit(det)	Deterministic jitter, peak-to-peak(4)	1.5 Gbps 2 ⁷ –1 PRBS input ⁽⁸⁾ (see Figure 6)		56	90	ps
tPHZ	Propagation delay, high-level-to-high-impedance output				6	
tPLZ	Propagation delay, low-level-to-high-impedance output	7			6	
^t PZH	Propagation delay, high-impedance -to-high-level output	See Figure 5			300	ns
tpzL	Propagation delay, high-impedance-to-low-level output				300	

⁽¹⁾ $t_{SK(D)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.

⁽²⁾ $t_{sk(0)}$ is the maximum delay time difference between drivers over temperature, V_{CC}, and process.

⁽³⁾ $t_{SK(DD)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

⁽⁴⁾ Jitter specifications are based on design and characteriztion. Stimulus system jitter of 1.9 ps t_{jit(per)}, 16 ps t_{jit(cc)}. 17 ps t_{jit(pp)}, and 7.2 ps t_{jit(det)} have been subtracted from the values.

⁽⁵⁾ Input voltage = V_{ID} = 200 mV, 50% duty cycle at 750 MHz, t_{Γ} = t_{f} = 50 ps (20% to 80%), measured over 1000 samples.

⁽⁶⁾ Input voltage = V_{ID} = 200 mV, 50% duty cycle at 750 MHz, $t_r = t_f = 50$ ps (20% to 80%), measured over 1000 samples. (7) Input voltage = V_{ID} = 200 mV, 2²³–1 PRBS pattern at 1.5 Gbps, $t_r = t_f = 50$ ps (20% to 80%), measured over 200k samples. (8) Input voltage = V_{ID} = 200 mV, 2⁷–1 PRBS pattern at 1.5 Gbps, $t_r = t_f = 50$ ps (20% to 80%).



PARAMETER MEASUREMENT INFORMATION

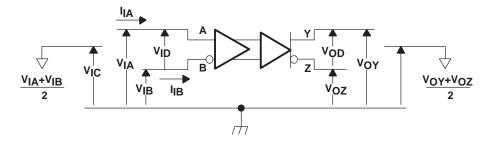


Figure 1. Voltage and Current Definitions

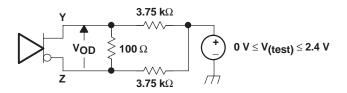
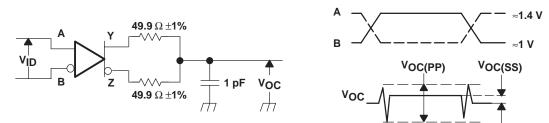
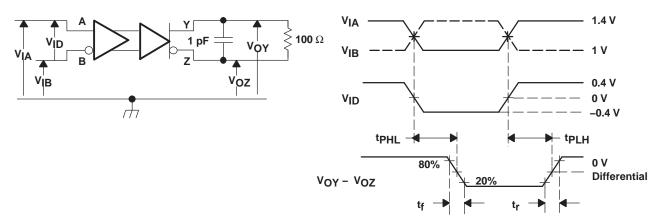


Figure 2. Differential Output Voltage (VOD) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns; R_L = 100W; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of V_{OC}(PP) is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

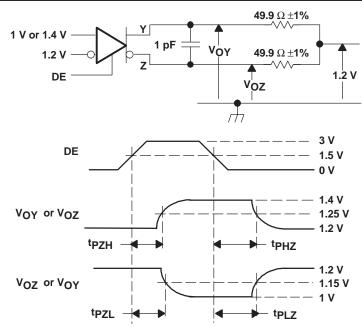
Figure 3. Test Circuit and Definitions fot the Driver Common-Mode Output Voltage



NOTE: All input pulses are supplied by a generator having the following characteristics: t_f or $t_f \le .25$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 \pm 10 ns . C_1 includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

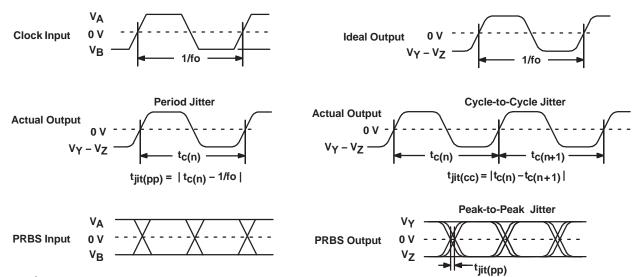
Figure 4. Timing Test Circuit and Waveforms





NOTE: A. All input pulses are supplied by a generator having the following characteristics: t_{Γ} or $t_{\Gamma} \le 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions



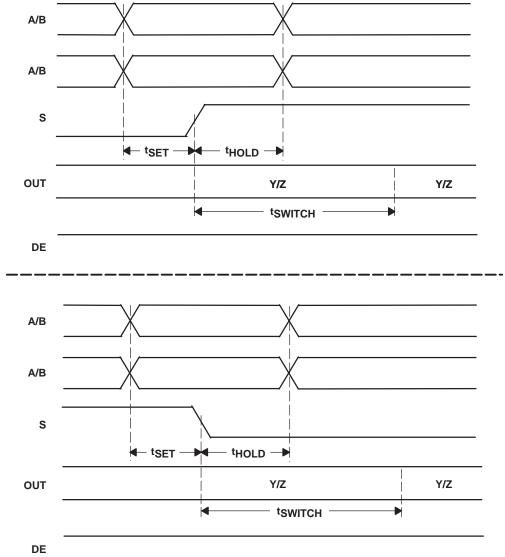
NOTE: A. All input pulses are supplied by an Agilent 81250 Stimulus System.

NOTE: B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software.

Figure 6. Driver Jitter Measurement Waveforms

SN65LVDS125A



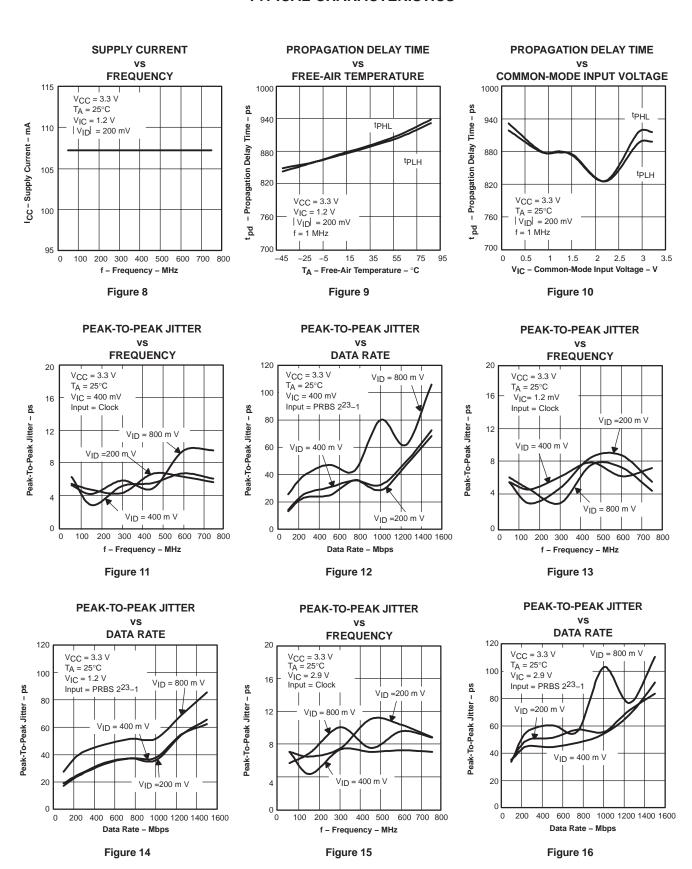


 $NOTE: \ \ t_{SET} \ and \ t_{HOLD} \ times \ specify \ that \ data \ must \ be \ in \ a \ stable \ state \ before \ and \ after \ mux \ control \ switches.$

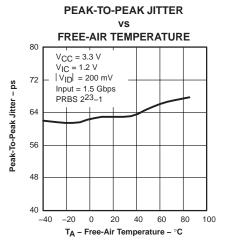
Figure 7. Input to Select for Both Rising and Falling Edge Setup and Hold Times



TYPICAL CHARACTERISTICS







PEAK-TO-PEAK JITTER DATA RATE 140 $V_{CC} = 3.3 \text{ V}$ 120 V_{IC} = 1.2 V $|V_{1D}| = 200 \text{ mV}$ Peak-To-Peak Jitter - ps T_A = 25°C 100 Input = PRBS 2²³–1 80 60 40 20 0 1500 2500 500 1000 2000 0

Figure 17

Figure 18

Data Rate - Mbps

DIFFERENTIAL OUTPUT VOLTAGE

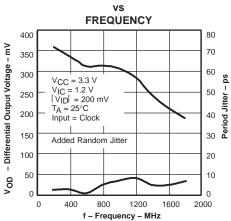


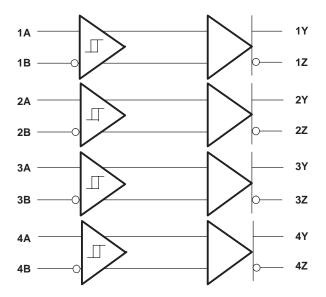
Figure 19



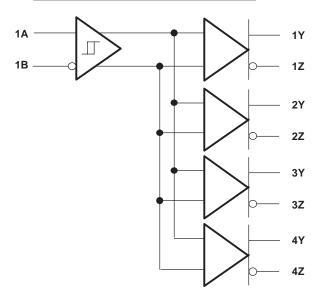
APPLICATION INFORMATION

CONFIGURATION EXAMPLES

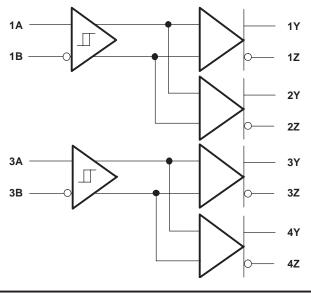
S10	S11	S20	S21
0	0	0	1
S30	S31	S40	S41
1	0	1	1



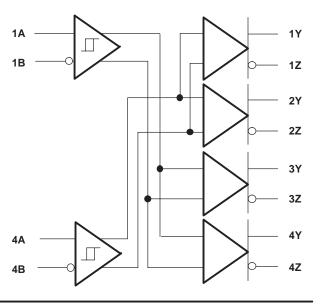
S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
0	0	0	0



S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
1	0	1	0



S10	S11	S20	S21
1	1	1	1
S30	S31	S40	S41
0	0	0	0





APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, ETC.)

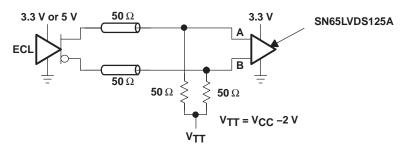


Figure 20. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

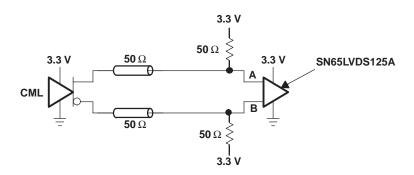


Figure 21. Current-Mode Logic (CML)

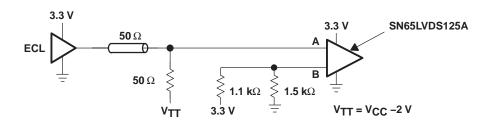


Figure 22. Single-Ended (LVPECL)

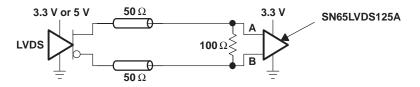


Figure 23. Low-Voltage Differential Signaling (LVDS)





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LVDS125ADBT	ACTIVE	SM8	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS125ADBTG4	ACTIVE	SM8	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS125ADBTR	ACTIVE	SM8	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS125ADBTRG4	ACTIVE	SM8	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDT125ADBT	ACTIVE	SM8	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDT125ADBTG4	ACTIVE	SM8	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDT125ADBTR	ACTIVE	SM8	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDT125ADBTRG4	ACTIVE	SM8	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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