EMC OPTIMIZED CAN TRANSCEIVER

FEATURES

- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **Improved Drop-In Replacement for the TJA1040**
- **Meets or Exceeds the Requirements of ISO 11898-5**
- **GIFT / ICT Compliant**
- **ESD Protection up to ±8 kV (Human-Body Model) on Bus Pins**
- **Low-Current Standby Mode With Bus Wake-Up, <12 μA Max**
- **High Electromagnetic Immunity (EMI)**
- **Low Electromagnetic Emissions (EME)**
- **Bus-Fault Protection of –27 V to 40 V**
- **Dominant Time-Out Function**
- **Thermal Shutdown Protection**
- **Power-Up/Down Glitch-Free Bus Inputs and Outputs**
  - **High Input Impedance with Low V_{CC}**
  - **Monotonic Outputs During Power Cycling**

APPLICATIONS

- **GMW3122 Dual-Wire CAN Physical Layer**
- **SAE J2284 High-Speed CAN for Automotive Applications**
- **SAE J1939 Standard Data Bus Interface**
- **ISO 11783 Standard Data Bus Interface**
- **NMEA 2000 Standard Data Bus Interface**
- **Industrial Automation**
  - **DeviceNet™ Data Buses (Vendor ID #806)**

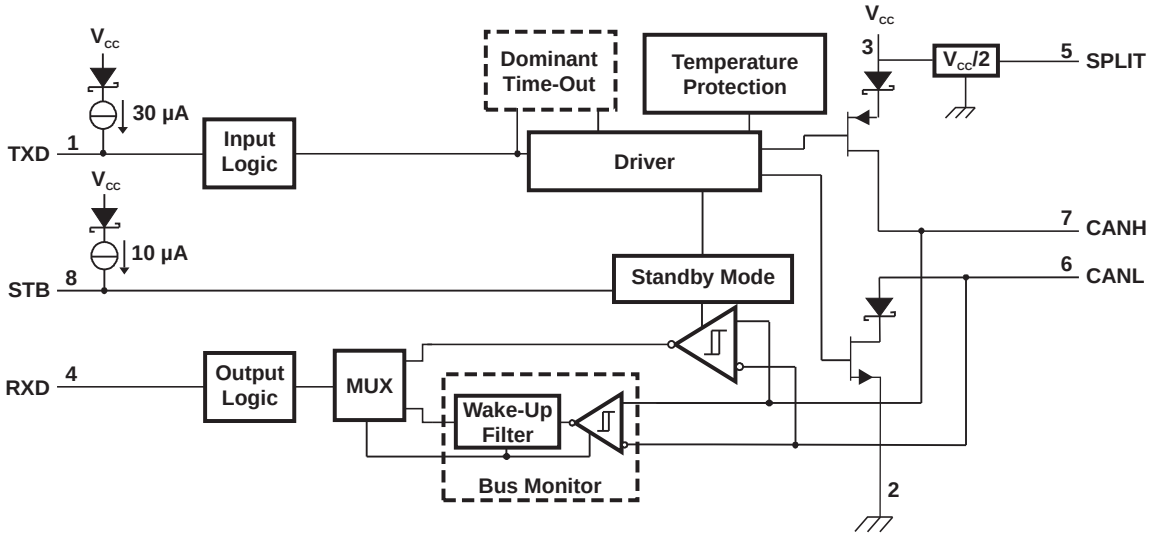
DESCRIPTION

The SN65HVD1040 meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN). The device is qualified for use in automotive applications.

As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps)(1).

(1) The signaling rate of a line is the number of voltage transitions that are made per second, expressed in the units bps (bits per second).

FUNCTIONAL BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Designed for operation in especially harsh environments, the SN65HVD1040 features cross-wire, over-voltage, and loss of ground protection from –27 V to 40 V, over-temperature protection, a –12 V to 12 V common-mode range, and withstands voltage transients from –200 V to 200 V, according to ISO 7637.

STB (pin 8) provides two different modes of operation: high-speed mode or low-current standby mode. The high-speed mode of operation is selected by connecting STB (pin 8) to ground.

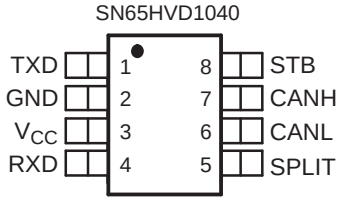
If a high logic level is applied to the STB pin of the SN65HVD1040, the device enters a low-current standby mode, while the receiver remains active in a low-power bus-monitor standby mode.

In the low-current standby mode, a dominant bit greater than 5 μs on the bus is passed by the bus-monitor circuit to the receiver output. The local protocol controller may then reactivate the device when it needs to transmit to the bus.

A dominant-time-out circuit in the SN65HVD1040 prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

SPLIT (pin 5) is available as a $V_{CC}/2$ common-mode bus voltage bias for a split-termination network (see application information) .

The SN65HVD1040 is characterized for operation from –40°C to 125°C.



ORDERING INFORMATION(1)

PART NUMBER	PACKAGE	MARKED AS	ORDERING NUMBER
SN65HVD1040-Q1	SOIC-8	H1040Q	SN65HVD1040QDRQ1 (reel)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

		VALUE
V_{CC}	Supply voltage	–0.3 V to 7 V
	Voltage range at bus terminals (CANH, CANL, SPLIT)	–27 V to 40 V
I_O	Receiver output current	20 mA
V_I	Voltage input, transient pulse(3) (CANH, CANL)	–200 V to 200 V
V_I	Voltage input range (TXD, STB)	–0.5 V to 6 V
T_J	Junction temperature	–40°C to 170°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6, and 7.

ELECTROSTATIC DISCHARGE PROTECTION

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		VALUE
Electrostatic discharge(1)	Human-Body Model(2)	Bus terminals (CANH, CANL, SPLIT) and GND	±8 kV
		All pins	±4 kV
	Charged-Device Model(3)	All pins	±1 kV
	Machine Model		±200 V

(1) All typical values at 25°C.
(2) Tested in accordance JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
V_{IH}	High-level input voltage	TXD, STB	2	5.25	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{ID}	Differential input voltage		–6	6	V
I_{OH}	High-level output current	Driver	–70		mA
		Receiver	–2		
I_{OL}	Low-level output current	Driver		70	mA
		Receiver		2	
T_J	Junction temperature	See *Thermal Characteristics* table		150	°C

SUPPLY CURRENT

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	5-V supply current	Standby mode	STB at V_{CC}, $V_I = V_{CC}$		6	12	µA
		Dominant	V_I = 0 V, 60-Ω load, STB at 0 V		50	70	mA
		Recessive	$V_I = V_{CC}$, No load, STB at 0 V		6	10	

DEVICE SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	Figure 9, STB at 0 V	90	230	ns
$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive		90	230	

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 1 and Figure 2	2.9	3.4	4.5	V
		CANL		0.8		1.75	
$V_{O(R)}$	Bus output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 1 and Figure 2	2	2.5	3	V
V_O	Bus output voltage (standby mode)		STB at Vcc, R_L = 60 Ω, See Figure 1 and Figure 2	–0.1		0.1	V
$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, STB at 0 V, See Figure 1, Figure 2, and Figure 3	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, STB at 0 V, See Figure 1, Figure 2, and Figure 3	1.4		3	V
$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 1 and Figure 2	–0.012		0.012	V
			V_I = 3 V, STB at 0 V, No Load	–0.5		0.05	
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$)		STB at 0 V, R_L = 60 Ω, See Figure 13	0.9 V_{CC}	V_{CC}	1.1 V_{CC}	V
$V_{OC(ss)}$	Steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, Figure 8	2	2.3	3	V
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage				30		mV
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	µA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	
$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0 V, TXD at 5 V			1	
$I_{OS(ss)}$	Short-circuit steady-state output current		V_{CANH} = –12 V, CANL open, See Figure 11	–120	–85		mA
			V_{CANH} = 12 V, CANL open, See Figure 11		0.4	1	
			V_{CANL} = –12 V, CANH open, See Figure 11	–1	–0.6		
			V_{CANL} = 12 V, CANH open, See Figure 11		75	120	
C_O	Output capacitance		See receiver input capacitance				

(1) All typical values are at 25°C with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	STB at 0 V, See Figure 4	25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low level output		25	45	120	
t_r	Differential output signal rise time			25		
t_f	Differential output signal fall time			45		
t_{en}	Enable time from standby mode to dominant	See Figure 7			10	µs
$t_{(dom)}$	Dominant time-out	↓V_I, See Figure 10	300	450	700	µs

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, high-speed mode	STB at 0 V, See Table 1		800	900	mV
V_{IT-}	Negative-going input threshold voltage, high-speed mode		500	650		
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		100	125		
V_{IT}	Input threshold voltage, standby mode	STB at V_{CC}	500		1150	
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 6	4	4.6		V
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 6		0.2	0.4	V
$I_{I(off)}$	Power-off bus input current	CANH = CANL = 5 V, V_{CC} at 0 V, TXD at 0 V			3	µA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, RXD at 5 V			20	µA
C_I	Input capacitance to ground, (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		12		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		2		
R_{ID}	Differential input resistance	TXD at 3 V, STB at 0 V	30		80	kΩ
R_{IN}	Input resistance, (CANH or CANL)		15	30	40	
$R_{I(m)}$	Input resistance matching $[1 - (R_{IN\ (CANH)} / R_{IN\ (CANL)})] \times 100\%$	$V_{(CANH)} = V_{(CANL)}$	–3	0	3	%

(1) All typical values are at 25°C with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V , See Figure 6	60	90	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output		45	70	130	ns
t_r	Output signal rise time			8		ns
t_f	Output signal fall time			8		ns
t_{BUS}	Dominant time required on bus for wake-up from standby	STB at V_{CC}, See Figure 12	1.5		5	µs

STB PIN CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_{IH}	High-level input current	STB at V_{CC}	–10	0	µA
I_{IL}	Low-level input current	STB at 0 V	–10	0	

SPLIT PIN CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	–500 µA < I_O < 500 µA	0.3 V_{CC}	0.5 V_{CC}	0.7 V_{CC}	V
$I_{O(stb)}$	Leakage current, standby mode	STB at 2 V, –12 V ≤ V_O ≤ 12 V	–5		5	µA

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	Low-K thermal resistance(1)		211		°C/W
		High-K thermal resistance		131		
θ_{JB}	Junction-to-board thermal resistance			53		
θ_{JC}	Junction-to-case thermal resistance			79		
P_D	Average power dissipation	V_{CC} = 5 V, T_j = 27°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF		112		mW
		V_{CC} = 5.5 V, T_j = 130°C, R_L = 45 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF			170	
	Thermal shutdown temperature			185		°C

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages.

FUNCTION TABLES

DRIVER

INPUTS		OUTPUTS		BUS STATE
TXD(1)	STB(1)	CANH(1)	CANL(1)	
L	L	H	L	DOMINANT
H	X	Z	Z	RECESSIVE
Open	X	Z	Z	RECESSIVE
X	H or Open	Z	Z	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

RECEIVER

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	STB	OUTPUT RXD(1)	BUS STATE
$V_{ID} \geq 0.9$ V	L	L	DOMINANT
$V_{ID} \geq 1.15$ V	H or Open	L	DOMINANT
0.5 V < V_{ID} < 0.9 V	X	?	?
$V_{ID} \leq 0.5$ V	X	H	RECESSIVE
Open	X	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

PARAMETER MEASUREMENT INFORMATION

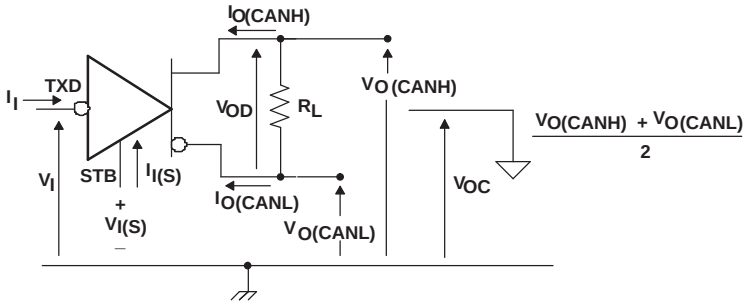


Figure 1. Driver Voltage, Current, and Test Definition

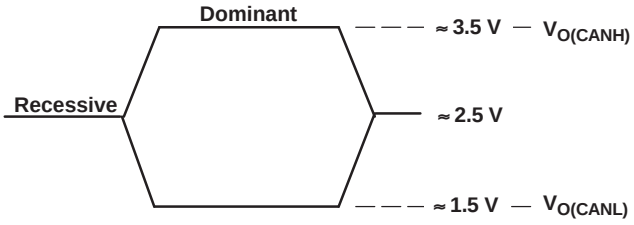


Figure 2. Bus Logic-State Voltage Definitions

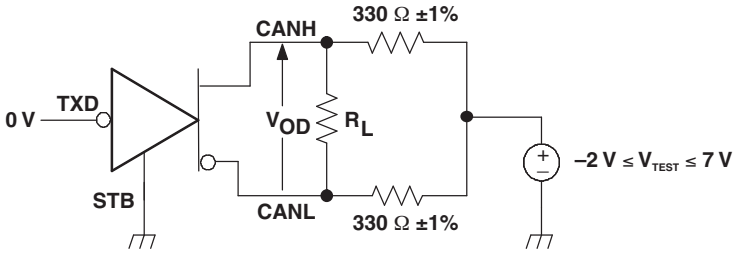


Figure 3. Driver V_{OD} Test Circuit

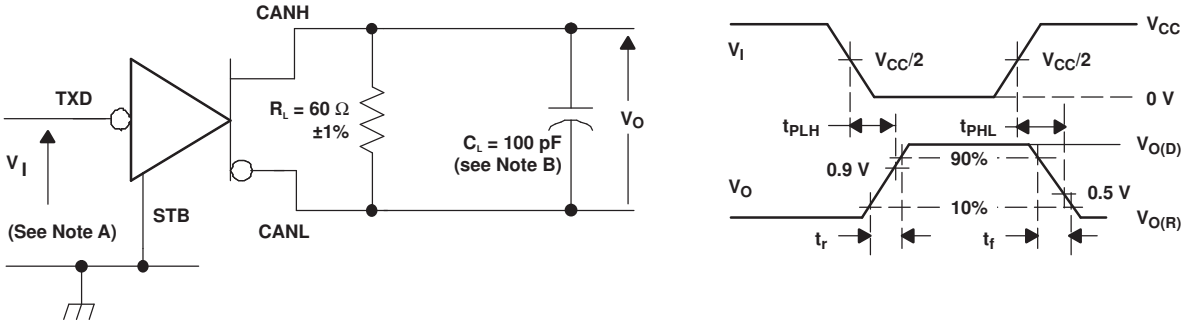


Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

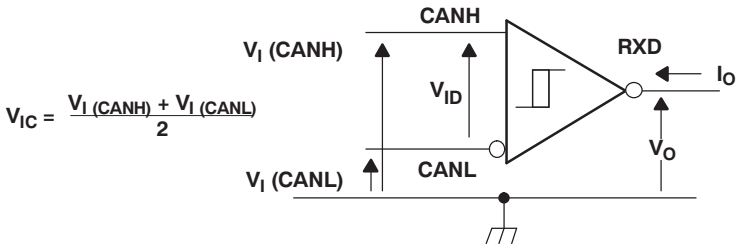
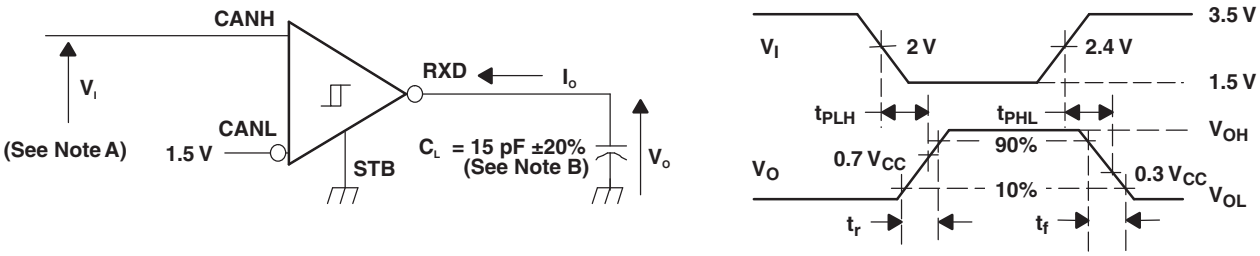


Figure 5. Receiver Voltage and Current Definitions



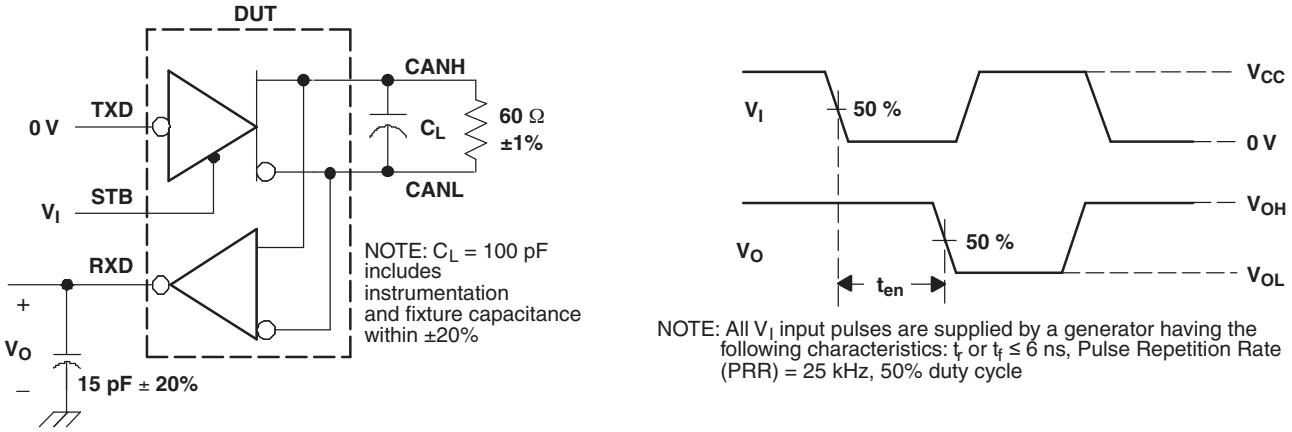
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms

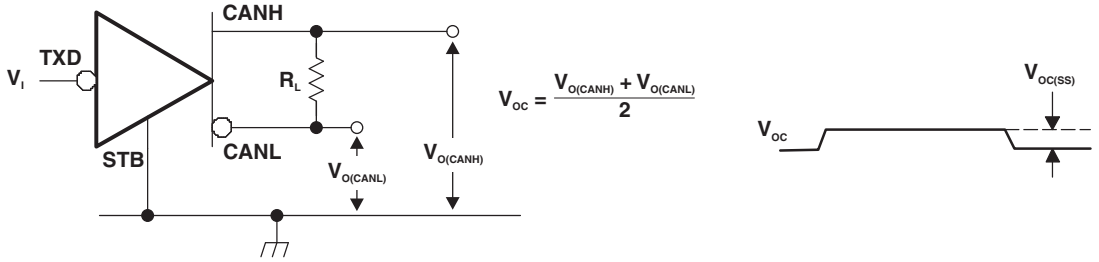
Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	



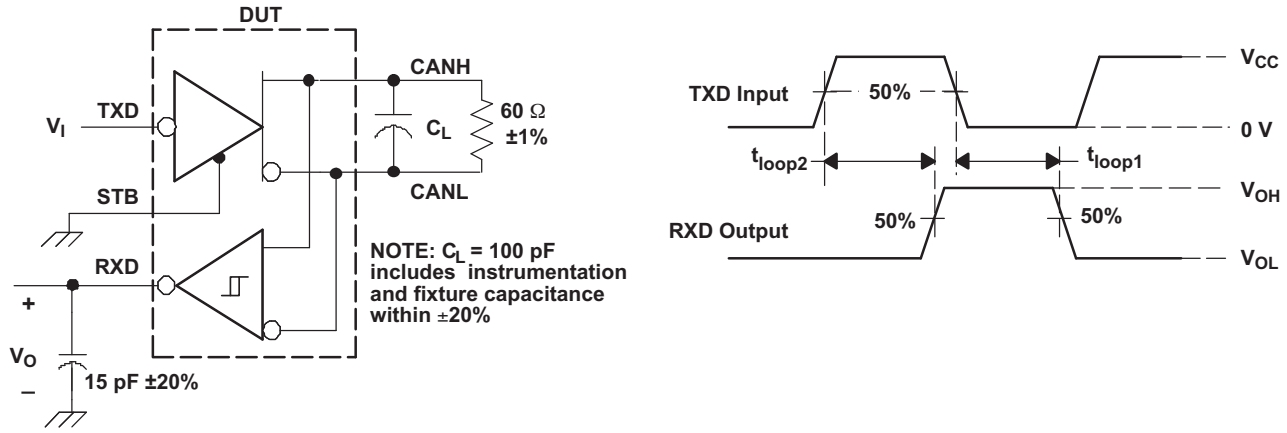
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, Pulse Repetition Rate (PRR) = 25 kHz, 50% duty cycle

Figure 7. t_{en} Test Circuit and Waveform



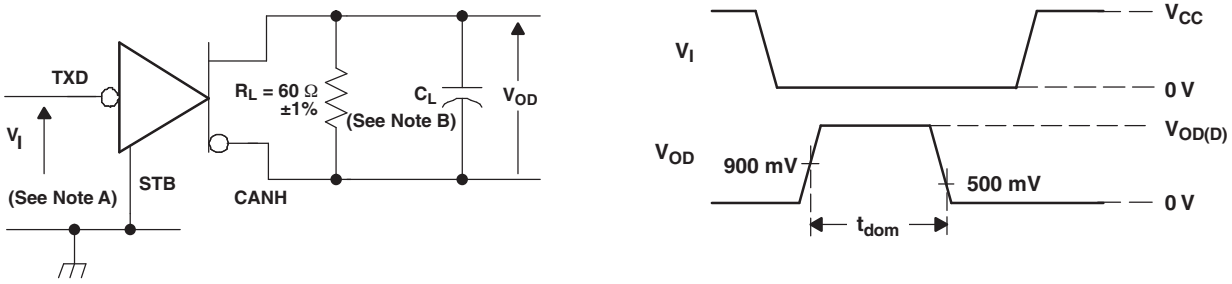
NOTE: All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. Common-Mode Output Voltage Test and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. $t_{(LOOP)}$ Test Circuit and Waveform



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or $t_f \le 6$ ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 10. Dominant Time-Out Test Circuit and Waveforms

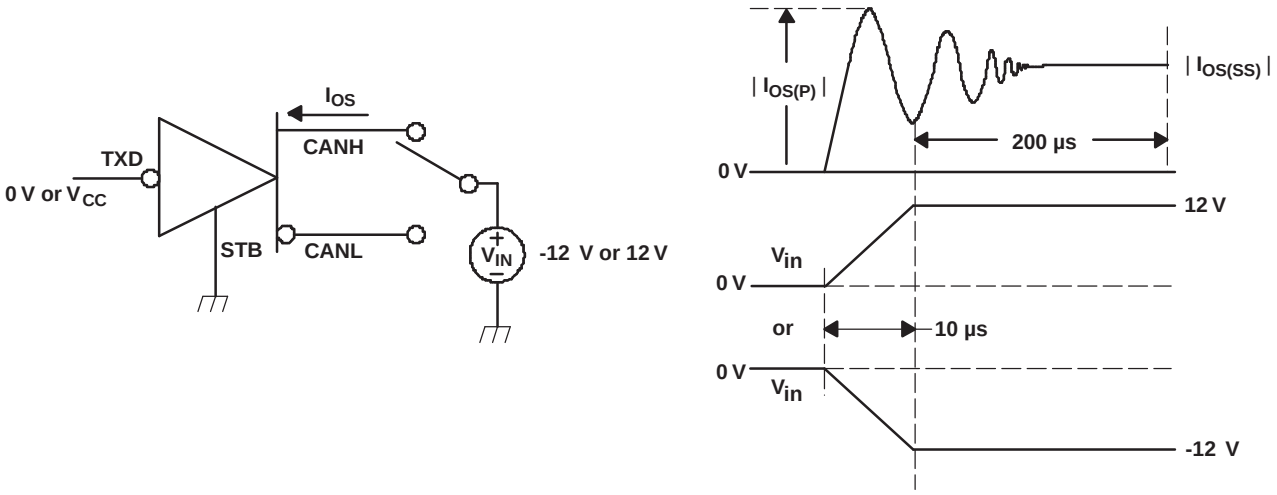
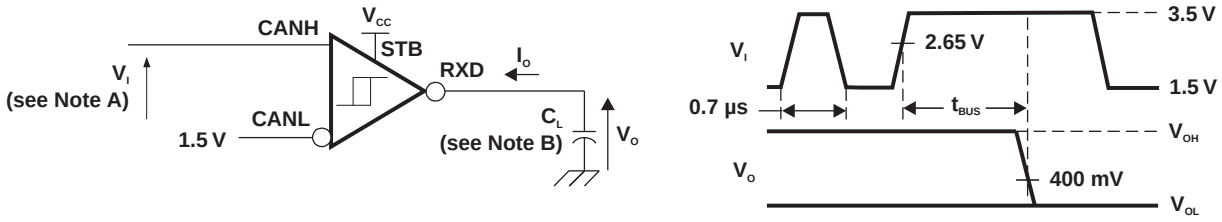


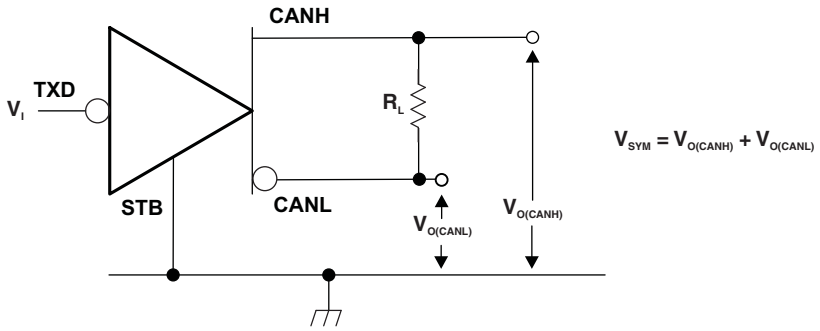
Figure 11. Driver Short-Circuit Current Test and Waveform



A. For V_I bit width ≤ 0.7 µs, $V_O = V_{OH}$. For V_I bit width ≥ 5 µs, $V_O = V_{OL}$. V_I input pulses are supplied from a generator with the following characteristics: $t_r/t_f < 6$ ns.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

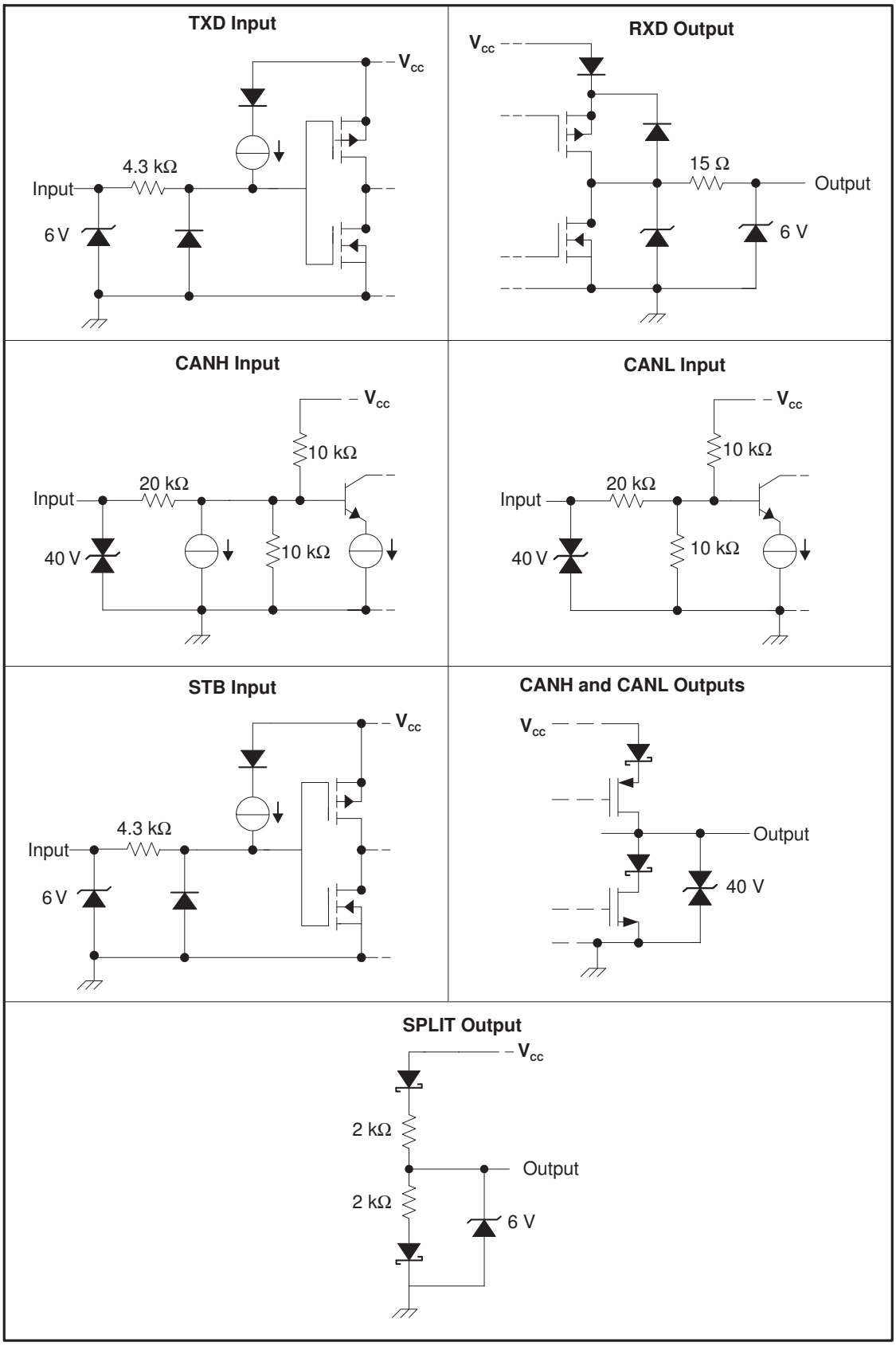
Figure 12. t_{BUS} Test Circuit and Waveform



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: $t_r/t_f \leq 6$ ns, Pulse Repetition Rate (PRR) = 250 kHz, 50% duty cycle.

Figure 13. Driver Output Symmetry Test Circuit

Equivalent Input and Output Schematic Diagrams



APPLICATION INFORMATION

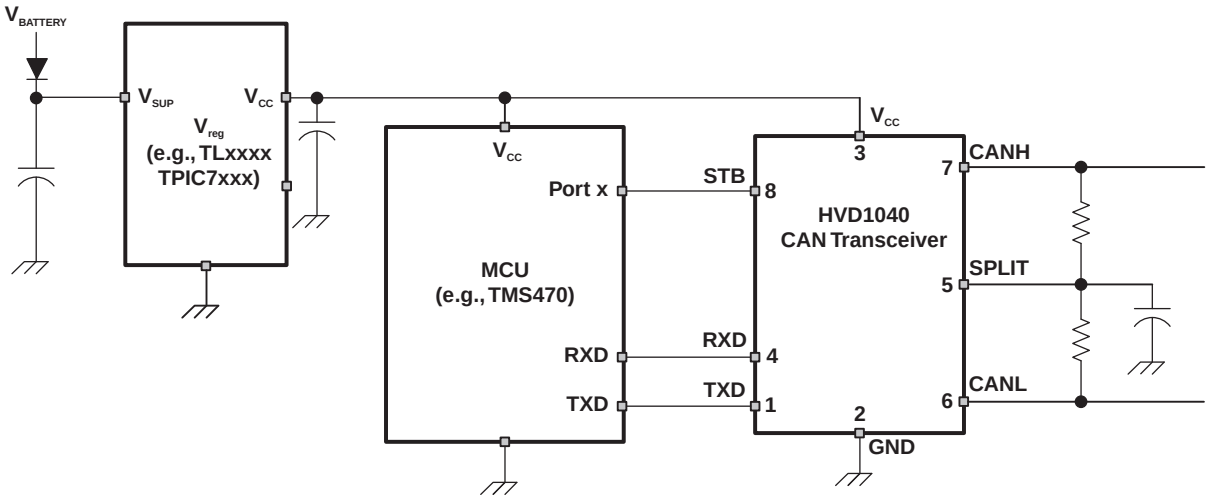


Figure 14. Typical Application Using Split Termination for Stabilization

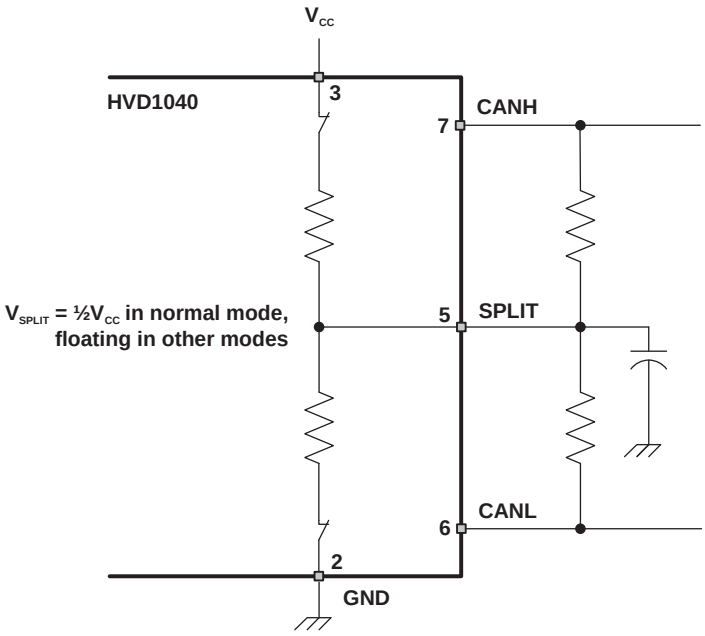


Figure 15. Split Pin Stabilization Circuitry and Application

PACKAGING INFORMATION

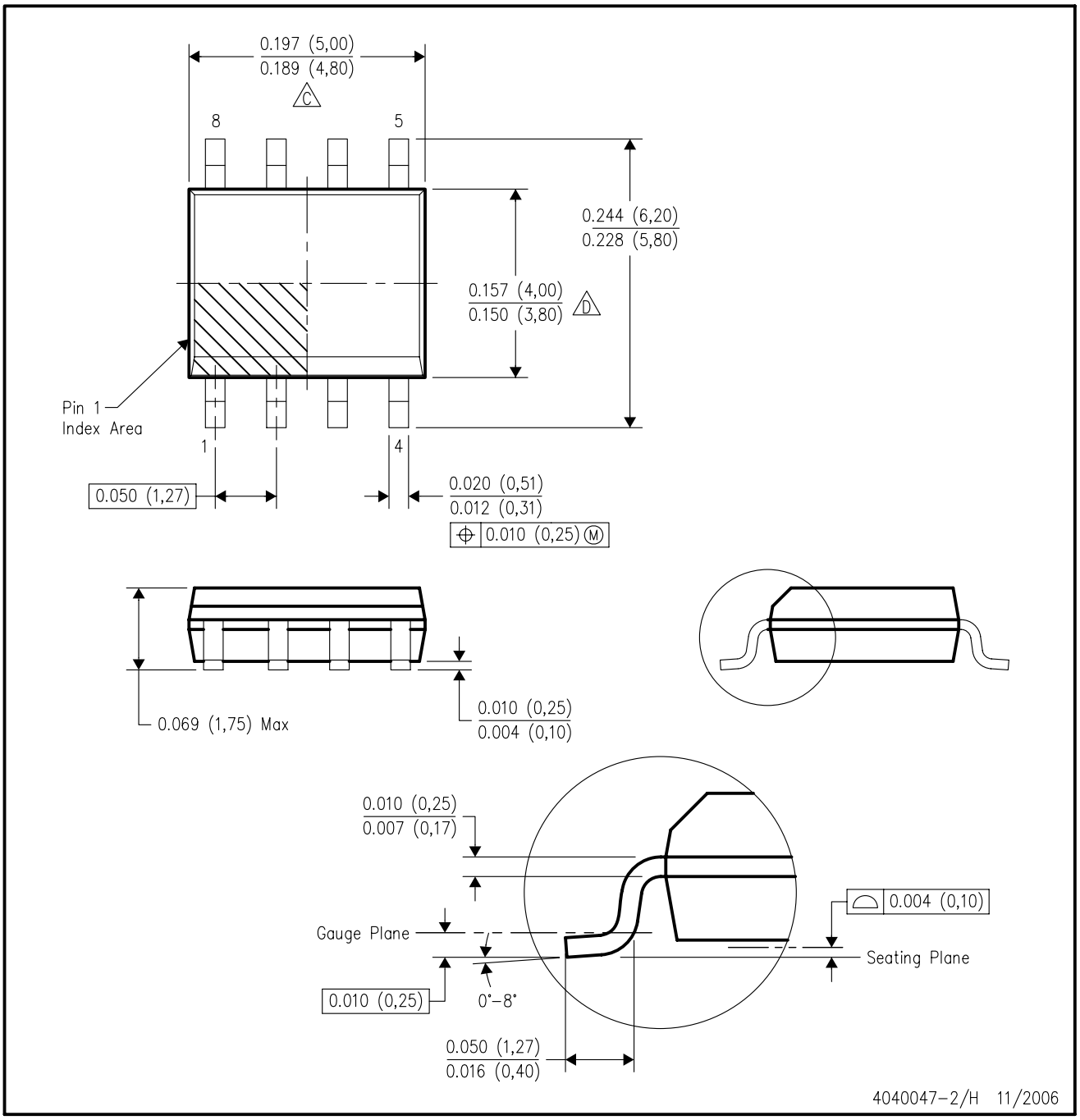
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65HVD1040QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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