



DIFFERENTIAL TRANSLATOR/REPEATER

FEATURES

- Designed for Signaling Rates ⁽¹⁾ ≥ 2 Gbps
- Total Jitter < 65 ps
- Low-Power Alternative for the MC100EP16
- Low 100 ps (Max) Part-To-Part Skew
- 25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range
- Inputs Electrically Compatible With LVPECL, CML, and LVDS Signal Levels
- 3.3-V Supply Operation
- LVDT Integrates 110- Ω Terminating Resistor
- Offered in SOIC and MSOP

APPLICATIONS

- 622 MHz Central Office Clock Distribution
- High-Speed Network Routing
- Wireless Basestations
- Low Jitter Clock Repeater
- Serdes LVPECL Output to FPGA LVDS Input Translator

- (1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

DESCRIPTION

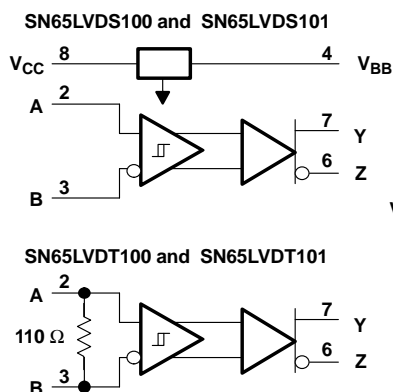
The SN65LVDS100, SN65LVDT100, SN65LVDS101, and SN65LVDT101 are a high-speed differential receiver and driver connected as a repeater. The receiver accepts low-voltage differential signaling (LVDS), positive-emitter-coupled logic (PECL), or current-mode logic (CML) input signals at rates up to 2 Gbps and repeats it as either an LVDS or PECL output signal. The signal path through the device is differential for low radiated emissions and minimal added jitter.

The outputs of the SN65LVDS100 and SN65LVDT100 are LVDS levels as defined by TIA/EIA-644-A. The outputs of the SN65LVDS101 and SN65LVDT101 are compatible with 3.3-V PECL levels. Both drive differential transmission lines with nominally 100- Ω characteristic impedance.

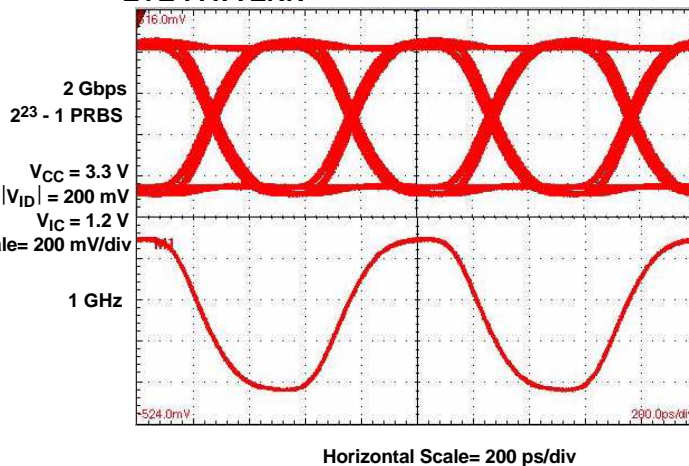
The SN65LVDT100 and SN65LVDT101 include a 110- Ω differential line termination resistor for less board space, fewer components, and the shortest stub length possible. They do not include the V_{BB} voltage reference found in the SN65LVDS100 and SN65LVDS101. V_{BB} provides a voltage reference of typically 1.35 V below V_{CC} for use in receiving single-ended input signals and is particularly useful with single-ended 3.3-V PECL inputs. When not used, V_{BB} should be unconnected or open.

All devices are characterized for operation from -40°C to 85°C .

FUNCTIONAL DIAGRAM



EYE PATTERN



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

OUTPUT	TERMINATION RESISTOR	V _{BB}	PART NUMBER ⁽¹⁾	PART MARKING	PACKAGE
LVDS	No	Yes	SN65LVDS100D	DL100	SOIC
LVDS	No	Yes	SN65LVDS100DGK	AZK	MSOP
LVDS	Yes	No	SN65LVDT100D	DE100	SOIC
LVDS	Yes	No	SN65LVDT100DGK	AZL	MSOP
LVPECL	No	Yes	SN65LVDS101D	DL101	SOIC
LVPECL	No	Yes	SN65LVDS101DGK	AZM	MSOP
LVPECL	Yes	No	SN65LVDT101D	DE101	SOIC
LVPECL	Yes	No	SN65LVDT101DGK	BAF	MSOP

(1) Add the suffix R for taped and reeled carrier (i.e. SN65LVDS100DR).

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range unless otherwise noted

		UNIT	
V _{CC}	Supply voltage range ⁽²⁾	-0.5 V to 4 V	
I _{BB}	V _{BB} Output current	±0.5 mA	
V _I	Voltage range, (A, B, Y, Z)	0 V to 4.3 V	
V _O			
V _{ID}	Differential voltage, V _A - V _B ('LVDT100 and 'LVDT101 only)	1 V	
ESD	Human Body Model ⁽³⁾	A, B, Y, Z, and GND	±5 kV
		All pins	±2 kV
	Charged-Device Model ⁽⁴⁾	All pins	±1500 V
P _D	Continuous power dissipation	See Dissipation Rating Table	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

POWER DISSIPATION RATINGS

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 85°C POWER RATING
DGK	377 mW	3.8 mW/°C	151 mW
D	481 mW	4.8 mW/°C	192 mW

(1) This is the inverse of the junction-to-ambient thermal resistance with no air flow installed on the JESD51-3 low effective thermal conductivity test board for leadless surface mount packages.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Magnitude of differential input voltage $ V_{ID} $	'LVDS100 or 'LVDS101	0.1		1	V
	'LVDT100 or 'LVDT101	0.1		0.8	
Input voltage (any combination of common-mode or input signals), V_I		0		4	V
V_{BB} output current, $I_{O(V_{BB})}$		-400 ⁽¹⁾		12	μ A
Operating free-air temperature, T_A		-40		85	$^{\circ}$ C

(1) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I_{CC}	Supply current, 'LVDx100	No load or input	25		30	mA
	Supply current, 'LVDx101	$R_L = 50 \Omega$ to 1 V, No input	50		61	
P_D	Device power dissipation, 'LVDx100	$R_L = 100 \Omega$, No input			110	mW
	Device power dissipation, 'LVDx101	Y and Z to $V_{CC} - 2$ V through 50Ω , No input	116		142	
V_{BB}	Reference voltage output, 'LVDS100 or 'LVDS101	$I_O = -400 \mu$ A or 12μ A	$V_{CC}-1.4$	$V_{CC}-1.35$	$V_{CC}-1.3$	mV
SN65LVDS100 and SN65LVDS101 INPUT CHARACTERISTICS (see Figure 1)						
V_{IT+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		-100			
I_I	Input current	$V_I = 0$ V or 2.4 V, Second input at 1.2 V	-20		20	μ A
		$V_I = 4$ V, Second input at 1.2 V			33	μ A
$I_{I(OFF)}$	Power off input current	$V_{CC} = 1.5$ V, $V_I = 0$ V or 2.4 V, Second input at 1.2 V	-20		20	μ A
		$V_{CC} = 1.5$ V, $V_I = 4$ V, Second input at 1.2 V			33	
I_{IO}	Input offset current ($ I_{IA} - I_{IB} $)	$V_{IA} = V_{IB}$, $0 \leq V_{IA} \leq 4$ V	-6		6	μ A
C_i	Small-signal input capacitance to GND	$V_I = 1.2$ V			0.6	pF
SN65LVDT100 and SN65LVDT101 INPUT CHARACTERISTICS (see Figure 1)						
V_{IT+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		-100			
I_I	Input current	$V_I = 0$ V or 2.4 V, Other input open	-40		40	μ A
		$V_I = 4$ V, Other input open			66	
$I_{I(OFF)}$	Power off input current	$V_{CC} = 1.5$ V, $V_I = 0$ V or 2.4 V, Other input open	-40		40	μ A
		$V_{CC} = 1.5$ V, $V_I = 4$ V, Other input open			66	
$R_{(T)}$	Differential input resistance	$V_{ID} = 300$ mV or 500 mV, $V_{IC} = 0$ V or 2.4 V	90	110	132	Ω
		$V_{CC} = 0$ V, $V_{ID} = 300$ mV or 500 mV, $V_{IC} = 0$ V or 2.4 V	90	110	132	
C_i	Small-signal differential input capacitance	$V_I = 1.2$ V			0.6	pF

(1) Typical values are with a 3.3-V supply voltage and room temperature

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
SN65LVDS100 and SN65LVDT100 OUTPUT CHARACTERISTICS (see Figure 1)						
$ V_{OD} $	Differential output voltage magnitude	See Figure 2	247	340	454	mV
$\Delta V_{OD} $	Change in differential output voltage magnitude between logic states		-50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{OS}	Short-circuit output current	$V_{O(Y)}$ or $V_{O(Z)} = 0$ V	-24		24	mA
$I_{OS(D)}$	Differential short-circuit output current	$V_{OD} = 0$ V	-12		12	mA
SN65LVDS101 and SN65LVDT101 OUTPUT CHARACTERISTICS (see Figure 1)						
V_{OH}	High-level output voltage	50 Ω to $V_{CC} - 2$ V, See Figure 4	$V_{CC} - 1.25$	$V_{CC} - 1.02$	$V_{CC} - 0.9$	V
		$V_{CC} = 3.3$ V, 50- Ω load to 2.3 V	2055	2280	2405	mV
V_{OL}	Low-level output voltage	50 Ω to $V_{CC} - 2$ V, See Figure 4	$V_{CC} - 1.83$	$V_{CC} - 1.61$	$V_{CC} - 1.53$	V
		$V_{CC} = 3.3$ V, 50- Ω load to 2.3 V	1475	1690	1775	mV
$ V_{OD} $	Differential output voltage magnitude	50- Ω load to $V_{CC} - 2$ V, See Figure 4	475	575	750	mV

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
t_{PLH}	Propagation delay time, low-to-high-level output	'LVDx100	300	470	800	ps	
		'LVDx101	400	630	900		
t_{PHL}	Propagation delay time, high-to-low-level output	'LVDx100	300	470	800	ps	
		'LVDx100	400	630	900		
t_r	Differential output signal rise time (20%–80%)	See Figure 5			220	ps	
t_f	Differential output signal fall time (20%–80%)				220	ps	
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $) ⁽²⁾			5	50	ps	
$t_{sk(pp)}$	Part-to-part skew ⁽³⁾		$V_{ID} = 0.2$ V, See Figure 5			100	ps
$t_{jit(per)}$	RMS period jitter ⁽⁴⁾		1 GHz 50% duty cycle square wave input, $V_{ID} = 200$ mV, $V_{IC} = 1.2$ V, See Figure 6		1	3.7	ps
$t_{jit(cc)}$	Peak cycle-to-cycle jitter ⁽⁵⁾			6	23	ps	
$t_{jit(pp)}$	Peak-to-peak jitter	2 GHz PRBS, $2^{23} - 1$ run length, $V_{ID} = 200$ mV, $V_{IC} = 1.2$ V, See Figure 6		28	65	ps	
$t_{jit(det)}$	Peak-to-peak deterministic jitter ⁽⁶⁾	2 GHz PRBS, $2^7 - 1$ run length, $V_{ID} = 200$ mV, $V_{IC} = 1.2$ V, See Figure 6		17	48	ps	

(1) All typical values are at 25°C and with a 3.3 V supply.

(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.

(3) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay time between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(4) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 1,000,000 cycles.

(5) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles, over a random sample of 1,000 adjacent cycle pairs.

(6) Deterministic jitter is the sum of pattern-dependent jitter and pulse-width distortion.

PARAMETER MEASUREMENT INFORMATION

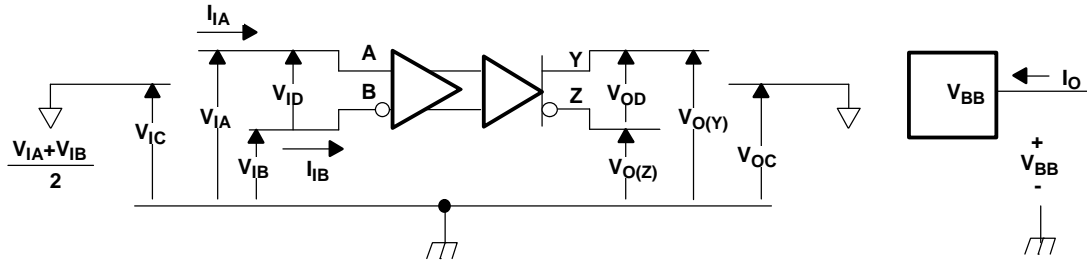


Figure 1. Voltage and Current Definitions

Table 1. Receiver Input Voltage Threshold Test

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT ⁽¹⁾
V _{IA}	V _{IB}	V _{ID}	V _{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	-100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4.0 V	-100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	-100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	-1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	-1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	-1000 mV	0.5 V	L

(1) H = high level, L = low level

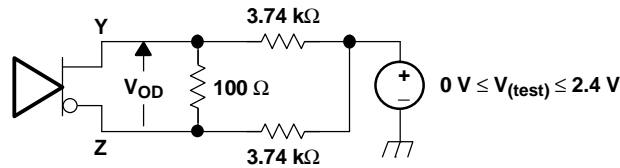
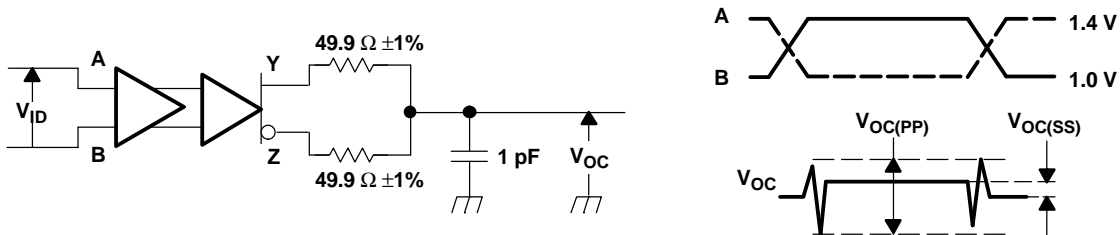


Figure 2. SN65LVDS100 Differential Output Voltage (V_{OD}) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 0.25$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the SN65LVDS100 Driver Common-Mode Output Voltage

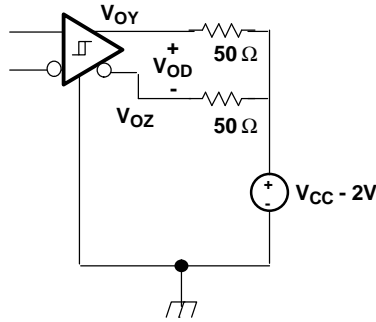
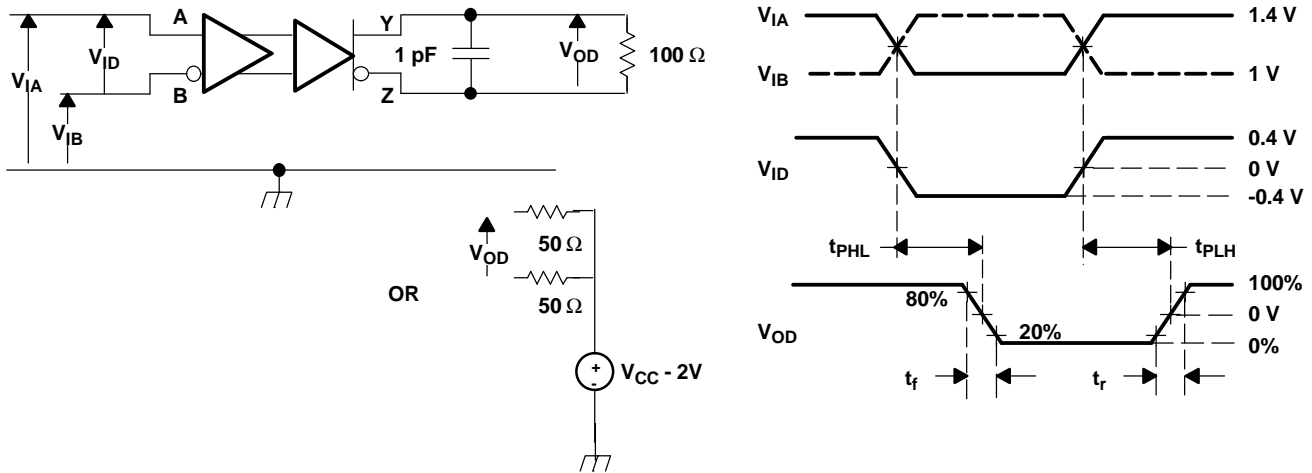


Figure 4. Typical Termination for LVPECL Output Driver (65LV Dx101)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 0.25$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. Measurement equipment provides a bandwidth of 5 GHz minimum.

Figure 5. Timing Test Circuit and Waveforms

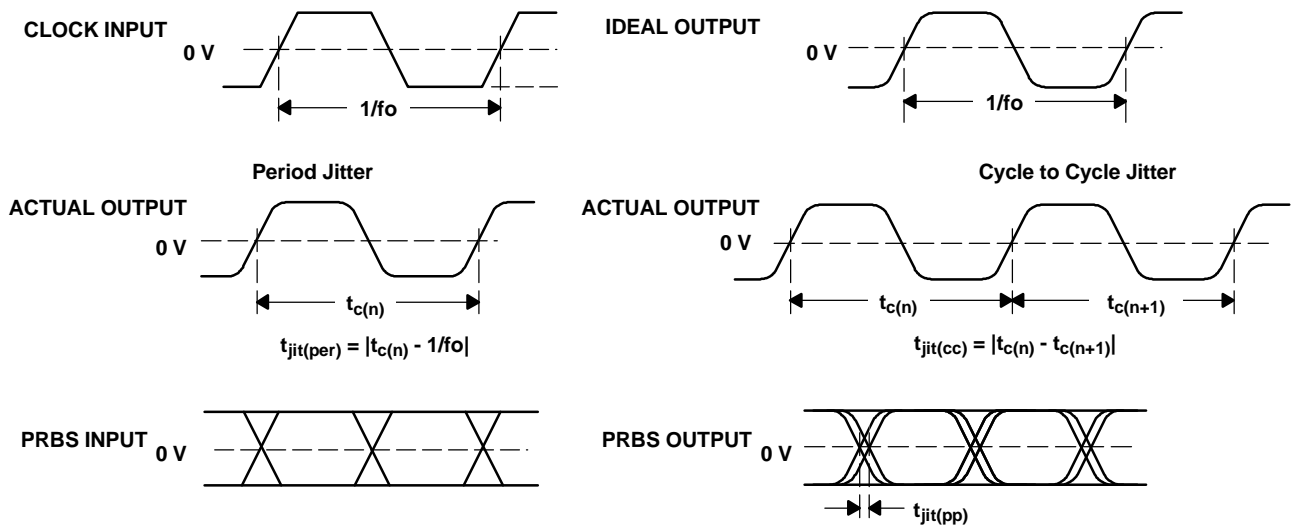
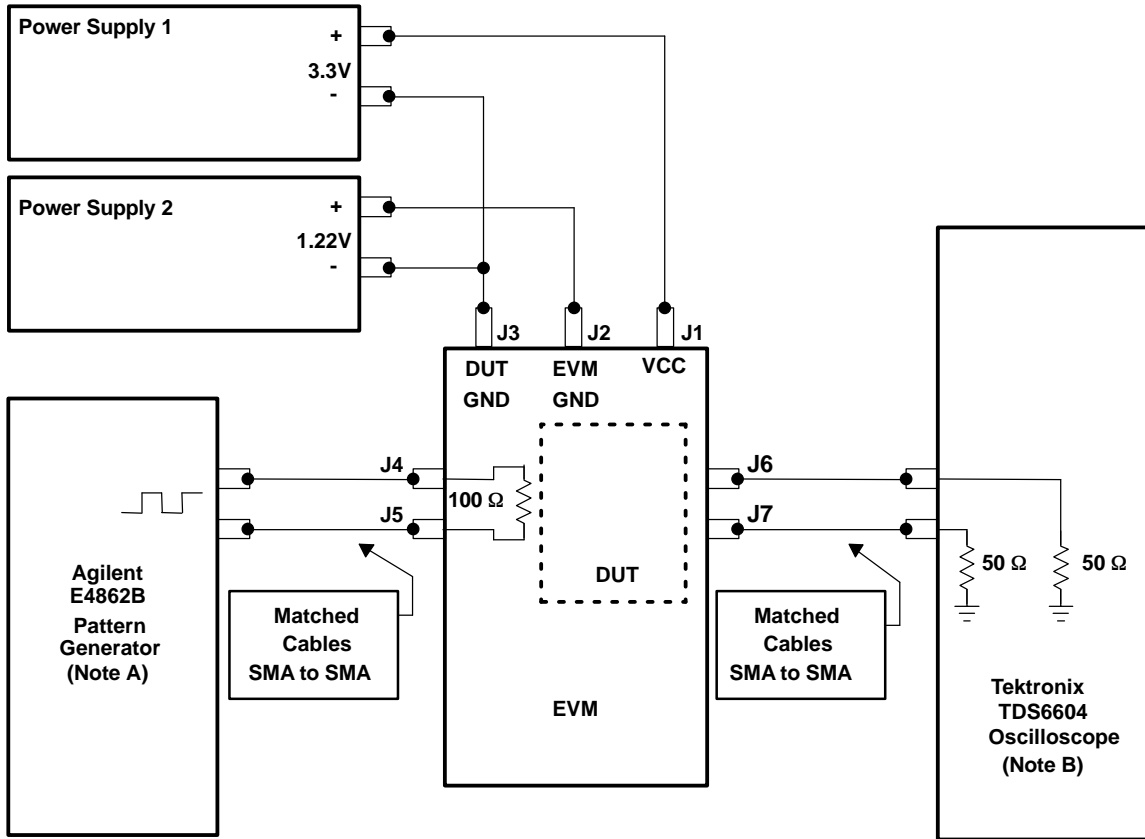


Figure 6. Driver Jitter Measurement Waveforms

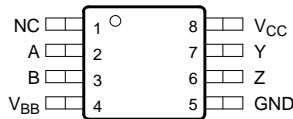


- A. Source jitter is subtracted from the measured values.
- B. TDS JIT3 jitter analysis software installed

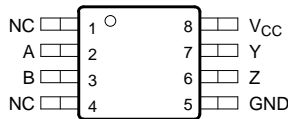
Figure 7. Jitter Setup Connections for SN65LVDS100 and SN65LVDS101

PIN ASSIGNMENTS

SN65LVDS100 and SN65LVDS101
D AND DGK PACKAGE
(TOP VIEW)



SN65LVDT100 and SN65LVDT101
D AND DGK PACKAGE
(TOP VIEW)



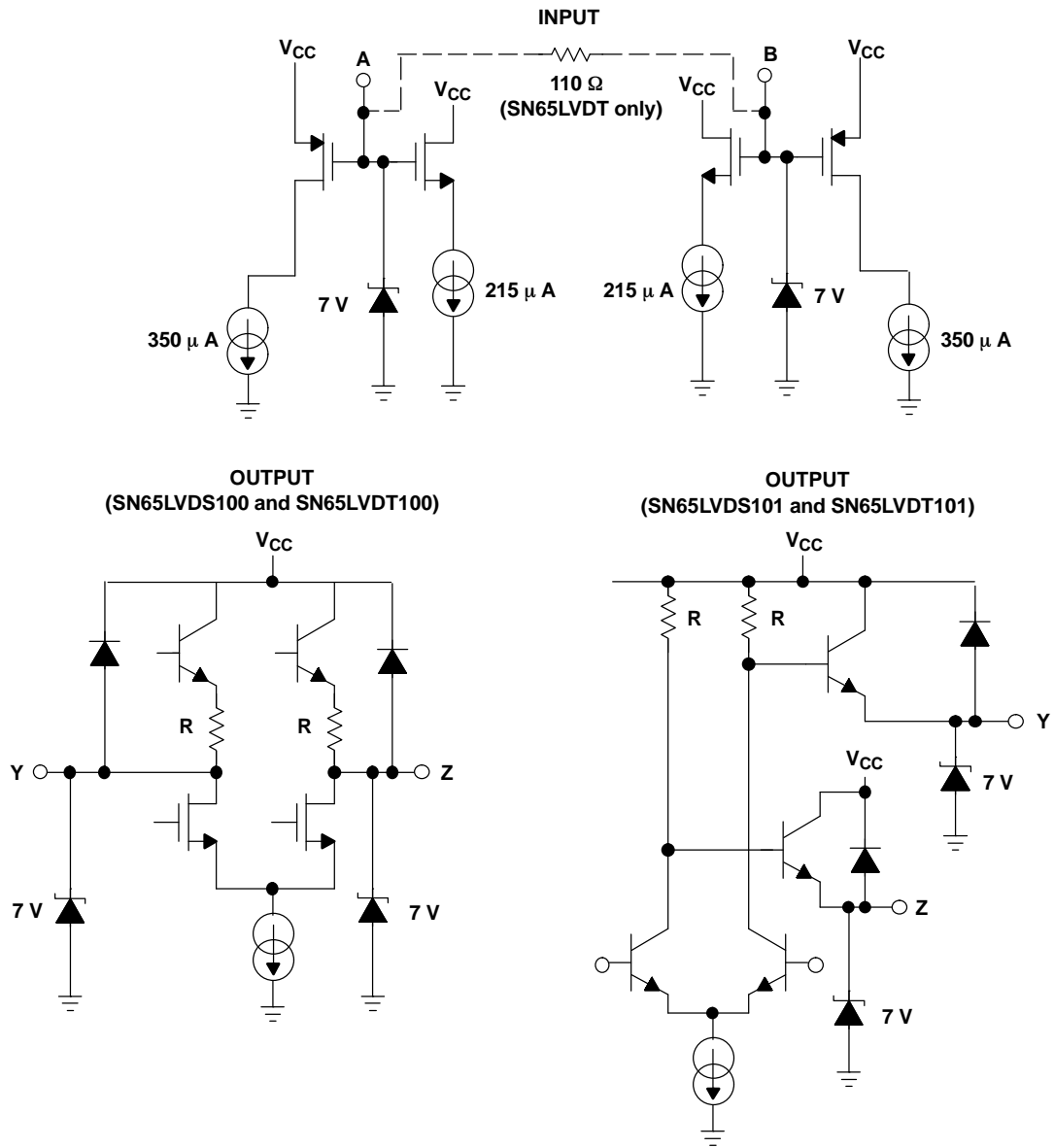
NC = Not Connected

FUNCTION TABLE

DIFFERENTIAL INPUT	OUTPUTS ⁽¹⁾	
$V_{ID} = V_A - V_B$	Y	Z
$V_{ID} \geq 100 \text{ mV}$	H	L
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$?	?
$V_{ID} \leq -100 \text{ mV}$	L	H
Open	?	?

(1) H = high level, L = low level, ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TYPICAL CHARACTERISTICS

SUPPLY CURRENT VS FREQUENCY

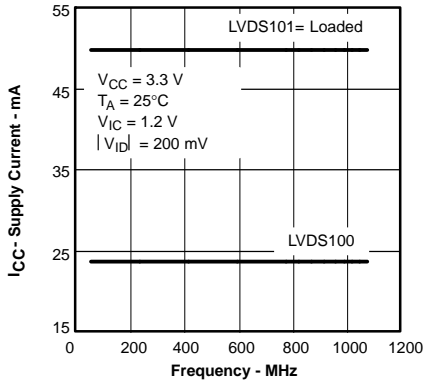


Figure 8.

SUPPLY CURRENT VS FREE-AIR TEMPERATURE

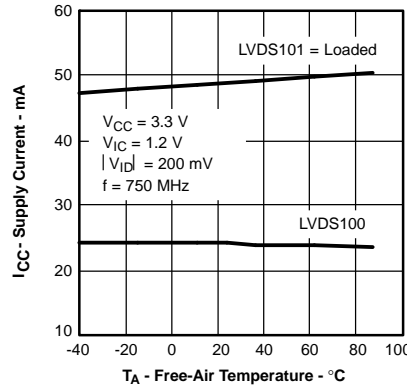


Figure 9.

DIFFERENTIAL OUTPUT VOLTAGE VS FREQUENCY

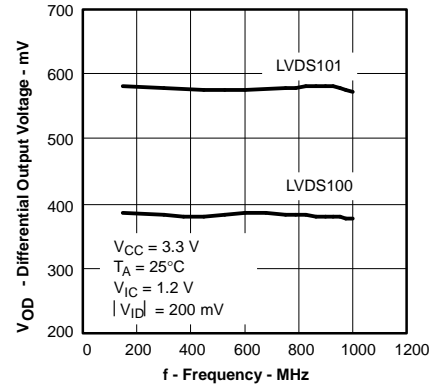


Figure 10.

SN65LVDS100 PROPAGATION DELAY TIME VS COMMON-MODE INPUT VOLTAGE

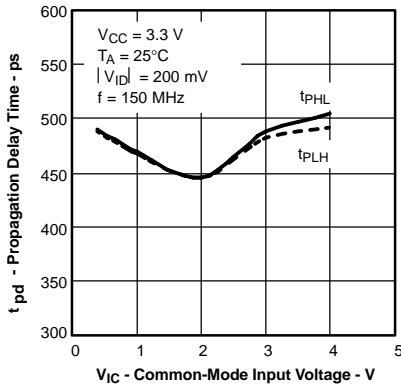


Figure 11.

SN65LVDS101 PROPAGATION DELAY TIME VS COMMON-MODE INPUT VOLTAGE

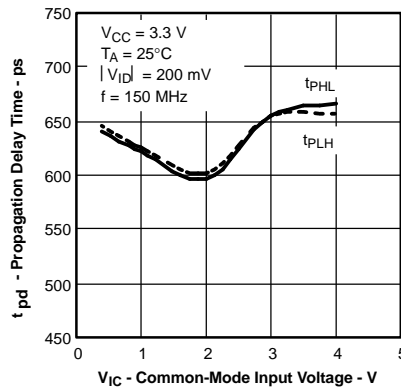


Figure 12.

SN65LVDS100 PROPAGATION DELAY TIME VS FREE-AIR TEMPERATURE

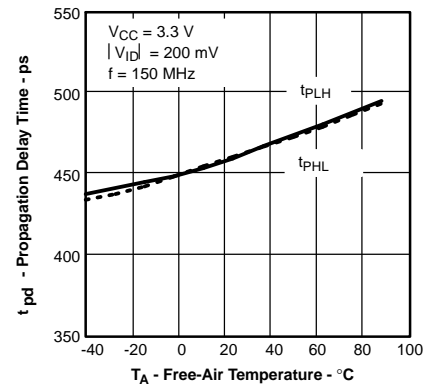


Figure 13.

SN65LVDS101 PROPAGATION DELAY TIME VS FREE-AIR TEMPERATURE

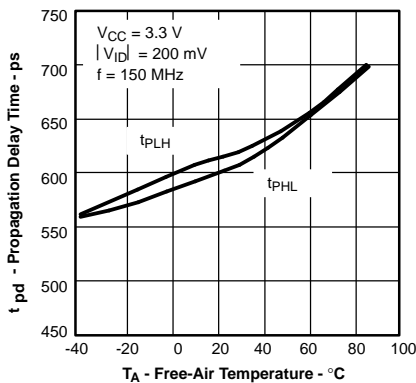


Figure 14.

SN65LVDS100 PEAK-TO-PEAK JITTER VS FREQUENCY

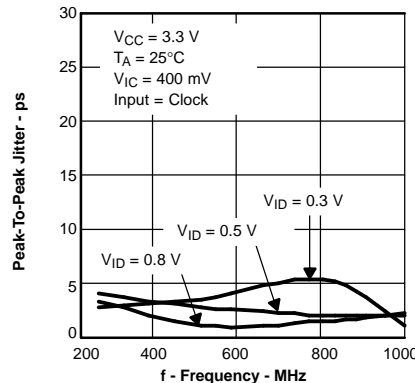


Figure 15.

SN65LVDS100 PEAK-TO-PEAK JITTER VS DATA RATE

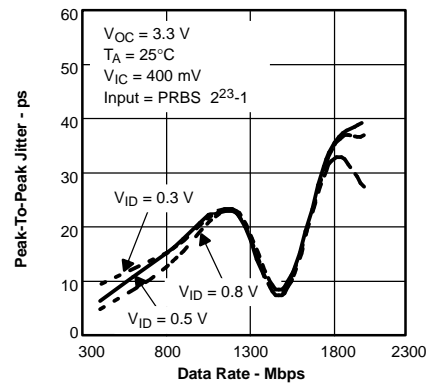


Figure 16.

TYPICAL CHARACTERISTICS (continued)

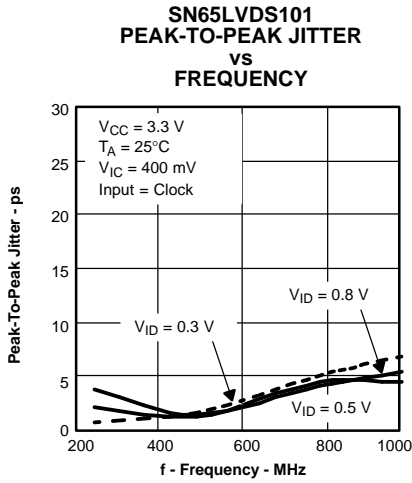


Figure 17.

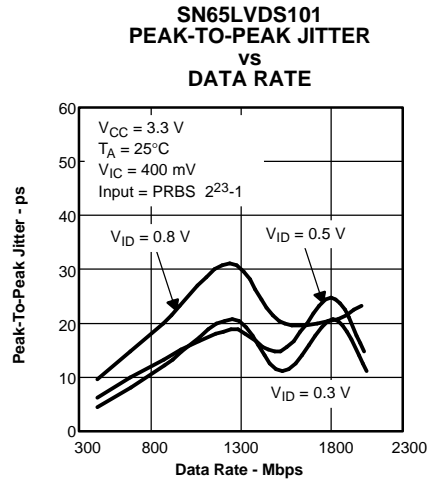


Figure 18.

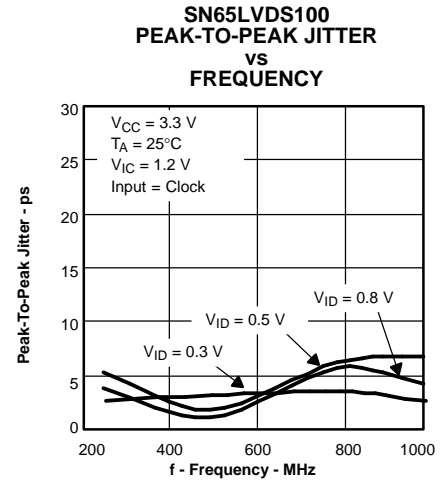


Figure 19.

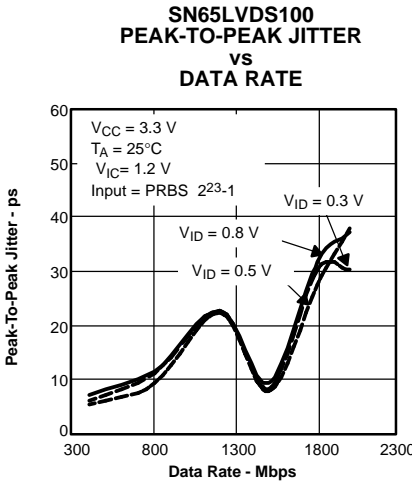


Figure 20.

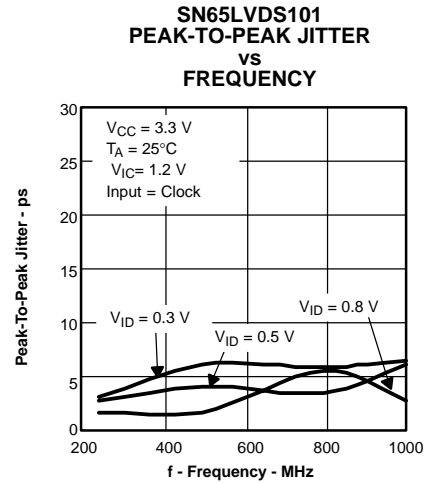


Figure 21.

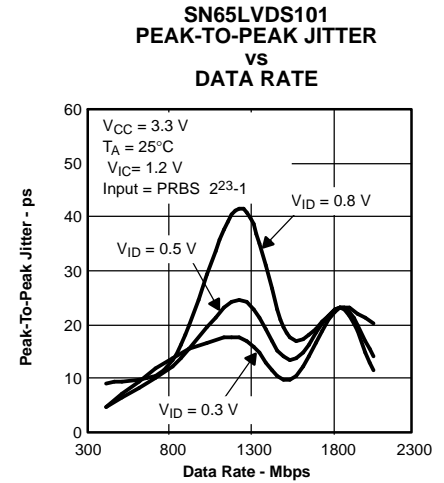


Figure 22.

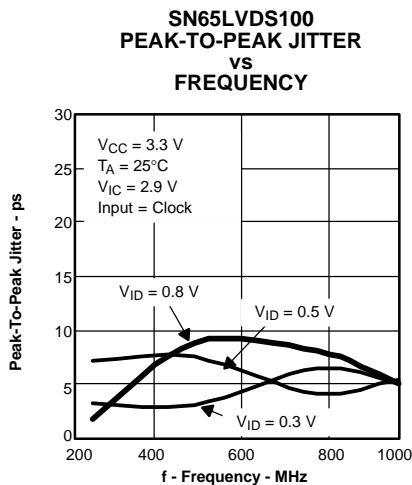


Figure 23.

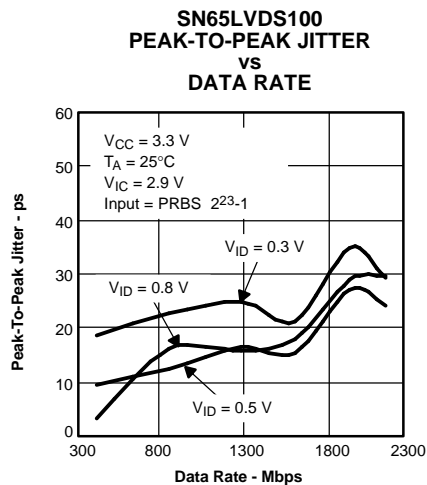


Figure 24.

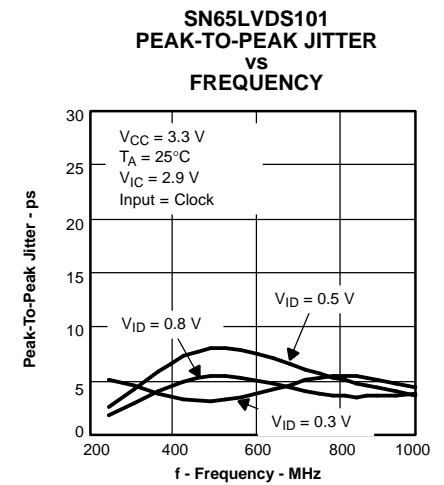


Figure 25.

TYPICAL CHARACTERISTICS (continued)

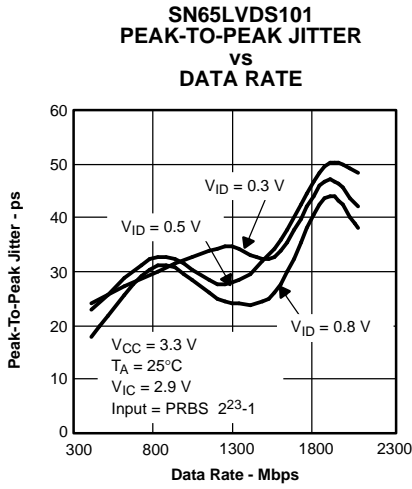


Figure 26.

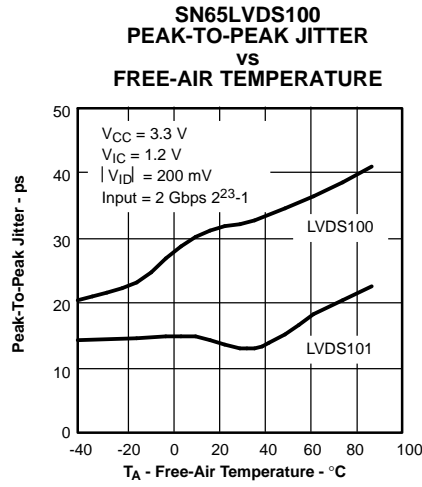


Figure 27.

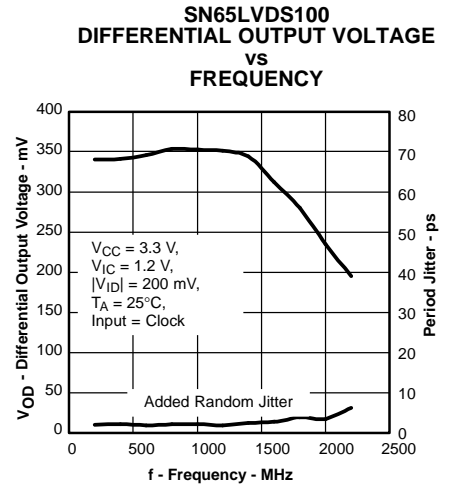


Figure 28.

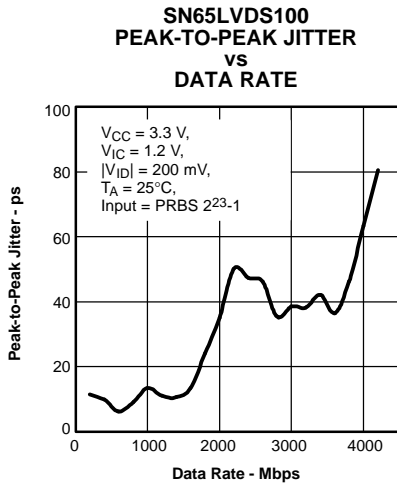


Figure 29.

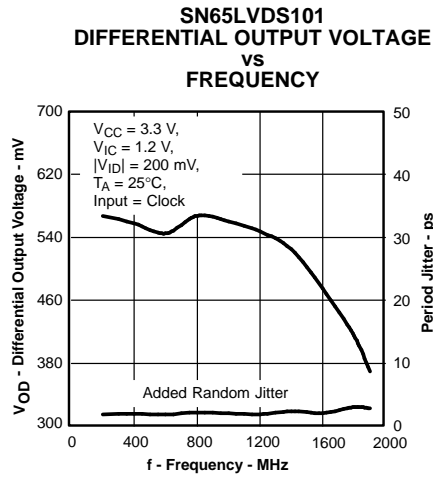


Figure 30.

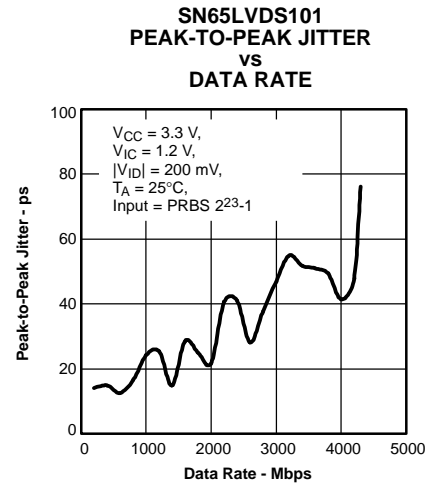
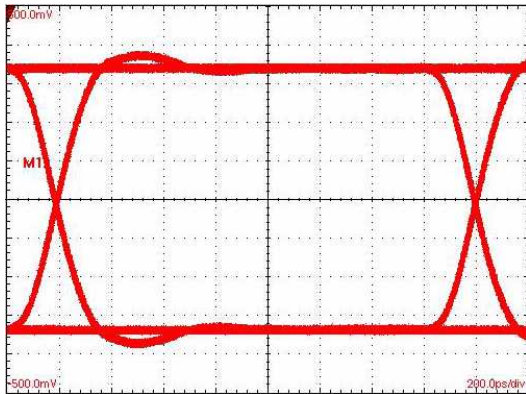


Figure 31.

TYPICAL CHARACTERISTICS (continued)

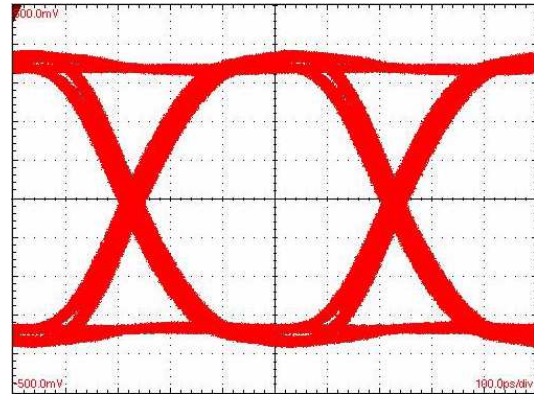
SN65LVDS100
622 Mbps, $2^{23}-1$ PRBS



Horizontal Scale= 200 ps/div
LVPECL-to-LVDS

Figure 32.

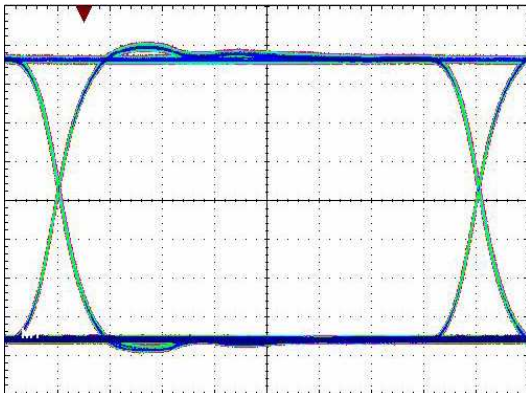
SN65LVDS100
2 Gbps, $2^{23}-1$ PRBS



Horizontal Scale= 100 ps/div
LVPECL-to-LVDS

Figure 33.

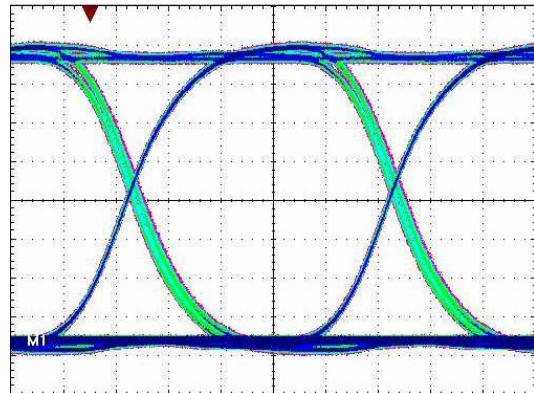
SN65LVDS101
622 Mbps, $2^{23}-1$ PRBS



Horizontal Scale= 200 ps/div
LVDS-to-LVPECL

Figure 34.

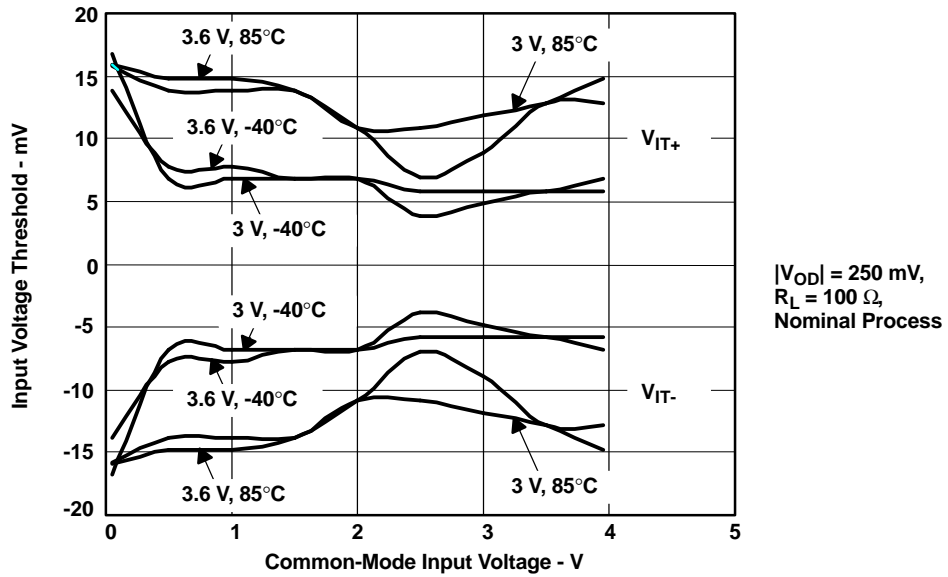
SN65LVDS101
2 Gbps, $2^{23}-1$ PRBS



Horizontal Scale= 100 ps/div
LVDS-to-LVPECL

Figure 35.

TYPICAL CHARACTERISTICS (continued)



NOTE: V_{IT} is a steady-state parameter. The switching time is influenced by the input overdrive above this steady-state threshold up to a differential input voltage magnitude of 100 mV.

Figure 36. SN65LVDS100 Simulated Input Voltage Threshold vs Common-Mode Input Voltage, Supply Voltage, and Temperature

APPLICATION INFORMATION

The SN65LVDS100, SN65LVDT100, SN65LVDS101, and SN65LVDT101 inputs will detect a 100-mV difference between any two signals between 0 V and 4 V. This range will allow receipt of many different single-ended and differential signals. Following are some of the more common connections.

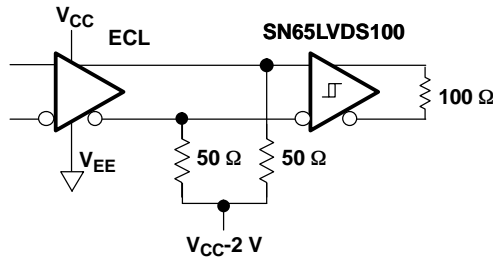


Figure 37. PECL-to-LVDS Translation

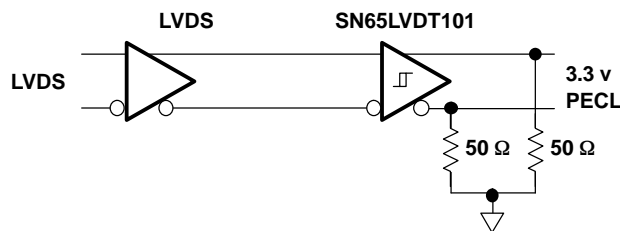


Figure 38. LVDS-to-3.3 V PECL Translation

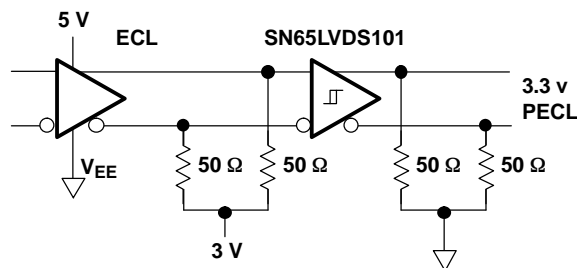


Figure 39. 5-V PECL to 3.3-V PECL Translation

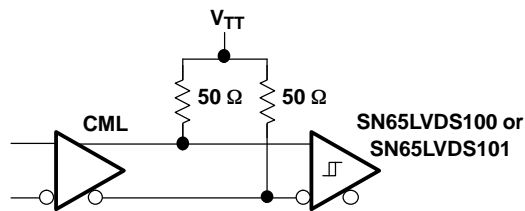


Figure 40. CML-to-LVDS or 3.3-V PECL Translation

APPLICATION INFORMATION (continued)

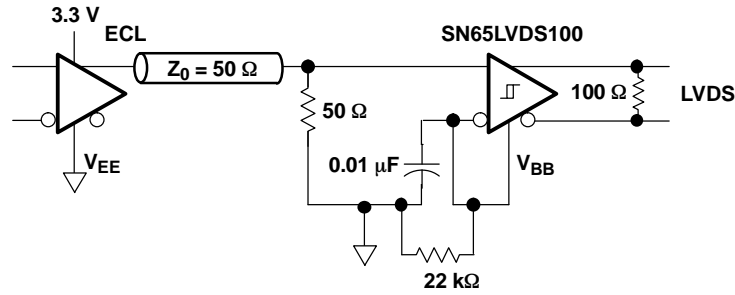


Figure 41. Single-Ended 3.3-V PECL-to-LVDS Translation

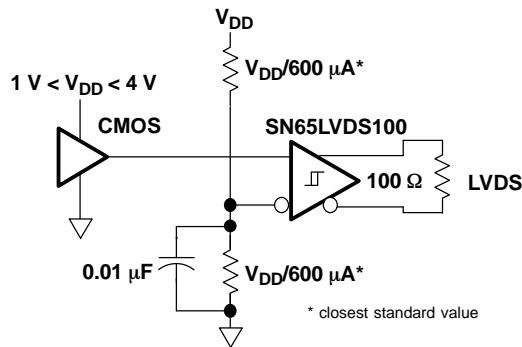


Figure 42. Single-Ended CMOS-to-LVDS Translation

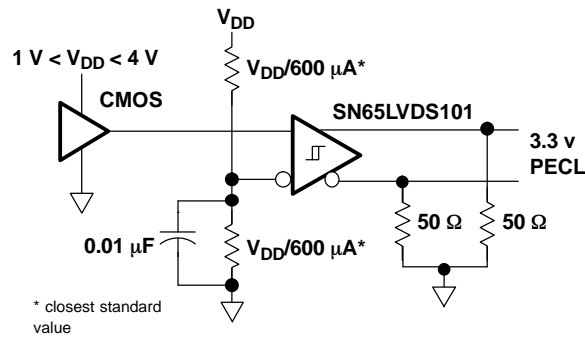


Figure 43. Single-Ended CMOS-to-3.3-V PECL Translation

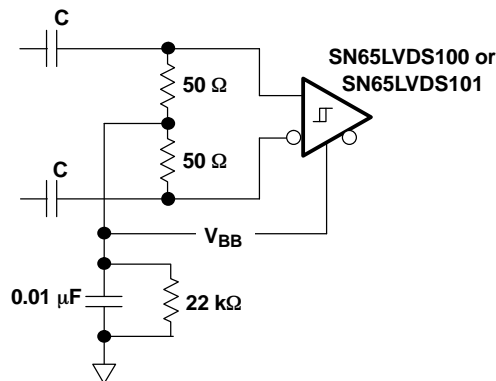


Figure 44. Receipt of AC-Coupled Signals

APPLICATION INFORMATION (continued)

FAILSAFE CONSIDERATIONS

Failsafe, in regard to a line receiver, usually means that the output goes to a defined logical state with no input signal. To keep added jitter to an absolute minimum, the SN65LVDS100 does not include this feature. It does exhibit 25 mV of input voltage hysteresis to prevent oscillation and keep the output in the last state prior to input-signal loss (assuming the differential noise in the system is less than the hysteresis).

Should failsafe be required, it may be added externally with a 1.6-k Ω pull-up resistor to the 3.3-V supply and a 1.6-k Ω pull-down resistor to ground as shown in Figure 45. The default output state is determined by which line is pulled up or down and is the user's choice. The location of the 1.6-k Ω resistors is not critical. However the 100- Ω resistor should be located at the end of the transmission line.

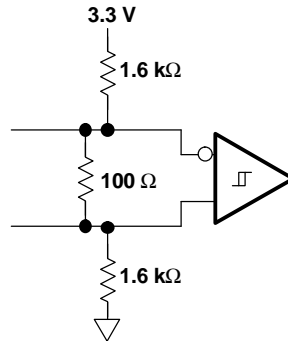


Figure 45. External Failsafe Circuit

Addition of this external failsafe will reduce the differential noise margin and add jitter to the output signal. The roughly 100-mV steady-state voltage generated across the 100- Ω resistor adds (or subtracts) from the signal generated by the upstream line driver. If the line driver's differential output is symmetrical about zero volts, then the input at the receiver will appear asymmetrical with the external failsafe. Perhaps more important, is the extra time it takes for the input signal to overcome the added failsafe offset voltage.

In Figure 46 and using an external failsafe, the high-level differential voltage at the input of the SN65LVDS100 reaches 340 mV and the low-level -400 mV indicating a 60-mV differential offset induced by the external failsafe circuitry. The figure also reveals that the lowest peak-to-peak time jitter does not occur at zero-volt differential (the nominal input threshold of the receiver) but at -60 mV, the failsafe offset.

The added jitter from external failsafe increases as the signal transition times are slowed by cable effects. When a ten-meter CAT-5 UTP cable is introduced between the driver and receiver, the zero-crossing peak-to-peak jitter at the receiver output adds 250 ps when the external failsafe is added with this specific test set up. If external failsafe is used in conjunction with the SN65LVDS100, the noise margin and jitter effects should be budgeted.

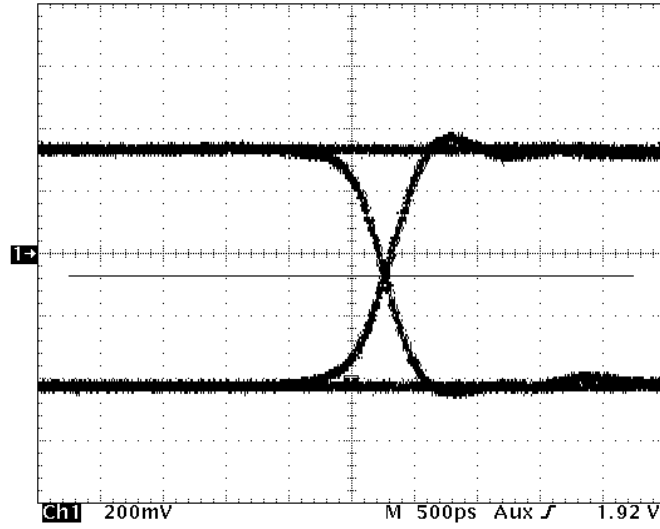


Figure 46. Receiver Input Eye Pattern With External Failsafe

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS100D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL100	Samples
SN65LVDS100DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL100	Samples
SN65LVDS100DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZK	Samples
SN65LVDS100DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZK	Samples
SN65LVDS100DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AZK	Samples
SN65LVDS100DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZK	Samples
SN65LVDS100DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL100	Samples
SN65LVDS100DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL100	Samples
SN65LVDS101D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL101	Samples
SN65LVDS101DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL101	Samples
SN65LVDS101DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZM	Samples
SN65LVDS101DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZM	Samples
SN65LVDS101DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZM	Samples
SN65LVDS101DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZM	Samples
SN65LVDS101DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL101	Samples
SN65LVDS101DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL101	Samples
SN65LVDT100D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE100	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDT100DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE100	Samples
SN65LVDT100DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZL	Samples
SN65LVDT100DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZL	Samples
SN65LVDT100DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZL	Samples
SN65LVDT100DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZL	Samples
SN65LVDT100DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE100	Samples
SN65LVDT100DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE100	Samples
SN65LVDT101D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE101	Samples
SN65LVDT101DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE101	Samples
SN65LVDT101DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BAF	Samples
SN65LVDT101DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BAF	Samples
SN65LVDT101DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BAF	Samples
SN65LVDT101DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BAF	Samples
SN65LVDT101DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE101	Samples
SN65LVDT101DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE101	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS100DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS100DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDS101DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS101DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDT100DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDT100DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDT101DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDT101DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS100DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65LVDS100DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65LVDS101DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65LVDS101DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65LVDT100DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65LVDT100DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65LVDT101DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65LVDT101DR	SOIC	D	8	2500	367.0	367.0	35.0

DGK (S-PDSO-G8)

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 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

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4040047-3/M 06/11

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