

## ISOLATED CAN TRANSCEIVER

### FEATURES

- 4000- $V_{PEAK}$  Isolation
- Failsafe Outputs
- Low Loop Delay: 150 ns Typical
- 50 kV/ $\mu$ s Typical Transient Immunity
- Meets or Exceeds ISO 11898 requirements
- Bus-Fault Protection of  $-27$  V to 40 V
- Dominant Time-Out Function
- UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2), IEC 61010-1, IEC 60950-1 and CSA Approval Pending
- 3.3-V Inputs are 5-V Tolerant
- Typical 25-Year Life at Rated Working Voltage (see Application Report [SLLA197](#) and [Figure 15](#))

### APPLICATIONS

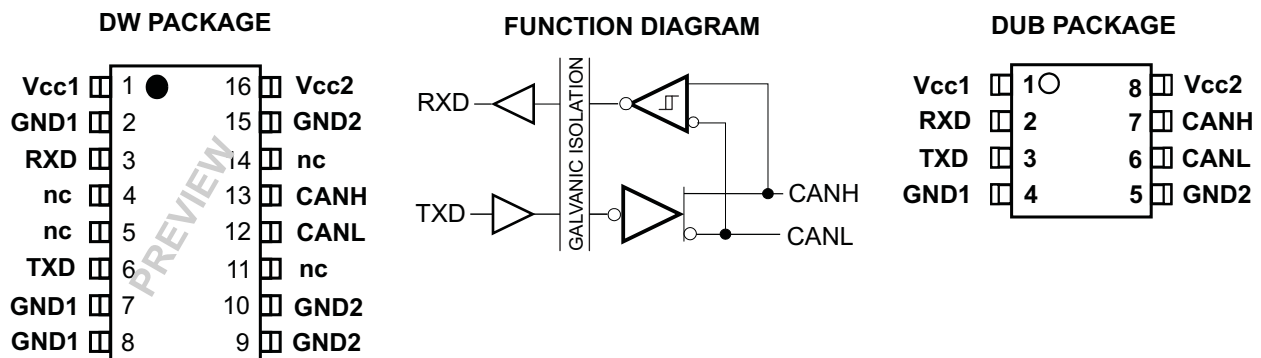
- CAN Data Buses
  - DeviceNet Data Buses
  - CANopen Data Buses
  - CANKingdom Data Buses
- Medical Scanning and Imaging
- Security Systems
- Telecom Base Station Status and Control
- HVAC
- Building Automation

### DESCRIPTION

The ISO1050 is a galvanically isolated CAN transceiver that meets or exceeds the specifications of the ISO 11898 standard. The device has the logic input and output buffers separated by a silicon oxide ( $\text{SiO}_2$ ) insulation barrier that provides galvanic isolation of up to 4000  $V_{PEAK}$ . Used in conjunction with isolated power supplies, the device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

As a CAN transceiver, the device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps). Designed for operation in especially harsh environments, the device features cross-wire, overvoltage and loss of ground protection from  $-27$  V to 40 V and overtemperature shut-down, as well as a  $-12$  V to 12 V common-mode range.

The ISO1050 is characterized for operation over the ambient temperature range of  $-55^\circ\text{C}$  to  $105^\circ\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1) (2)</sup>

				VALUE / UNIT
$V_{CC1}, V_{CC2}$	Supply voltage <sup>(3)</sup>			–0.5 V to 6 V
$V_I$	Voltage input (TXD)			–0.5 V to 6 V
$V_{CANH}$ or $V_{CANL}$	Voltage range at any bus terminal (CANH, CANL)			–27 V to 40 V
$I_O$	Receiver output current			±15 mA
ESD	Human Body Model	JEDEC Standard 22, Method A114-C.01	Bus pins and GND2 <sup>(4)</sup>	±4 kV
			All pins	±4 kV
	Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1.5 kV
	Machine Model	ANSI/ESDS5.2-1996	All pins	±200 V
$T_J$	Junction temperature			–55°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This isolator is suitable for basic isolation within the safety limiting data. Maintenance of the safety data must be ensured by means of protective circuitry.
- (3) All input and output logic voltage values are measured with respect to the GND1 logic side ground. Differential bus-side voltages are measured to the respective bus-side GND2 ground terminal.
- (4) Tested while connected between  $V_{CC2}$  and GND2.

## RECOMMENDED OPERATING CONDITIONS

				MIN	NOM	MAX	UNIT
$V_{CC1}$	Supply voltage, controller side			3		5.5	V
$V_{CC2}$	Supply voltage, bus side			4.75	5	5.25	V
$V_I$ or $V_{IC}$	Voltage at bus pins (separately or common mode)			–12 <sup>(1)</sup>		12	V
$V_{IH}$	High-level input voltage	TXD		2		5.25	V
$V_{IL}$	Low-level input voltage	TXD		0		0.8	V
$V_{ID}$	Differential input voltage			–7		7	V
$I_{OH}$	High-level output current	Driver		–70			mA
		Receiver		–4			
$I_{OL}$	Low-level output current	Driver				70	mA
		Receiver				4	
$T_J$	Junction temperature (see THERMAL CHARACTERISTICS)			–55		125	°C

- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## SUPPLY CURRENT

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$I_{CC1}$	$V_{CC1}$ Supply current	$V_I = 0$ V or $V_{CC1}, V_{CC1} = 3.3$ V			1	2	mA
		$V_I = 0$ V or $V_{CC1}, V_{CC1} = 5$ V			2	3	
$I_{CC2}$	$V_{CC2}$ Supply current	Dominant	$V_I = 0$ V, 60-Ω Load		52	73	mA
		Recessive	$V_I = V_{CC1}$		8	12	

- (1) All typical values are at 25°C with  $V_{CC1} = V_{CC2} = 5$  V.

## DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{loop1}$	Total loop delay, driver input to receiver output, Recessive to Dominant	See <a href="#">Figure 9</a>	112	150	210	ns
$t_{loop2}$	Total loop delay, driver input to receiver output, Dominant to Recessive	See <a href="#">Figure 9</a>	112	150	210	ns

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	See <a href="#">Figure 1</a> and <a href="#">Figure 2</a> , $V_I = 0\text{ V}$ , $R_L = 60\Omega$	2.9	3.5	4.5	V
		CANL		0.8	1.2	1.5	
$V_{O(R)}$	Bus output voltage (Recessive)	See <a href="#">Figure 1</a> and <a href="#">Figure 2</a> , $V_I = 2\text{ V}$ , $R_L = 60\Omega$	2	2.3	3	V	
$V_{OD(D)}$	Differential output voltage (Dominant)	See <a href="#">Figure 1</a> , <a href="#">Figure 2</a> and <a href="#">Figure 3</a> , $V_I = 0\text{ V}$ , $R_L = 60\Omega$	1.5		3	V	
		See <a href="#">Figure 1</a> , <a href="#">Figure 2</a> , and <a href="#">Figure 3</a> $V_I = 0\text{ V}$ , $R_L = 45\Omega$ , $V_{CC} > 4.8\text{ V}$	1.4		3		
$V_{OD(R)}$	Differential output voltage (Recessive)	See <a href="#">Figure 1</a> and <a href="#">Figure 2</a> , $V_I = 3\text{ V}$ , $R_L = 60\Omega$	-0.12		0.012	V	
		$V_I = 3\text{ V}$ , No Load	-0.5		0.05		
$V_{OC(D)}$	Common-mode output voltage (Dominant)	See <a href="#">Figure 8</a>	2	2.3	3	V	
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage			0.3			
$I_{IH}$	High-level input current, TXD input	$V_I$ at 2 V			5	$\mu\text{A}$	
$I_{IL}$	Low-level input current, TXD input	$V_I$ at 0.8 V	-5			$\mu\text{A}$	
$I_{O(off)}$	Power-off TXD leakage current	$V_{CC1}$ , $V_{CC2}$ at 0 V, TXD at 5 V			10	$\mu\text{A}$	
$I_{OS(ss)}$	Short-circuit steady-state output current	See <a href="#">Figure 11</a> , $V_{CANH} = -12\text{ V}$ , CANL Open	-105	-72		mA	
		See <a href="#">Figure 11</a> , $V_{CANH} = 12\text{ V}$ , CANL Open		0.36	1		
		See <a href="#">Figure 11</a> , $V_{CANL} = -12\text{ V}$ , CANH Open	-1	-0.5			
		See <a href="#">Figure 11</a> , $V_{CANL} = 12\text{ V}$ , CANH Open		71	105		
$C_O$	Output capacitance	See receiver input capacitance					
CMTI	Common-mode transient immunity	See <a href="#">Figure 13</a> , $V_I = V_{CC}$ or 0 V	25	50		kV/ $\mu\text{s}$	

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, recessive-to-dominant output	See <a href="#">Figure 4</a>	31	74	110	ns
$t_{PHL}$	Propagation delay time, dominant-to-recessive output		25	44	75	
$t_r$	Differential output signal rise time			20	50	
$t_f$	Differential output signal fall time			20	50	
$t_{dom}$	Dominant time-out		$\downarrow C_L = 100\text{ pF}$ , See <a href="#">Figure 10</a>	300	450	

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IT+</sub>	Positive-going bus input threshold voltage	See <a href="#">Table 1</a>		750	900	mV
V <sub>IT-</sub>	Negative-going bus input threshold voltage		500	650	mV	
V <sub>hys</sub>	Hysteresis voltage (V <sub>IT+</sub> – V <sub>IT-</sub> )		150	mV		
V <sub>OH</sub>	High-level output voltage with V <sub>CC</sub> = 5V	I <sub>OH</sub> = –4 mA, See <a href="#">Figure 6</a>	V <sub>CC</sub> – 0.8	4.6		V
		I <sub>OH</sub> = –20 μA, See <a href="#">Figure 6</a>	V <sub>CC</sub> – 0.1	5		
V <sub>OH</sub>	High-level output voltage with V <sub>CC1</sub> = 3.3V	I <sub>OL</sub> = 4 mA, See <a href="#">Figure 6</a>	V <sub>CC</sub> – 0.8	3.1		V
		I <sub>OL</sub> = 20 μA, See <a href="#">Figure 6</a>	V <sub>CC</sub> – 0.1	3.3		
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA, See <a href="#">Figure 6</a>		0.2	0.4	V
		I <sub>OL</sub> = 20 μA, See <a href="#">Figure 6</a>		0	0.1	
C <sub>I</sub>	Input capacitance to ground, (CANH or CANL)	TXD at 3 V, V <sub>I</sub> = 0.4 sin (4E6πt) + 2.5V		6		pF
C <sub>ID</sub>	Differential input capacitance	TXD at 3 V, V <sub>I</sub> = 0.4 sin (4E6πt)		3		pF
R <sub>ID</sub>	Differential input resistance	TXD at 3 V	30		80	kΩ
R <sub>IN</sub>	Input resistance (CANH or CANL)	TXD at 3 V	15	30	40	kΩ
R <sub>I(m)</sub>	Input resistance matching (1 – [R <sub>IN (CANH)</sub> / R <sub>IN (CANL)</sub> ]) × 100%	V <sub>CANH</sub> = V <sub>CANL</sub>	–3%	0%	3%	
CMTI	Common-mode transient immunity	V <sub>I</sub> = V <sub>CC</sub> or 0 V, See <a href="#">Figure 13</a>	25	50		kV/μs

(1) All typical values are at 25°C with V<sub>CC1</sub> = V<sub>CC2</sub> = 5V.

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	TXD at 3 V, See <a href="#">Figure 6</a>	66	90	130	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output		51	80	105	
t <sub>r</sub>	Output signal rise time		3	6		
t <sub>f</sub>	Output signal fall time		3	6		
t <sub>fs</sub>	Failsafe output delay time from bus-side power loss	V <sub>CC1</sub> at 5 V, See <a href="#">Figure 12</a>		6		μs

PARAMETER MEASUREMENT INFORMATION

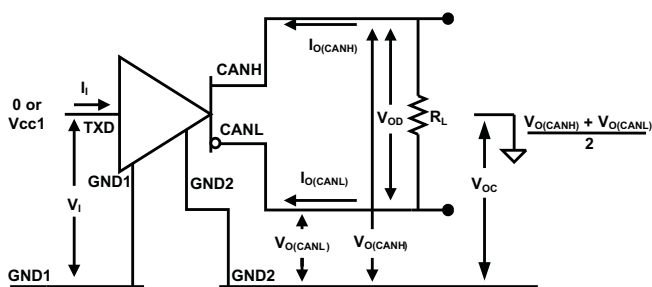


Figure 1. Driver Voltage, Current and Test Definitions

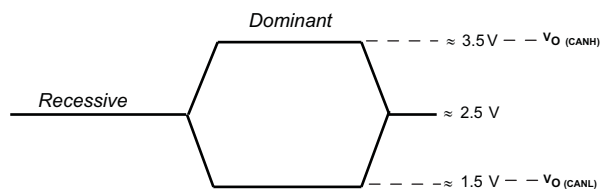


Figure 2. Bus Logic State Voltage Definitions

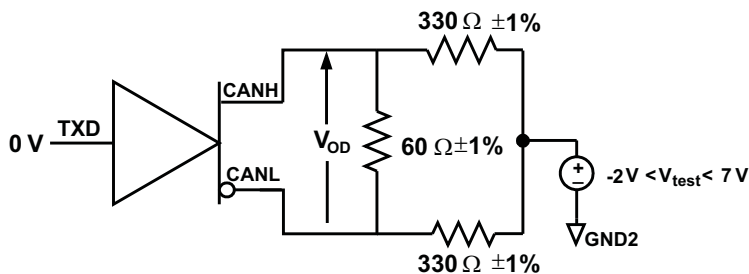
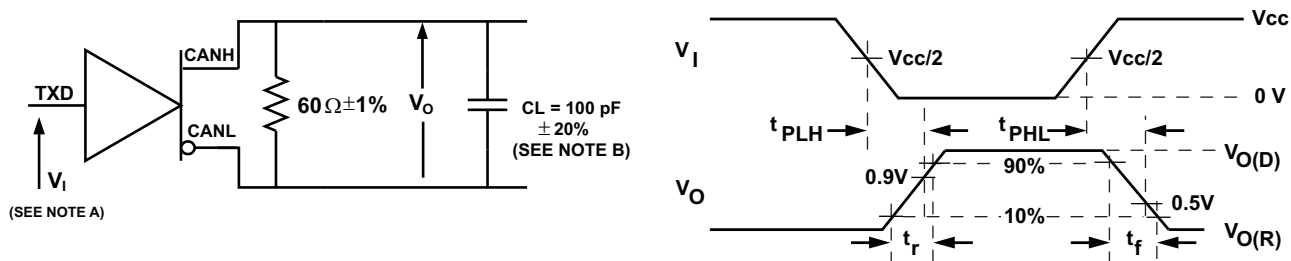


Figure 3. Driver  $V_{OD}$  with Common-mode Loading Test Circuit



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  125 kHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O = 50\Omega$ .
- B.  $C_L$  includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 4. Driver Test Circuit and Voltage Waveforms

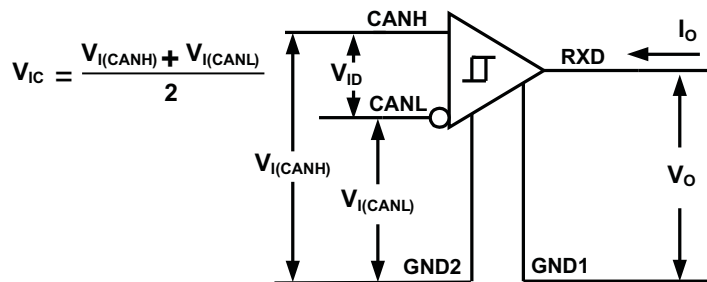
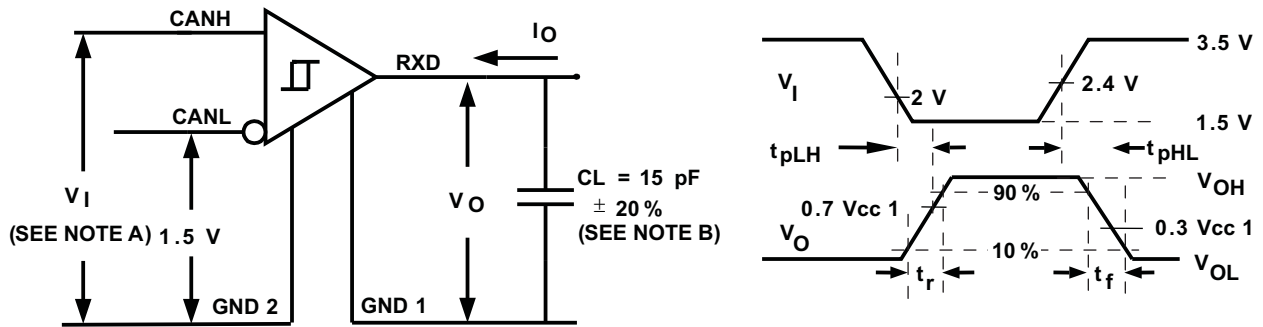


Figure 5. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

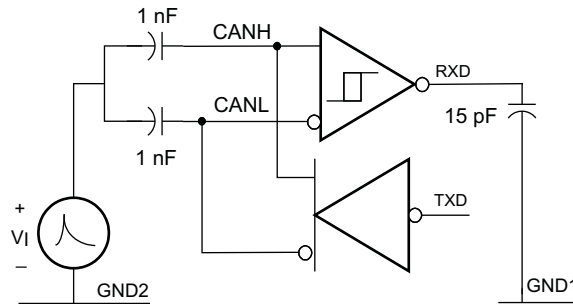


- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50\Omega$ .
- B.  $C_L$  includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 6. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
$V_{CANH}$	$V_{CANL}$	$ V_{ID} $	R	
-11.1 V	-12 V	900 mV	L	$V_{OL}$
12 V	11.1 V	900 mV	L	
-6 V	-12 V	6 V	L	
12 V	6 V	6 V	L	
-11.5 V	-12 V	500 mV	H	$V_{OH}$
12 V	11.5 V	500 mV	H	
-12 V	-6 V	-6 V	H	
6 V	12 V	-6 V	H	
Open	Open	X	H	



The waveforms of the applied transients are in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, and 3b.

Figure 7. Transient Over-Voltage Test Circuit

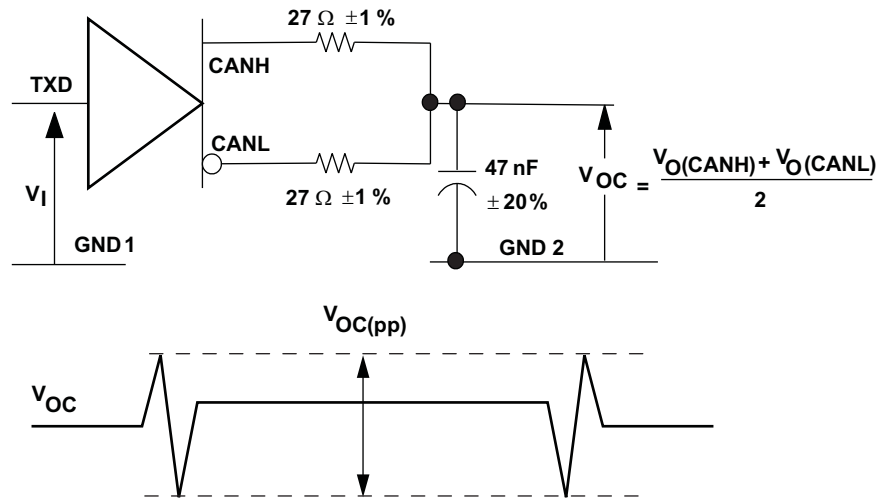


Figure 8. Peak-to-Peak Output Voltage Test Circuit and Waveform

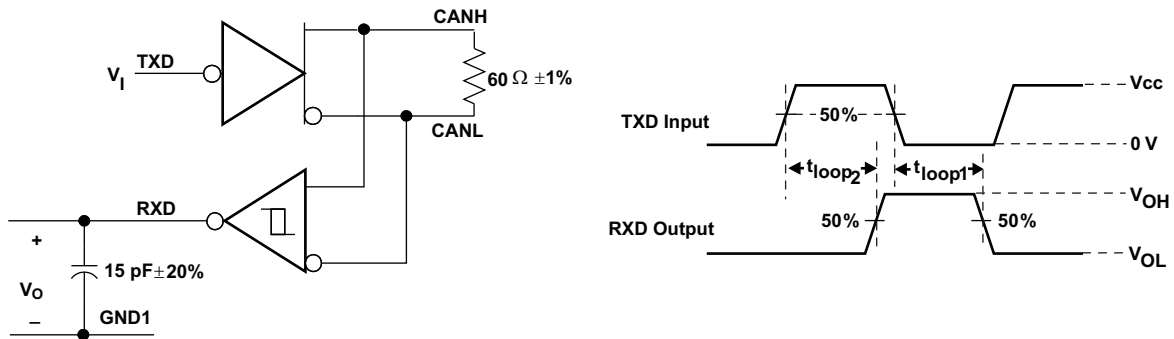
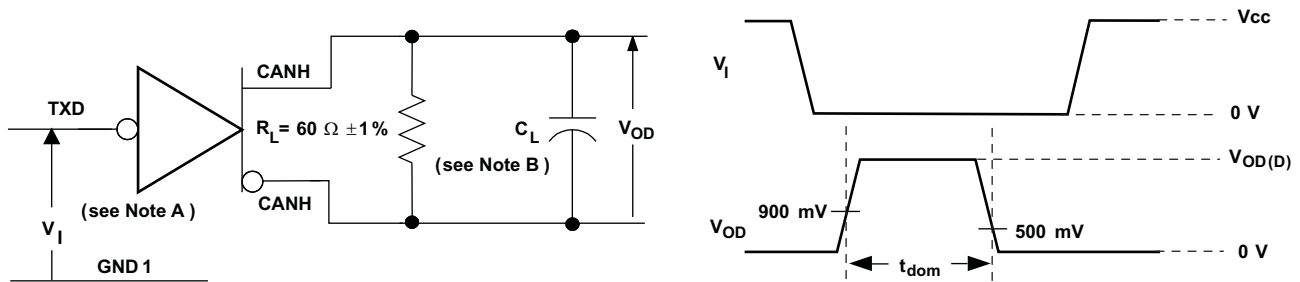


Figure 9.  $t_{LOOP}$  Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  125 kHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_0 = 50\Omega$ .
- B.  $C_L$  includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 10. Dominant Timeout Test Circuit and Voltage Waveforms

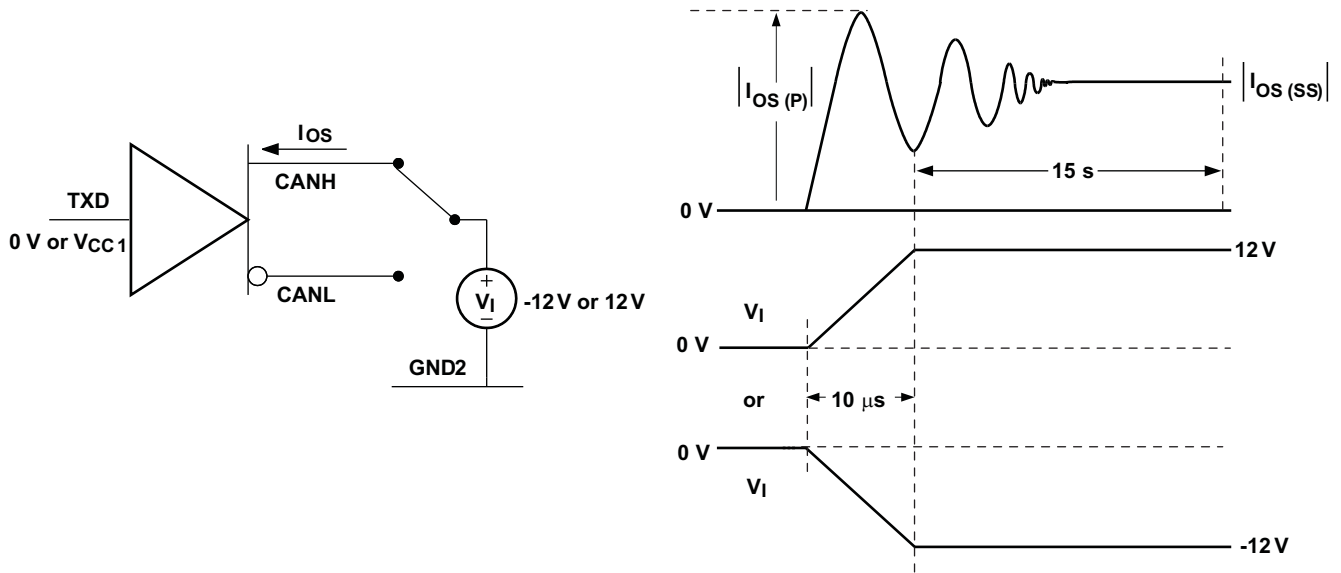


Figure 11. Driver Short-Circuit Current Test Circuit and Waveforms

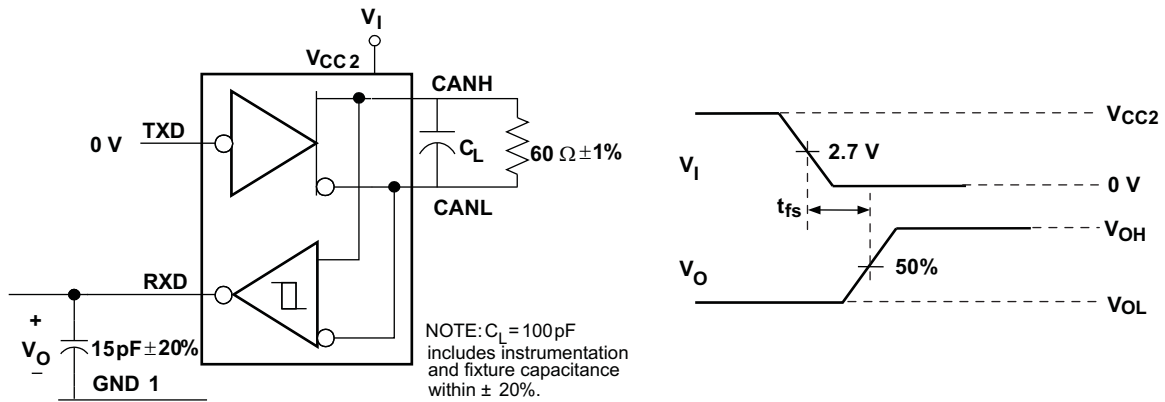


Figure 12. Failsafe Delay Time Test Circuit and Voltage Waveforms



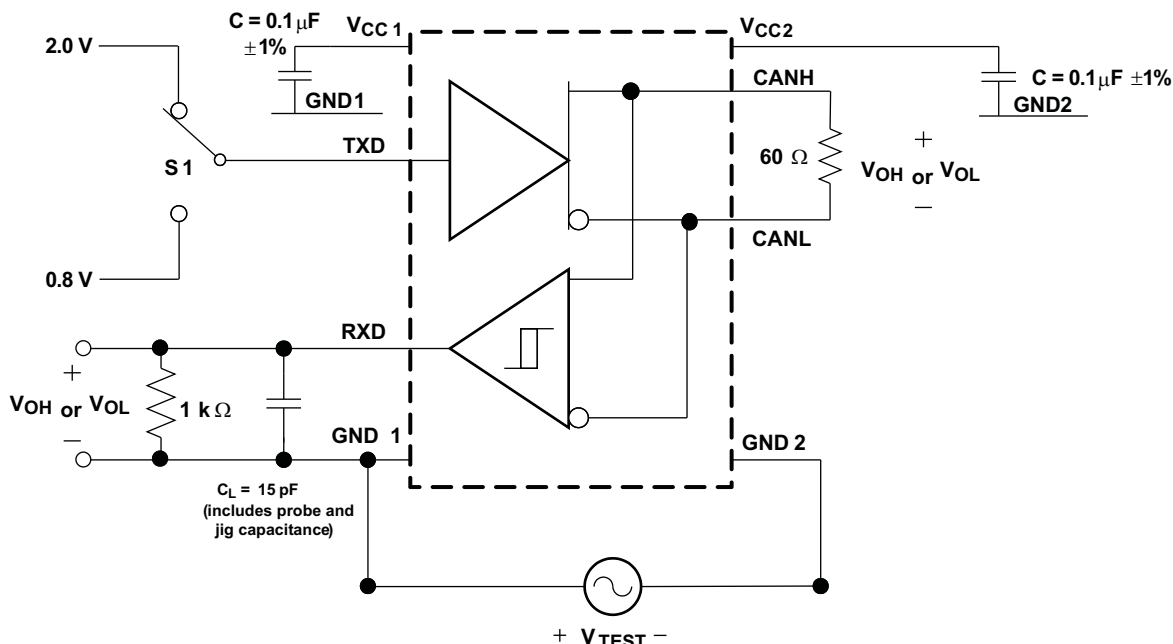


Figure 13. Common-Mode Transient Immunity Test Circuit

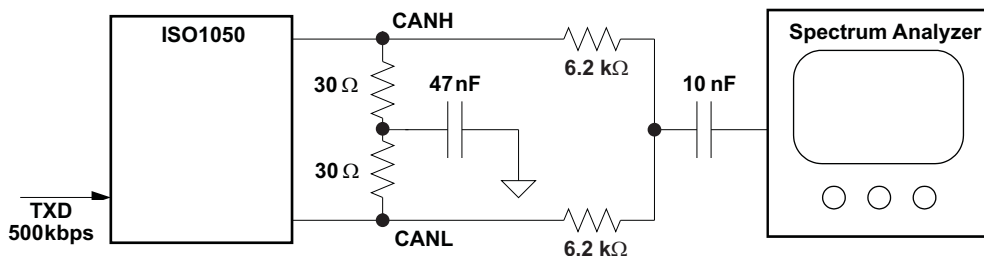


Figure 14. Electromagnetic Emissions Measurement Setup

DEVICE INFORMATION

FUNCTION TABLE<sup>(1)</sup>

DRIVER				RECEIVER		
INPUTS	OUTPUTS		BUS STATE	DIFFERENTIAL INPUTS $V_{ID} = \text{CANH} - \text{CANL}$	OUTPUT RXD	BUS STATE
TXD	CANH	CANL				
L <sup>(2)</sup>	H	L	DOMINANT	$V_{ID} \geq 0.9 \text{ V}$	L	DOMINANT
H	Z	Z	RECESSIVE	$0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$	?	?
Open	Z	Z	RECESSIVE	$V_{ID} \leq 0.5 \text{ V}$	H	RECESSIVE
X	Z	Z	RECESSIVE	Open	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance  
 (2) Logic low pulses to prevent dominant time-out.

## DEVICE INFORMATION

### ISOLATOR CHARACTERISTICS <sup>(1)</sup> <sup>(2)</sup>

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	6.1			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	6.8			mm
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	8.10			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R <sub>IO</sub>	Isolation resistance	Input to output, V <sub>IO</sub> = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T <sub>amb</sub> < 100°C		>10 <sup>12</sup>		Ω
		Input to output V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>amb</sub> ≤ T <sub>amb max</sub>		>10 <sup>11</sup>		Ω
C <sub>IO</sub>	Barrier capacitance	V <sub>I</sub> = 0.4 sin (4E6πt)		1.9		pF
C <sub>I</sub>	Input capacitance to ground	V <sub>I</sub> = 0.4 sin (4E6πt)		1.3		pF

- Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.
- Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

### IEC SAFETY LIMITING VALUES

safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	SOIC-8			124	mA
					190	
T <sub>S</sub>	Maximum case temperature	SOIC-8			150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assured junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

### REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program <sup>(1)</sup>
File Number: pending	File Number: pending	File Number: pending

- Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

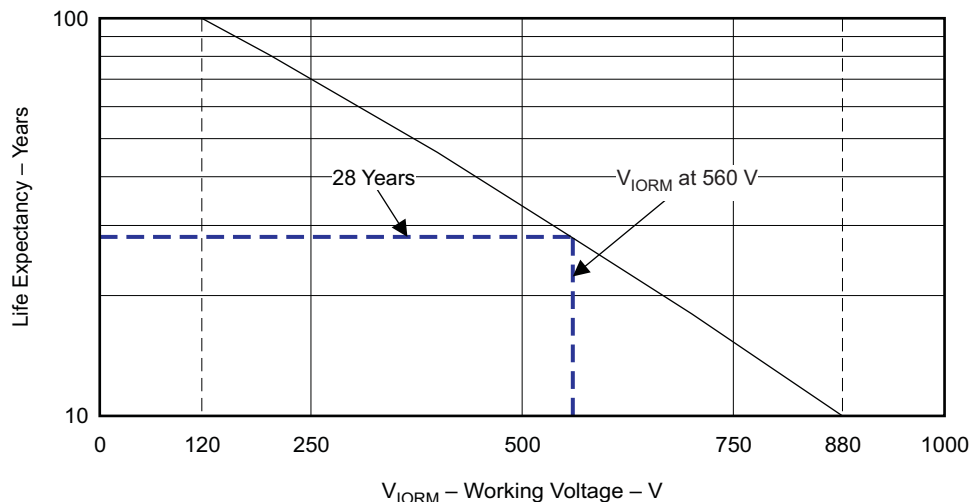
### THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\theta_{JA}$	Junction-to-air	Low-K Thermal Resistance <sup>(1)</sup>		120		°C/W
		High-K Thermal Resistance		73.3		°C/W
$\theta_{JB}$	Junction-to-board thermal resistance	Low-K Thermal Resistance		10.2		°C/W
$\theta_{JC}$	Junction-to-case thermal resistance	Low-K Thermal Resistance		14.5		°C/W
$P_D$	Device power dissipation	$V_{CC1}=5.5V$ , $V_{CC2}=5.25V$ , $T_A=105^\circ C$ , $R_L=60\Omega$ , TXD input is a 500kHz 50% duty-cycle square wave			200	mW
$T_{j\text{ shutdown}}$	Thermal shutdown temperature <sup>(2)</sup>			190		°C

- (1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.
- (2) Extended operation in thermal shutdown may affect device reliability.

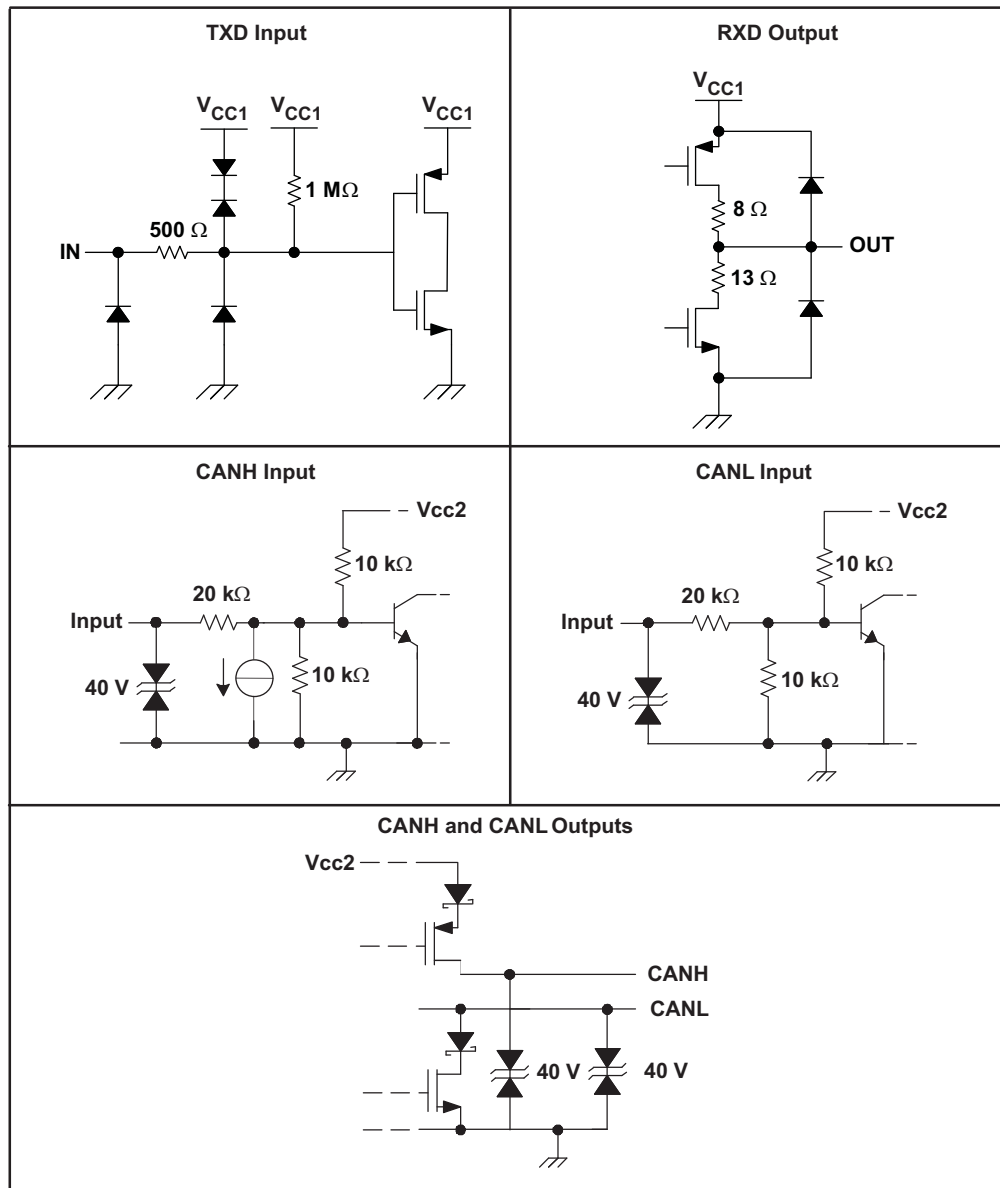
### LIFE EXPECTANCY vs WORKING VOLTAGE



G001

**Figure 15. Life Expectancy vs Working Voltage**

EQUIVALENT I/O SCHEMATICS



TYPICAL CHARACTERISTICS

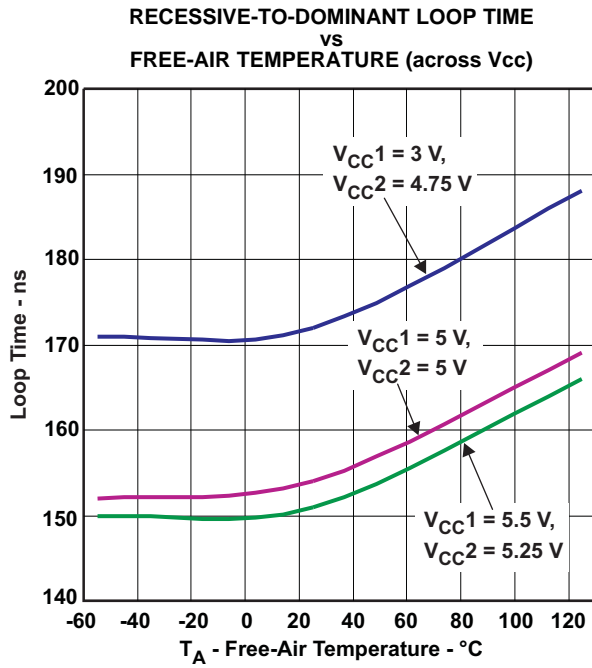


Figure 16.

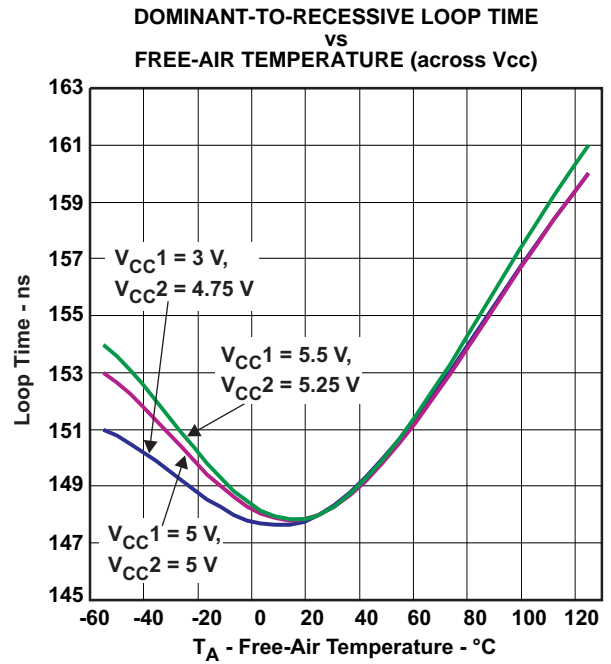


Figure 17.

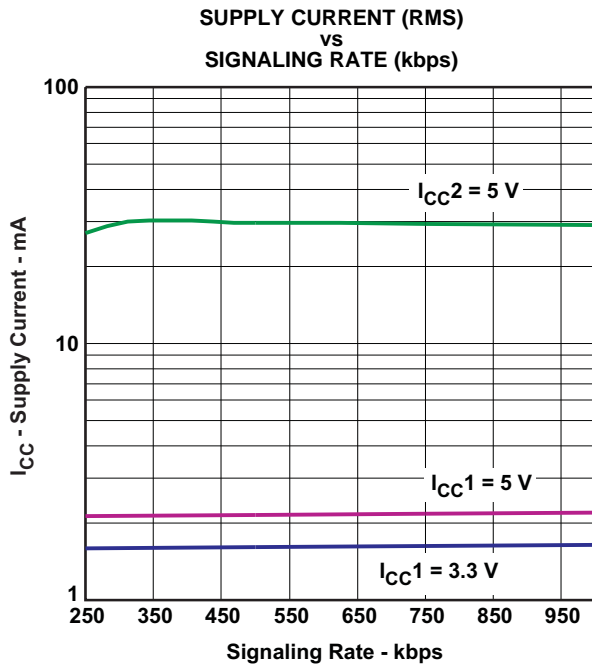


Figure 18.

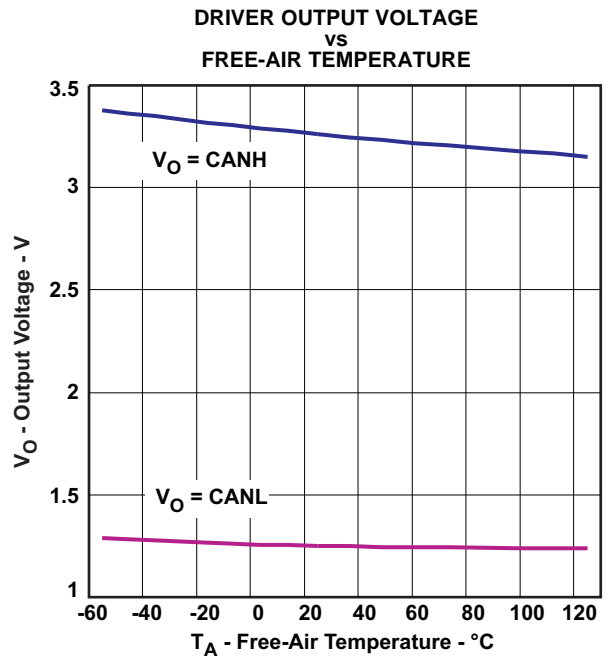


Figure 19.

TYPICAL CHARACTERISTICS (continued)

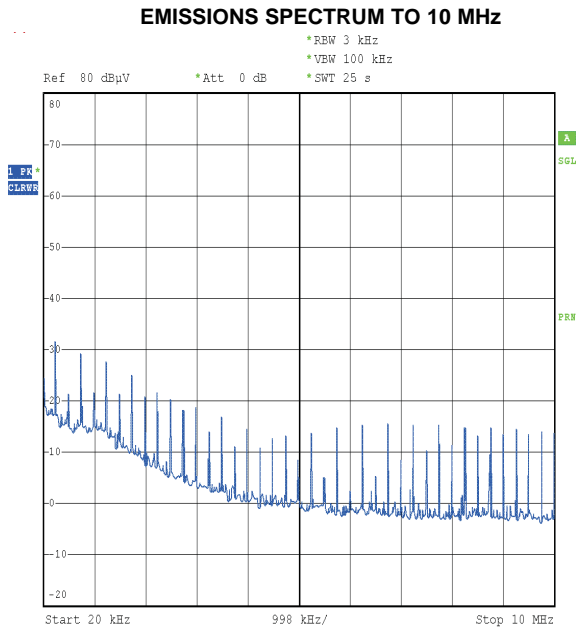


Figure 20.

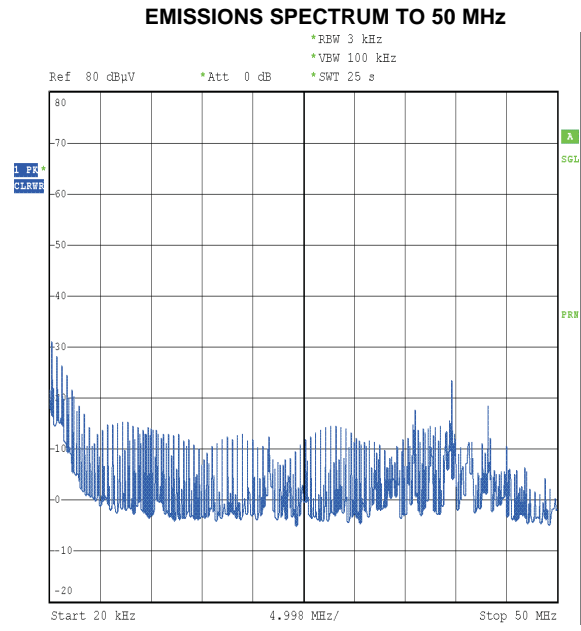


Figure 21.

## APPLICATION INFORMATION

### DOMINANT TIME-OUT

A dominant time-out circuit in the ISO1050 prevents the driver from blocking network communications if a local controller fault occurs. The time-out circuit is triggered by a falling edge on TXD. If no rising edge occurs on TXD before the time-out of the circuits expires, the driver is disabled to prevent the local node from continuously transmitting a Dominant bit. If a rising edge occurs on TXD, commanding a Recessive bit, the timer will be reset and the driver will be re-enabled. The time-out value is set so that normal CAN communication will not cause the Dominant time-out circuit to expire.

### FAILSAFE

If the bus-side power supply  $V_{cc2}$  is lower than about 2.7V, the power shutdown circuits in the ISO1050 will disable the transceiver to prevent spurious transitions due to an unstable supply. If  $V_{cc1}$  is still active when this occurs, the receiver output will go to a failsafe HIGH value in about 6 microseconds.

### THERMAL SHUTDOWN

The ISO1050 has an internal thermal shutdown circuit that turns off the driver outputs when the internal temperature becomes too high for normal operation. This shutdown circuit prevents catastrophic failure due to short-circuit faults on the bus lines. If the device cools sufficiently after thermal shutdown, it will automatically re-enable, and may again rise in temperature if the bus fault is still present. Prolonged operation with thermal shutdown conditions may affect device reliability.

### REVISION HISTORY

Changes from Original (June 2009) to Revision A	Page
• Added Typical 25-Year Life at Rated Working Voltage to Features.....	1
• Added LIFE EXPECTANCY vs WORKING VOLTAGE section.....	11



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
ISO1050DUB	ACTIVE	SOP	DUB	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
ISO1050DUBR	ACTIVE	SOP	DUB	8	350	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

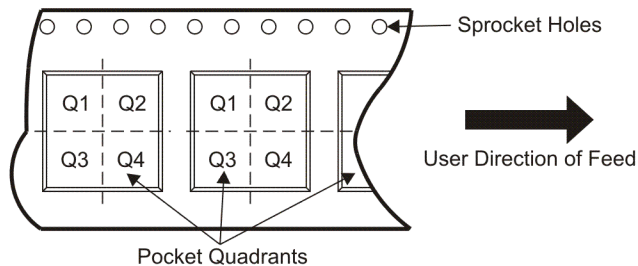
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1050DUBR	SOP	DUB	8	350	330.0	24.4	10.9	10.01	5.85	16.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

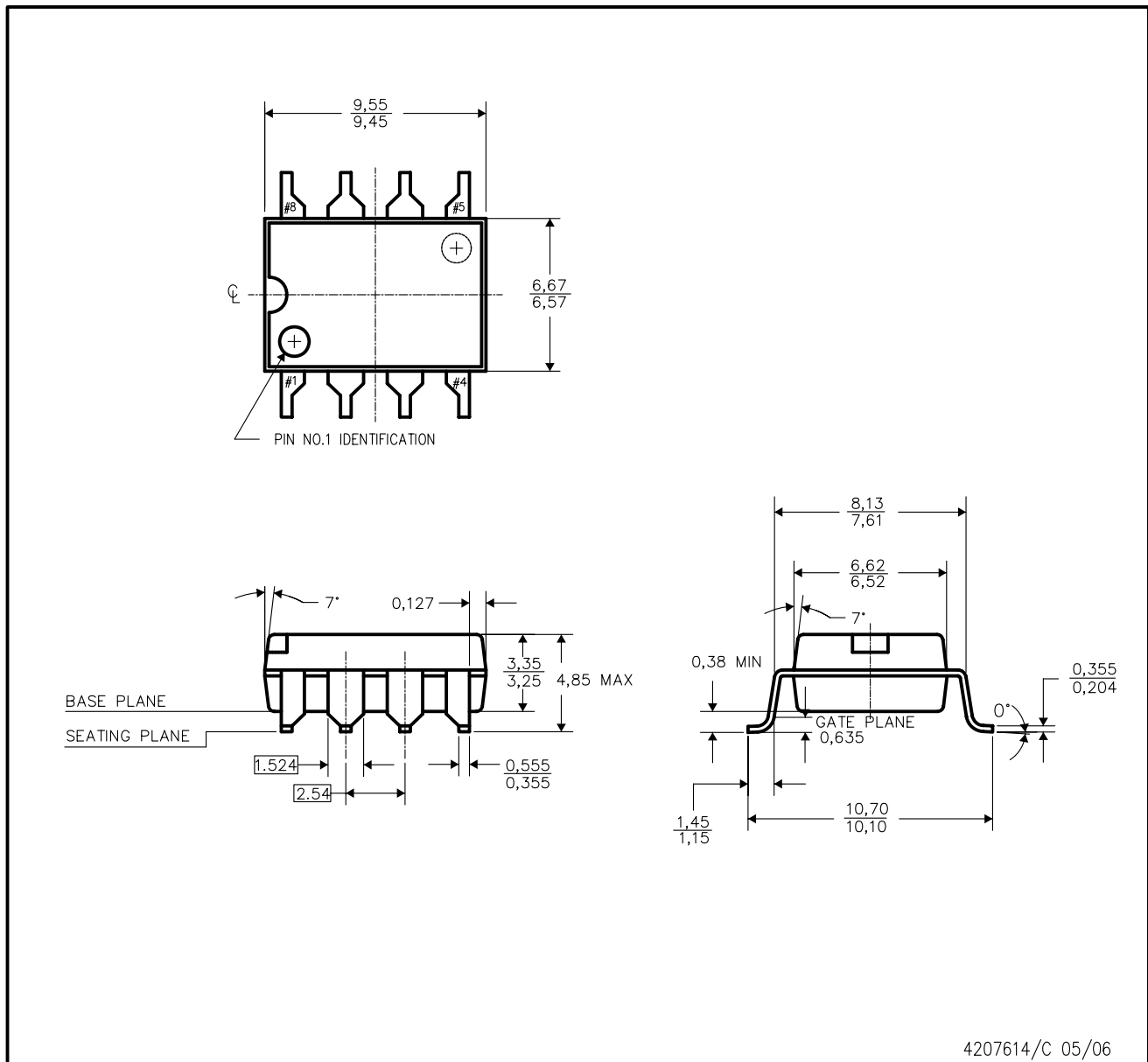


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1050DUBR	SOP	DUB	8	350	358.0	335.0	35.0

DUB (R-PDSO-G8)

PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ANSI Y14.5 M-1982.
  - B. This drawing is subject to change without notice.
  - C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.254mm.

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