DS90LV047A 3V LVDS Quad CMOS Differential Line Driver

Check for Samples: DS90LV047A

FEATURES

- **>400 Mbps (200 MHz) Switching Rates**
- **Flow-Through Pinout Simplifies PCB Layout**
- **300 ps Typical Differential Skew**
- **400 ps Maximum Differential Skew**
- **1.7 ns Maximum Propagation Delay**
- **3.3V Power Supply Design**
- **±350 mV Differential Signaling**
- **Low Power Dissipation (13mW at 3.3V Static)**
- **Interoperable with Existing 5V LVDS Receivers**
- **High impedance on LVDS Outputs on Power Down**
- **Conforms to TIA/EIA-644 LVDS Standard**
- **Industrial Operating Temperature Range (−40°C to +85°C)**
- **Available in Surface Mount (SOIC) and Low Profile TSSOP Package**

DESCRIPTION

The DS90LV047A is a quad CMOS flow-through differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV047A accepts low voltage TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition, the driver supports a TRI-STATE function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13 mW typical. The DS90LV047A has a flow-through pinout for easy PCB layout.

The EN and EN* inputs are ANDed together and control the TRI-STATE outputs. The enables are common to all four drivers. The DS90LV047A and companion line receiver (DS90LV048A) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Connection Diagram

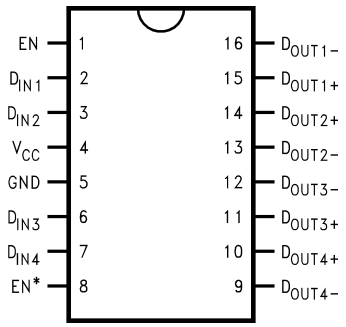
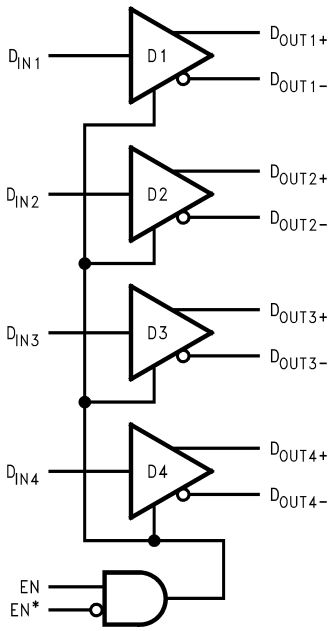


Figure 1. Order Number DS90LV047ATM, DS90LV047ATMTC
D0016A, PW0016A Packages

Truth Table

ENABLES		INPUT	OUTPUTS	
EN	**EN***	**D_{IN}**	**D_{OUT+}**	**D_{OUT-}**
H	L or Open	L	L	H
		H	H	L
All other combinations of ENABLE inputs		X	Z	Z

Functional Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC})		−0.3V to +4V
Input Voltage (D_{IN})		−0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (EN, EN*)		−0.3V to (V_{CC} + 0.3V)
Output Voltage (D_{OUT+}, D_{OUT-})		−0.3V to +3.9V
Short Circuit Duration	(D_{OUT+}, D_{OUT-})	Continuous
Maximum Package Power Dissipation @ +25°C	D0016A Package	1088 mW
	PW0016A Package	866 mW
	Derate D0016A Package	8.5 mW/°C above +25°C
	Derate PW0016A Package	6.9 mW/°C above +25°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range	Soldering (4 sec.)	+260°C
Maximum Junction Temperature		+150°C
ESD Rating(2)	(HBM, 1.5 kΩ, 100 pF)	≥ 10 kV
	(EIAJ, 0 Ω, 200 pF)	≥ 1200 V

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.

(2) ESD Ratings:
HBM (1.5 kΩ, 100 pF) ≥ 10 kV
EIAJ (0 Ω, 200 pF) ≥ 1200 V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified(1)(2)(3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Output Voltage	R_L = 100Ω (Figure 2)	D_{OUT-} D_{OUT+}	250	310	450	mV
ΔV_{OD1}	Change in Magnitude of V_{OD1} for Complementary Output States				1	35	|mV|
V_{OS}	Offset Voltage			1.125	1.17	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				1	25	|mV|
V_{OH}	Output High Voltage				1.33	1.6	V
V_{OL}	Output Low Voltage			0.90	1.02		V
V_{IH}	Input High Voltage		D_{IN}, EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.5V		−10	2	+10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V		−10	−2	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.8		V
I_{OS}	Output Short Circuit Current(4)	ENABLED, D_{IN} = V_{CC}, D_{OUT+} = 0V or D_{IN} = GND, D_{OUT-} = 0V	D_{OUT-} D_{OUT+}		−4.2	−9.0	mA
I_{OSD}	Differential Output Short Circuit Current(4)	ENABLED, V_{OD} = 0V			−4.2	−9.0	mA
I_{OFF}	Power-off Leakage	V_{OUT} = 0V or 3.6V, V_{CC} = 0V or Open		−20	±1	+20	µA
I_{OZ}	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V V_{OUT} = 0V or V_{CC}		−10	±1	+10	µA
I_{CC}	No Load Supply current Drivers Enabled	D_{IN} = V_{CC} or GND	V_{CC}		4.0	8.0	mA
I_{CCL}	Loaded Supply Current Drivers Enabled	R_L = 100Ω All Channels, D_{IN} = V_{CC} or GND (all inputs)			20	30	mA
I_{CCZ}	No Load Supply Current Drivers Disabled	D_{IN} = V_{CC} or GND, EN = GND, EN* = V_{CC}			2.2	6.0	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.
(2) All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.
(3) The DS90LV047A is a current mode device and only functions within datasheet specifications when a resistive load is applied to the driver outputs typical range is (90Ω to 110Ω).
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Switching Characteristics

V_{CC} = +3.3V ± 10%, T_A = −40°C to +85°C(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 15 pF (Figure 3 and Figure 4)	0.5	0.9	1.7	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.5	1.2	1.7	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$(4)		0	0.3	0.4	ns
t_{SKD2}	Channel-to-Channel Skew(5)		0	0.4	0.5	ns
t_{SKD3}	Differential Part to Part Skew(6)		0		1.0	ns
t_{SKD4}	Differential Part to Part Skew(7)		0		1.2	ns
t_{TLH}	Rise Time			0.5	1.5	ns
t_{THL}	Fall Time			0.5	1.5	ns
t_{PHZ}	Disable Time High to Z	R_L = 100Ω, C_L = 15 pF (Figure 5 and Figure 6)		2	5	ns
t_{PLZ}	Disable Time Low to Z			2	5	ns
t_{PZH}	Enable Time Z to High			3	7	ns
t_{PZL}	Enable Time Z to Low			3	7	ns
f_{MAX}	Maximum Operating Frequency(8)		200	250		MHz

(1) All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r ≤ 1 ns, and t_f ≤ 1 ns.
(3) C_L includes probe and jig capacitance.
(4) t_{SKD1} $|t_{PHLD} - t_{PLHD}|$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) t_{SKD2} is the Differential Channel-to-Channel Skew of any event on the same device.
(6) t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(7) t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(8) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, 0V to 3V. Output Criteria: duty cycle = 45%/55%, VOD > 250mV, all channels switching.

Parameter Measurement Information

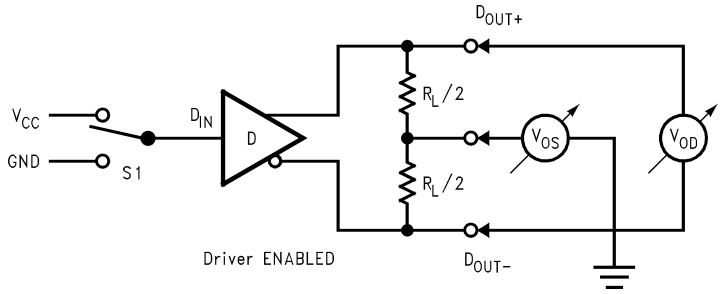


Figure 2. Driver V_{OD} and V_{OS} Test Circuit

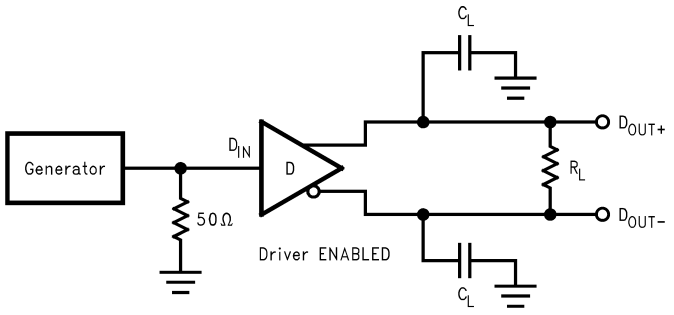


Figure 3. Driver Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (continued)

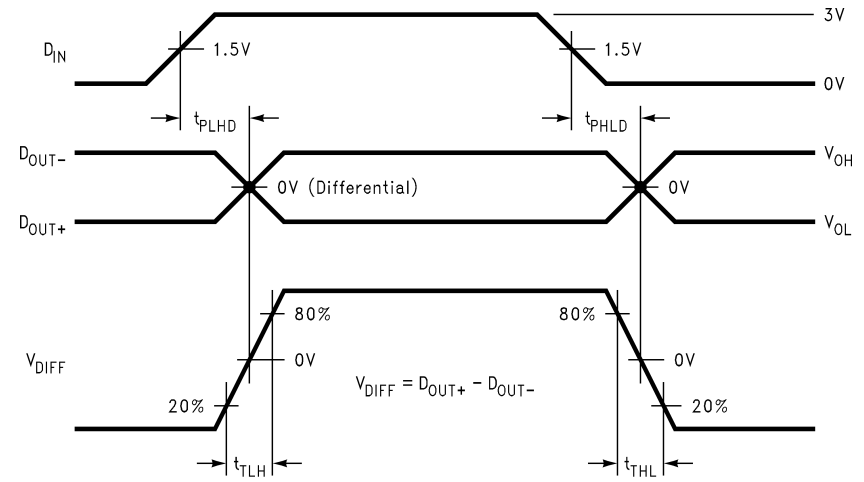


Figure 4. Driver Propagation Delay and Transition Time Waveforms

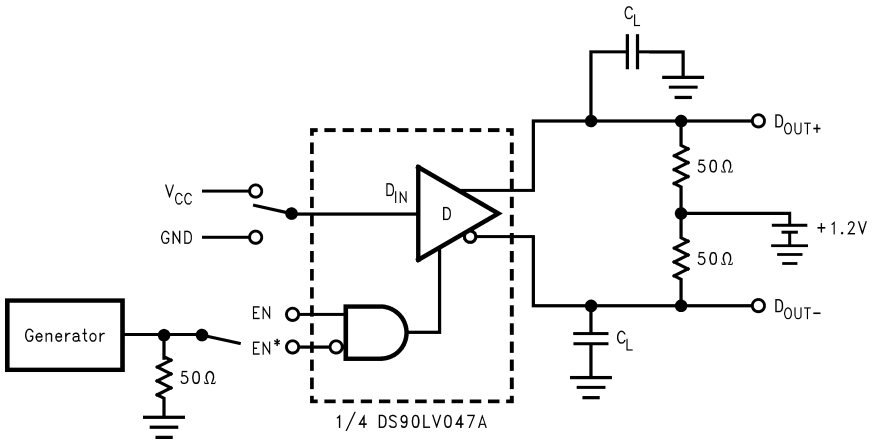


Figure 5. Driver TRI-STATE Delay Test Circuit

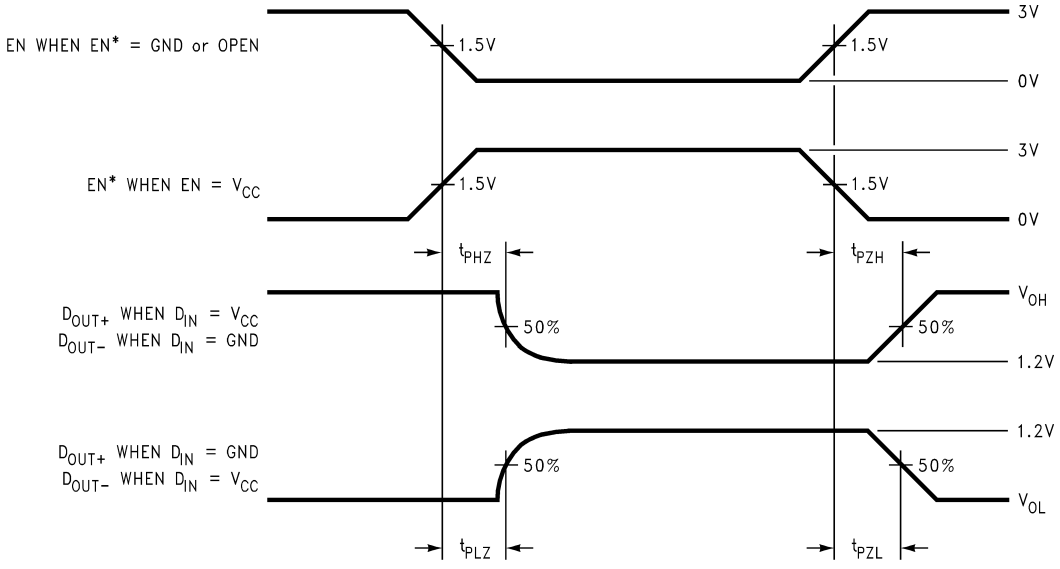


Figure 6. Driver TRI-STATE Delay Waveform

Typical Application

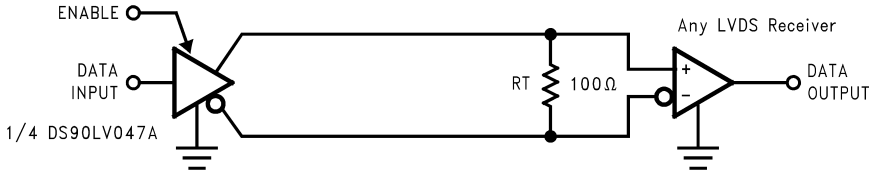


Figure 7. Point-to-Point Application

APPLICATION INFORMATION

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (lit #550062-001), AN808, AN977, AN971, AN916, AN805, AN903.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 7. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic differential impedance of the media is in the range of 100Ω. A termination resistor of 100Ω (selected to match the media), and is located as close to the receiver input pins as possible. The termination resistor converts the driver output current (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV047A differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 3.1 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode driver **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 7. AC or unterminated configurations are not allowed. The 3.1 mA loop current will develop a differential voltage of 310mV across the 100Ω termination resistor which the receiver detects with a 250mV minimum differential noise margin, (driven signal minus receiver threshold (250mV – 100mV = 150mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in Figure 8. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 620mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

The DS90LV047A has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

POWER DECOUPLING RECOMMENDATIONS

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1µF and 0.001µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

PC BOARD CONSIDERATIONS

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

DIFFERENTIAL TRACES

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number or vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

TERMINATION

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX).

PROBING LVDS TRANSMISSION LINES

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

CABLES AND CONNECTORS, GENERAL COMMENTS

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver.

For cable distances < 0.5M, most cables can be made to work effectively. For distances 0.5M ≤ d ≤ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

LVDS FAIL-SAFE

This section addresses the common concern of fail-safe biasing of LVDS interconnects, specifically looking at the DS90LV047A driver outputs and the DS90LV048A receiver inputs.

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90LV048A is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will ensure a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the DS90LV047A driver is disconnected (cable unplugged), or if the DS90LV047A driver is in a TRI-STATE or power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

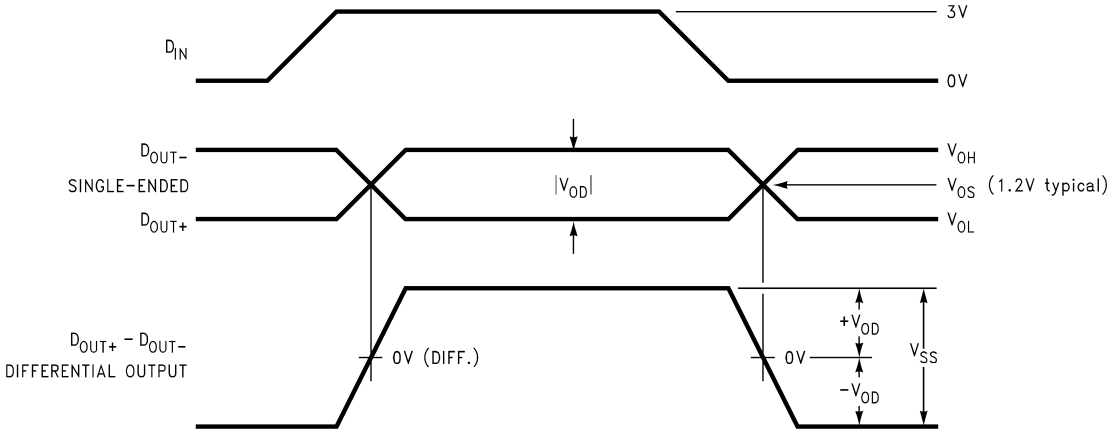


Figure 8. Driver Output Levels

PIN DESCRIPTIONS

Pin No.	Name	Description
2, 3, 6, 7	D_{IN}	Driver input pin, TTL/CMOS compatible
10, 11, 14, 15	D_{OUT+}	Non-inverting driver output pin, LVDS levels
9, 12, 13, 16	D_{OUT-}	Inverting driver output pin, LVDS levels
1	EN	Driver enable pin: When EN is low, the driver is disabled. When EN is high and EN* is low or open, the driver is enabled. If both EN and EN* are open circuit, then the driver is disabled.
8	EN*	Driver enable pin: When EN* is high, the driver is disabled. When EN* is low or open and EN is high, the driver is enabled. If both EN and EN* are open circuit, then the driver is disabled.
4	V_{CC}	Power supply pin, +3.3V ± 0.3V
5	GND	Ground pin

Typical Performance Curves

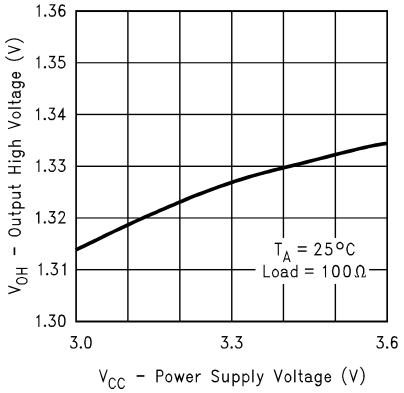


Figure 9. Output High Voltage vs Power Supply Voltage

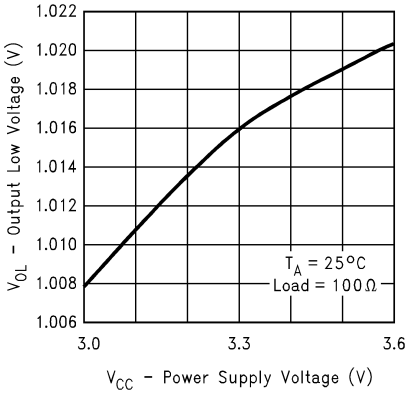


Figure 10. Output Low Voltage vs Power Supply Voltage

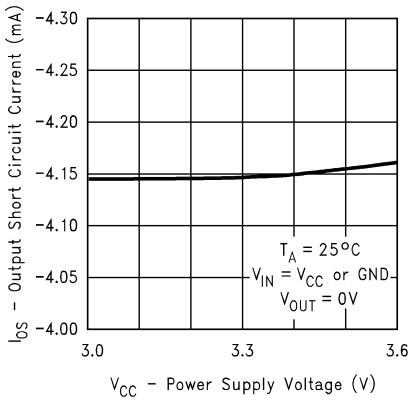


Figure 11. Output Short Circuit Current vs Power Supply Voltage

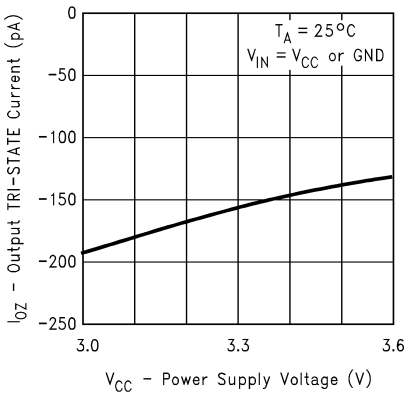


Figure 12. Output TRI-STATE Current vs Power Supply Voltage

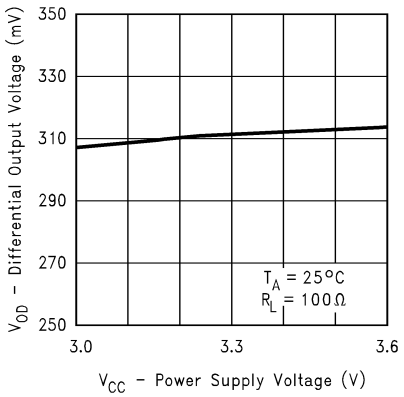


Figure 13. Differential Output Voltage vs Power Supply Voltage

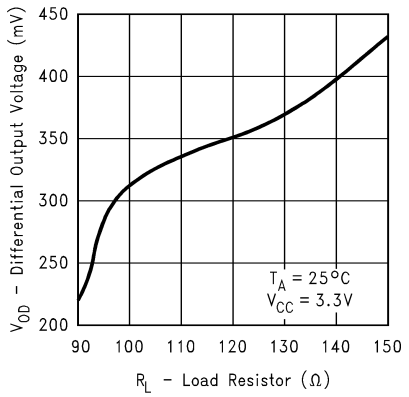


Figure 14. Differential Output Voltage vs Load Resistor

Typical Performance Curves (continued)

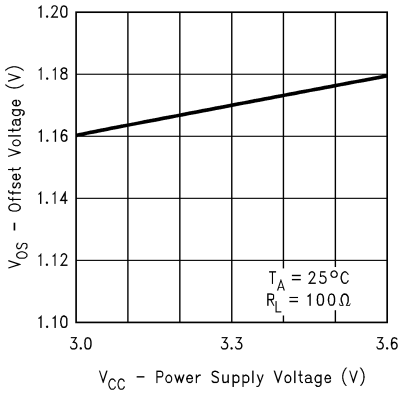


Figure 15. Offset Voltage vs Power Suppy Voltage

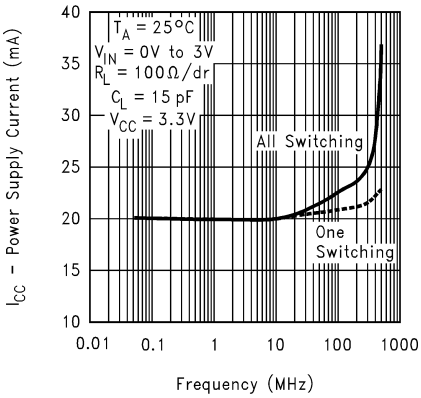


Figure 16. Power Supply Current vs Frequency

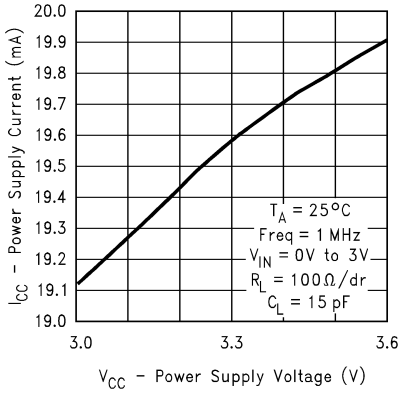


Figure 17. Power Supply Current vs Power Supply Voltage

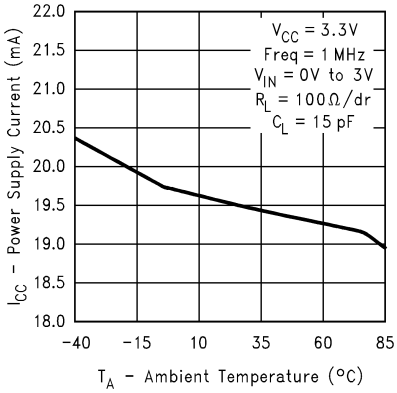


Figure 18. Power Supply Current vs Ambient Temperature

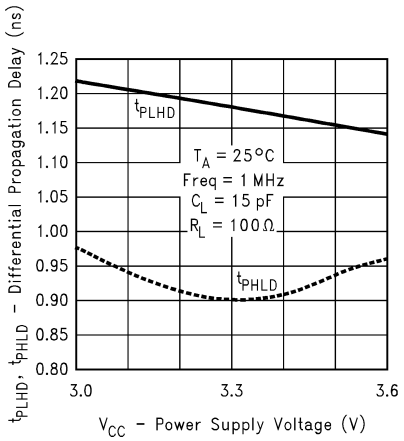


Figure 19. Differential Propagation Delay vs Power Supply Voltage

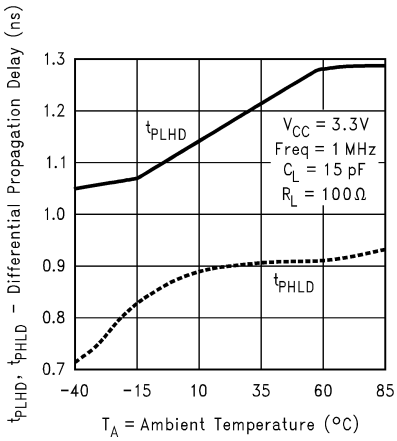


Figure 20. Differential Propagation Delay vs Ambient Temperature

Typical Performance Curves (continued)

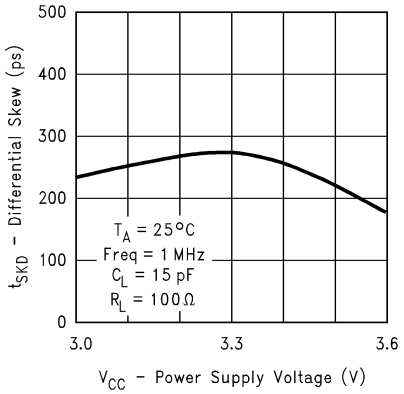


Figure 21. Differential Skew vs Power Supply Voltage

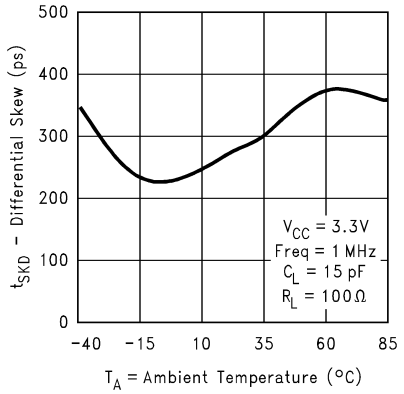


Figure 22. Differential Skew vs Ambient Temperature

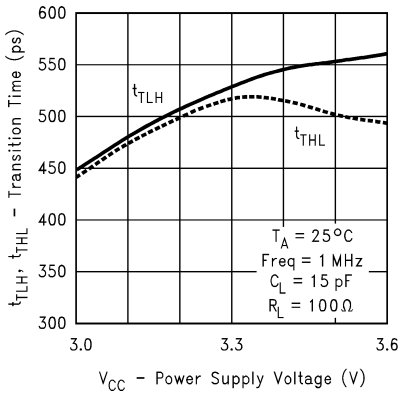


Figure 23. Transition Time vs Power Supply Voltage

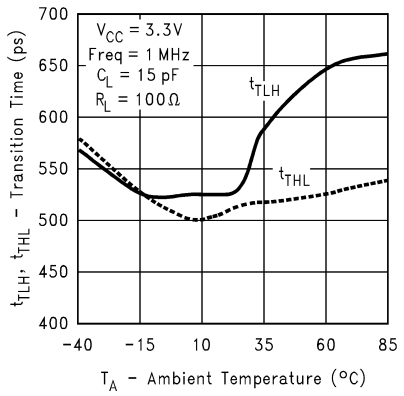


Figure 24. Transition Time vs Ambient Temperature

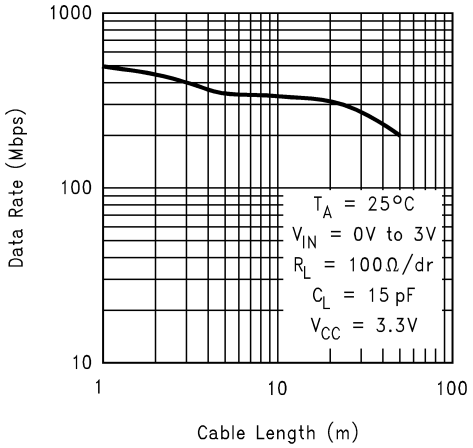


Figure 25. Data Rate vs Cable Length

Data Rate vs Cable Length Graph Test Procedure

A pseudo-random bit sequence (PRBS) of 2^9-1 bits was programmed into a function generator (Tektronix HFS9009) and connected to the driver inputs via 50Ω cables and SMB connectors. An oscilloscope (Tektronix 11801B) was used to probe the resulting eye pattern, measured differentially at the input to the receiver. A 100Ω resistor was used to terminate the pair at the far end of the cable. The measurements were taken at the far end of the cable, at the receiver"s input, and used for the jitter analysis for this graph (Figure 25). The frequency of the input signal was increased until the measured jitter (t_{tcs}) equaled 20% with respect to the unit interval (t_{tui}) for the particular cable length under test. Twenty percent jitter is a reasonable place to start with many system designs. The data used was NRZ. Jitter was measured at the 0V differential voltage of the differential eye pattern. The cables used were LG UTP 4 pair 24 gauge CAT 5 cables. The DS90LV047A and DS90LV048A were tested using the new LVDS Flow-Evaluation Board LVDS47/48PCB which is available in the LVDS47/48EVK evaluation kit.

The curve shows very good typical performance that can be used as a design guideline for data rate vs cable length. Increasing the jitter percentage increases the curve respectively, allowing the device to transmit faster over longer cable lengths. This relaxes the jitter tolerance of the system allowing more jitter into the system, which could reduce the reliability and efficiency of the system. Alternatively, decreasing the jitter percentage will have the opposite effect on the system. The area under the curve is considered the safe operating area based on the above signal quality criteria. For more information on eye pattern testing, please see TI Application Note AN-808.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV047ATM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS90LV047A TM	
DS90LV047ATM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90LV047A TM	Samples
DS90LV047ATMTC	NRND	TSSOP	PW	16	92	TBD	Call TI	Call TI	-40 to 85	DS90LV 047AT	
DS90LV047ATMTC/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90LV 047AT	Samples
DS90LV047ATMTCX	NRND	TSSOP	PW	16	2500	TBD	Call TI	Call TI	-40 to 85	DS90LV 047AT	
DS90LV047ATMTCX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90LV 047AT	Samples
DS90LV047ATMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90LV047A TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

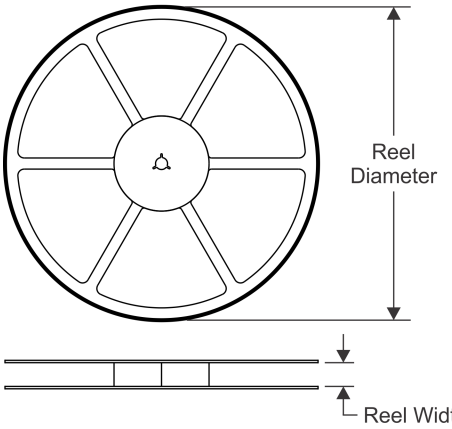
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

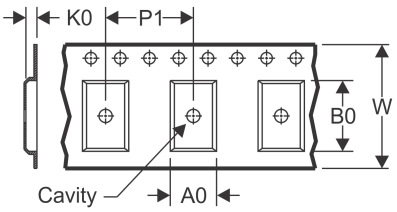
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

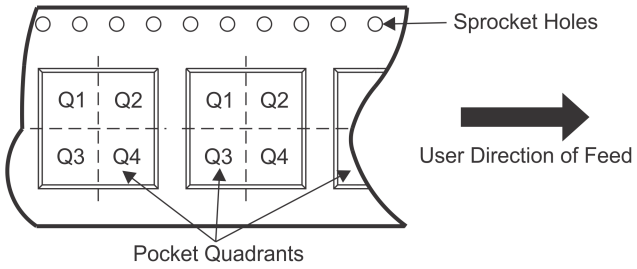


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

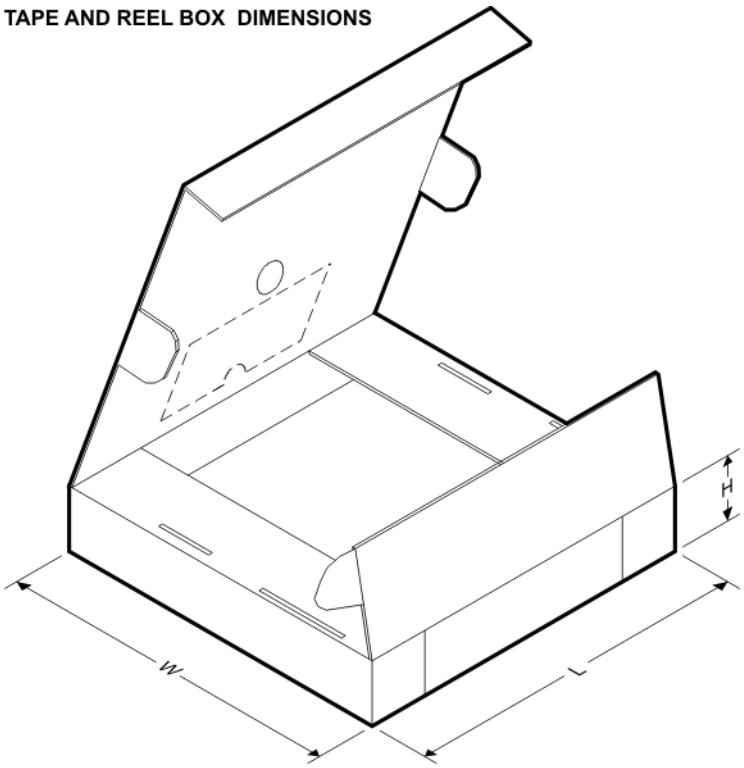
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV047ATMTCX	TSSOP	PW	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
DS90LV047ATMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

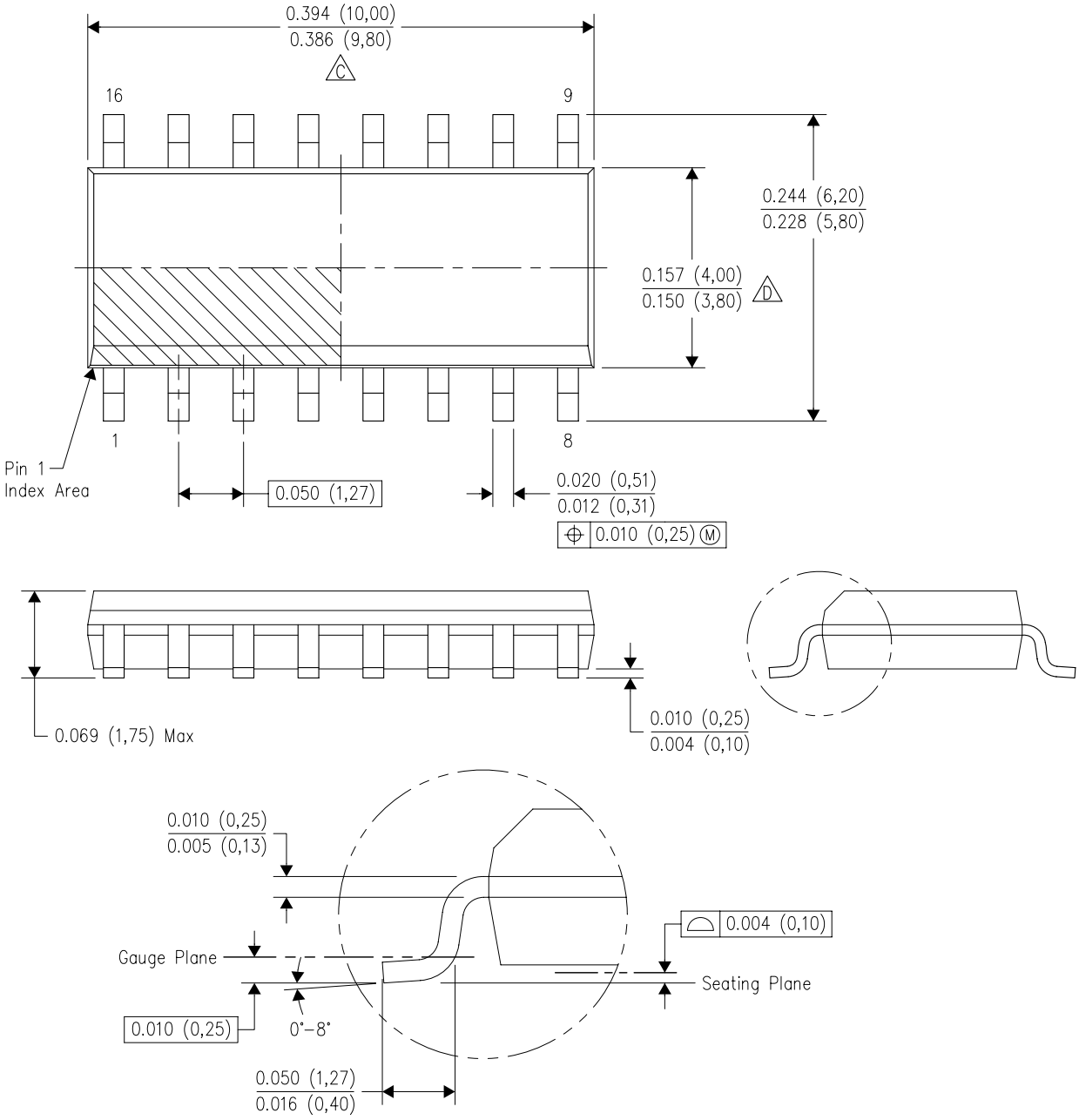
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

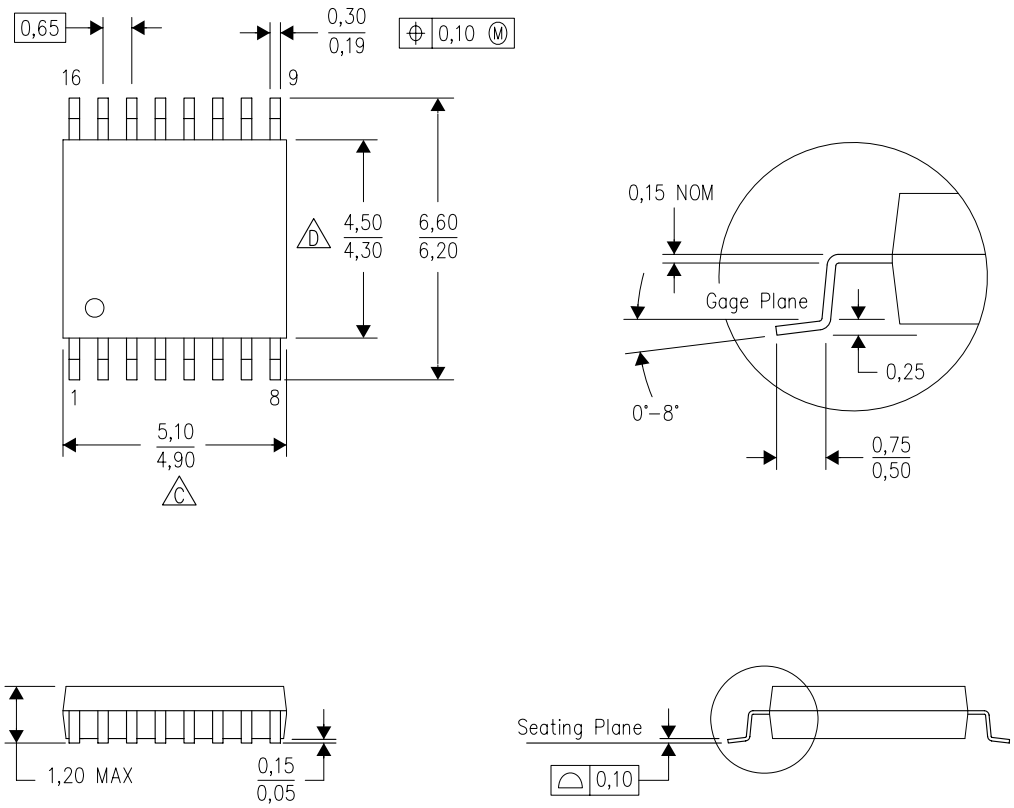
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV047ATMTCX	TSSOP	PW	16	2500	367.0	367.0	35.0
DS90LV047ATMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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