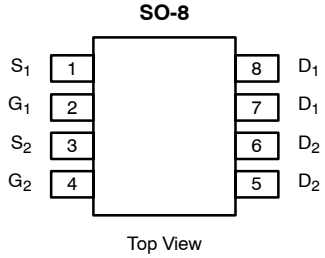
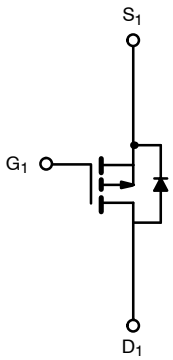
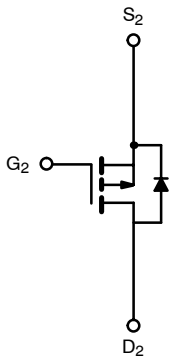
Dual P-Channel 60-V (D-S) 175° MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−60	0.120 @ V_{GS} = −10 V	−3.1
	0.150 @ V_{GS} = −4.5 V	−2.8





P-Channel MOSFET



P-Channel MOSFET

Ordering Information: Si4948BEY—E3 (Lead Free)
Si4948BEY-T1—E3 (Lead Free with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	−60		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	−3.1	−2.4	A
	T_A = 70°C		−2.6	−2.0	
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	−25		
Continuous Source Current (Diode Conduction)[a]		I_S	−2	−1.1	
Avalanche Current	L = 0.1 mH	I_{AS}	15		
Single Pulse Avalanche Energy		E_{AS}	11		mJ
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.4	1.4	W
	T_A = 70°C		1.7	0.95	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	53	62.5	°C/W
	Steady State		85	110	
Maximum Junction-to-Foot	Steady State	R_{thJF}	30	37	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

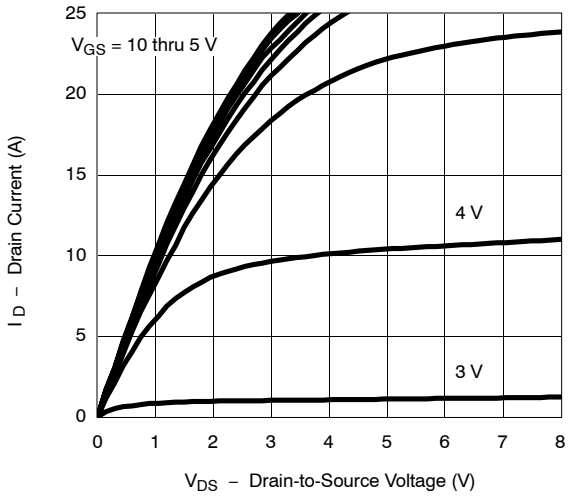
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	−1		−3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −60 V, V_{GS} = 0 V			−1	μA
		V_{DS} = −60 V, V_{GS} = 0 V, T_J = 70°C			−10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = −5 V, V_{GS} = −10 V	−25			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −3.1 A		0.100	0.120	Ω
		V_{GS} = −4.5 V, I_D = −0.2 A		0.126	0.150	
Forward Transconductance[a]	g_{fs}	V_{DS} = −15 V, I_D = −3.1 A		8.5		S
Diode Forward Voltage[a]	V_{SD}	I_S = −2 A, V_{GS} = 0 V		−0.8	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −30 V, V_{GS} = −10 V, I_D = −3.1 A		14.5	22	nC
Gate-Source Charge	Q_{gs}			2.2		
Gate-Drain Charge	Q_{gd}			3.7		
Gate Resistance	R_g	f = 1 MHz		14		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −30 V, R_L = 30 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_g = 6 Ω		10	15	ns
Rise Time	t_r			15	22	
Turn-Off Delay Time	$t_{d(off)}$			50	75	
Fall Time	t_f			35	55	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −2 A, di/dt = 100 A/μs		30	50	

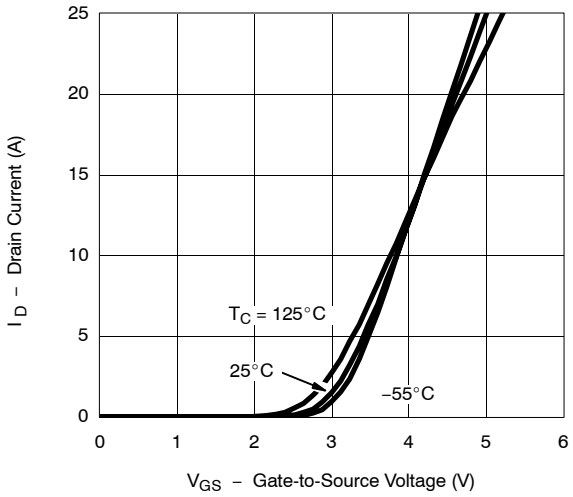
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

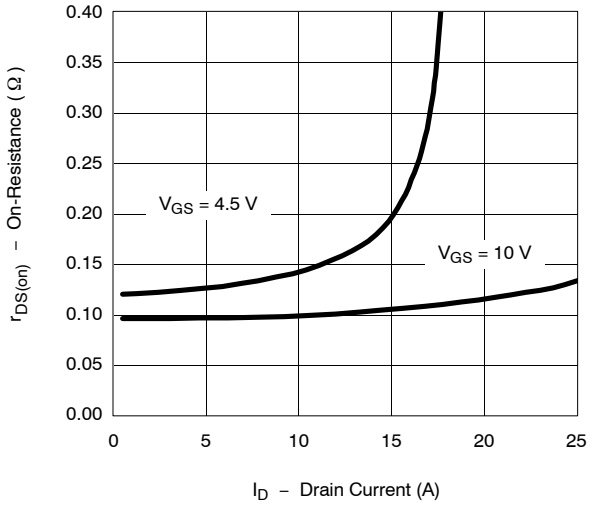


Transfer Characteristics

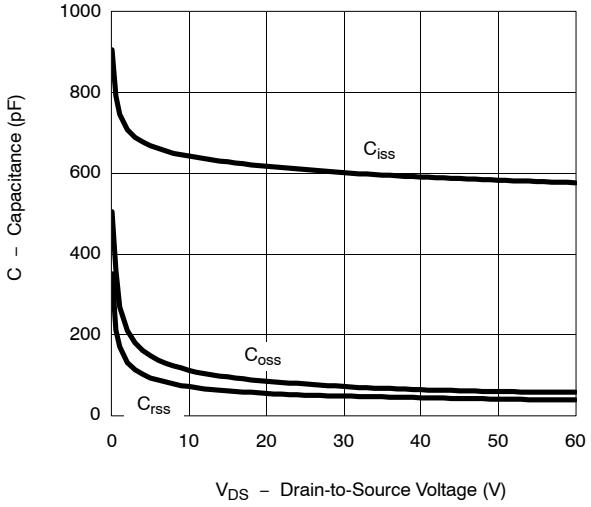


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

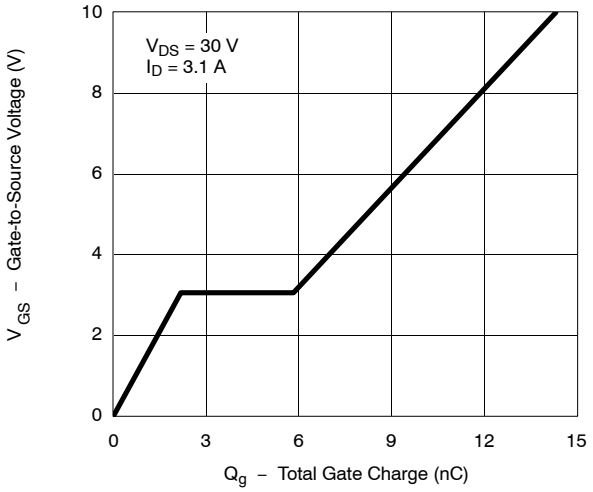
On-Resistance vs. Drain Current



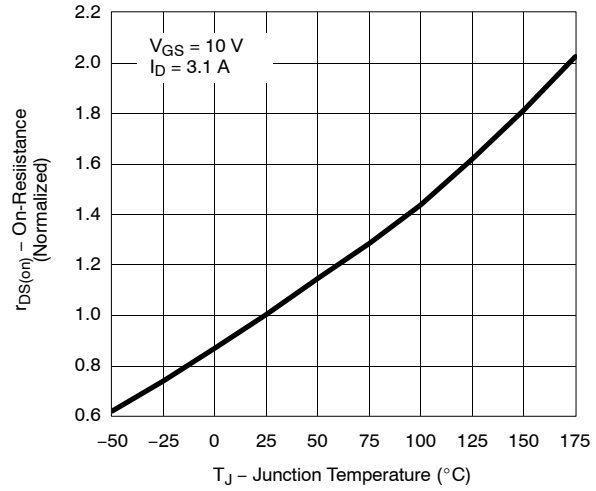
Capacitance



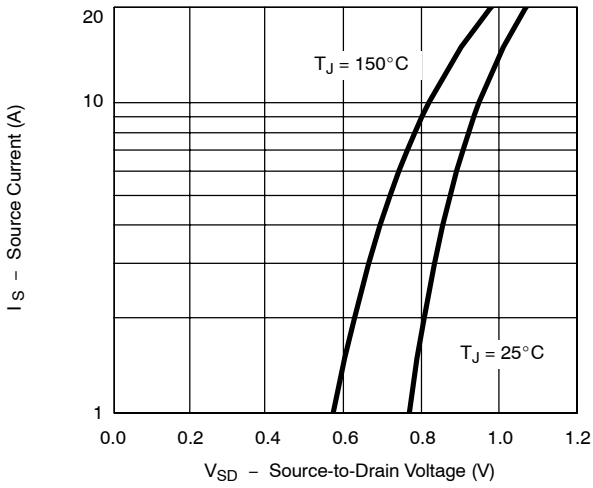
Gate Charge



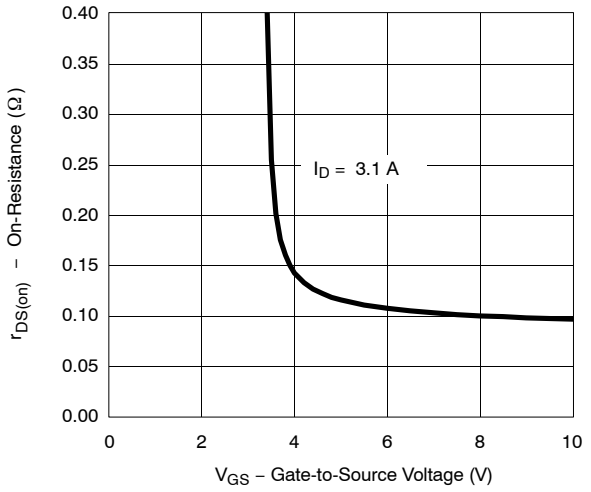
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

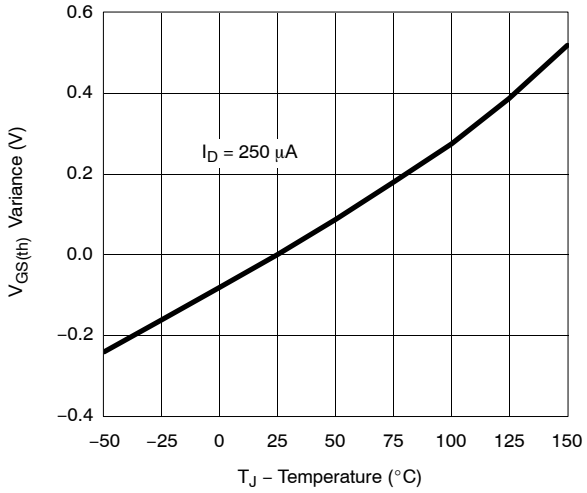


On-Resistance vs. Gate-to-Source Voltage

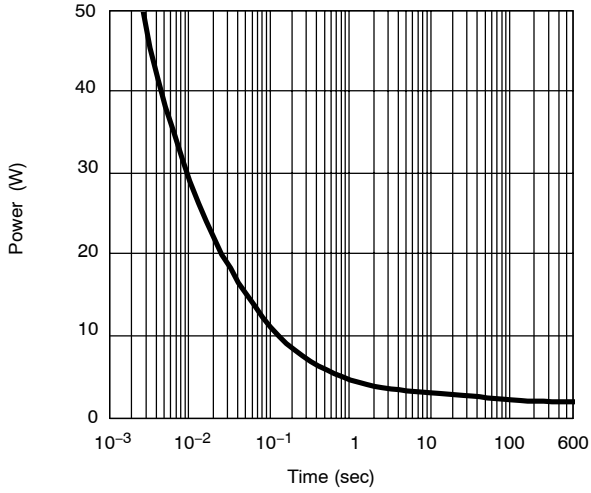


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

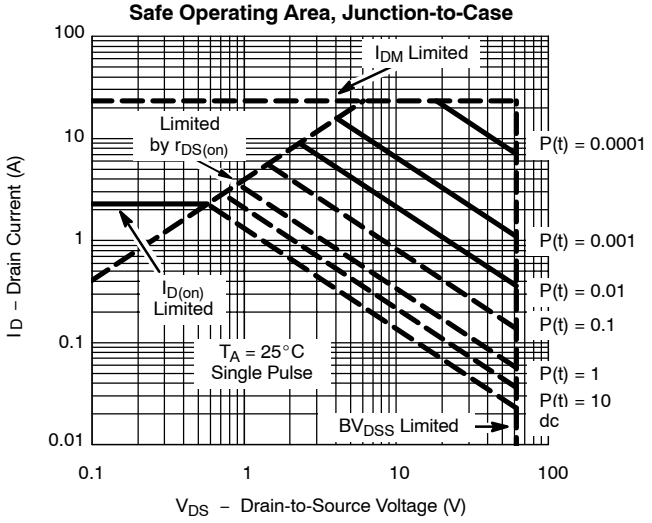
Threshold Voltage



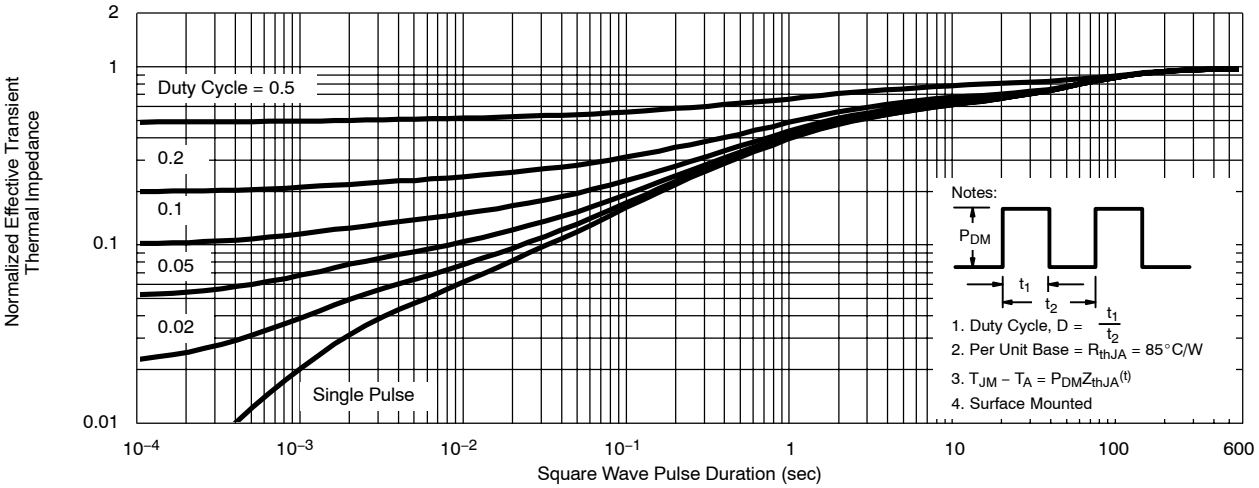
Single Pulse Power



Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)