

## Power MOSFET


 Available  
**RoHS\***  
 COMPLIANT

PRODUCT SUMMARY	
$V_{DS}$ (V)	- 50
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10$ V   0.14
$Q_g$ (Max.) (nC)	39
$Q_{gs}$ (nC)	10
$Q_{gd}$ (nC)	15
Configuration	Single

### FEATURES

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

### Note

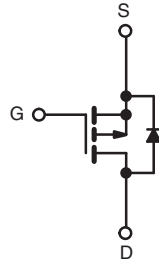
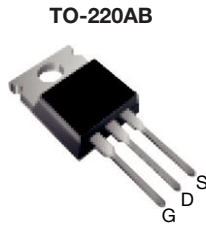
\* Lead (Pb)-containing terminations are not RoHS-compliant. Exemptions may apply.

### DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the power MOSFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The p-channel power MOSFET's are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common n-channel Power MOSFET's such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-channel power MOSFETs are intended for use in power stages where complementary symmetry with n-channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.



P-Channel MOSFET

### ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF9Z30PbF
	SiHF9Z30-E3
SnPb	IRF9Z30
	SiHF9Z30

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	- 50	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at - 10 V	$T_C = 25^\circ\text{C}$	- 18	A
		$T_C = 100^\circ\text{C}$	- 11	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	- 60		
Linear Derating Factor		0.59	W/ $^\circ\text{C}$	
Inductive Current, Clamped	$L = 100 \mu\text{H}$	$I_{LM}$	- 60	A
Unclamped Inductive Current (Avalanche Current)		$I_L$	- 3.1	A
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	74	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 $^\circ$	

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
- $V_{DS} = -25$  V, starting  $T_J = 25^\circ\text{C}$ ,  $L = 100 \mu\text{H}$ ,  $R_g = 25 \Omega$
- 0.063" (1.6 mm) from case.

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	80	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.7	

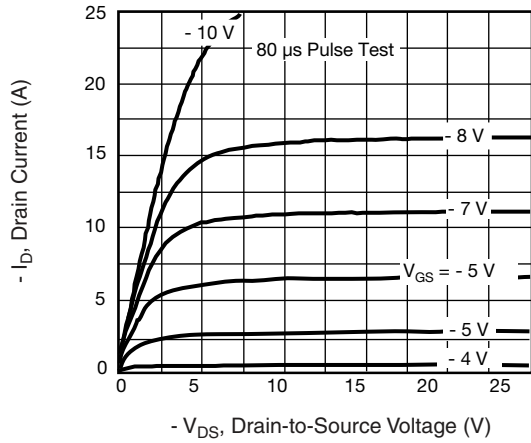
**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = -250\text{ }\mu\text{A}$	- 50	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$	- 2.0	-	- 4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 500$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{max. rating}$ , $V_{GS} = 0\text{ V}$	-	-	- 250	$\mu\text{A}$
		$V_{DS} = \text{max. rating} \times 0.8$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ °C}$	-	-	- 1000	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$   $I_D = -9.3\text{ A}^b$	-	0.093	0.14	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 2 \times V_{GS}$ , $I_{DS} = -9\text{ A}^b$	3.1	4.7	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = -25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 9	-	900	-	pF
Output Capacitance	$C_{oss}$		-	570	-	
Reverse Transfer Capacitance	$C_{rss}$		-	140	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$   $I_D = -18\text{ A}$ , $V_{DS} = -0.8$ max. rating. see fig. 17	-	26	39	nC
Gate-Source Charge	$Q_{gs}$		-	6.9	10	
Gate-Drain Charge	$Q_{gd}$		-	9.7	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -25\text{ V}$ , $I_D = -18\text{ A}$ , $R_g = 13\text{ }\Omega$ , $R_D = 1.3\text{ }\Omega$ , see fig. 16 (MOSFET switching times are essentially independent of operating temperature)	-	12	18	ns
Rise Time	$t_r$		-	110	170	
Turn-Off Delay Time	$t_{d(off)}$		-	21	32	
Fall Time	$t_f$		-	64	96	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode	-	-	- 18	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	- 60	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ °C}$ , $I_S = -18\text{ A}$ , $V_{GS} = 0\text{ V}^b$	-	-	- 6.3	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ °C}$ , $I_F = -18\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$	54	120	250	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		0.20	0.47	1.1	$\mu\text{C}$

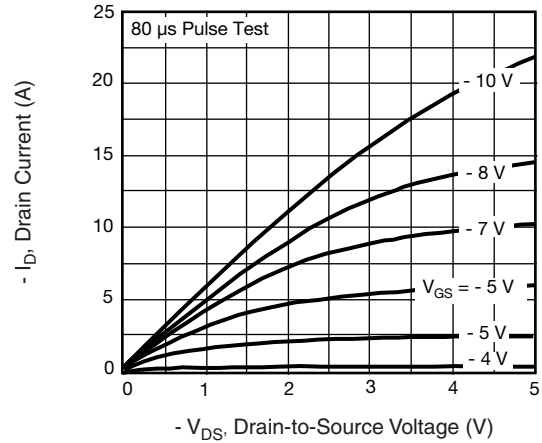
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

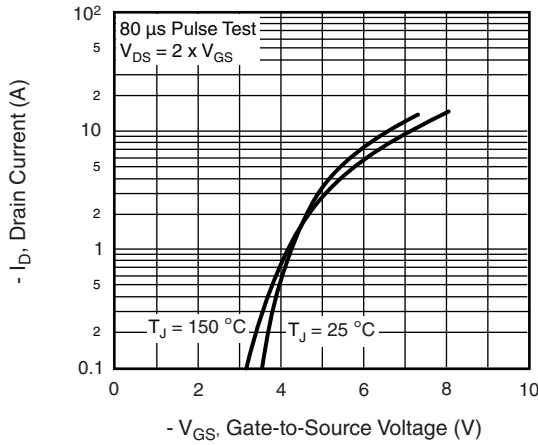
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



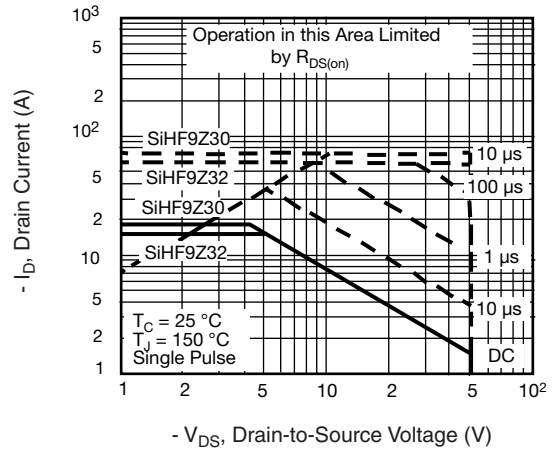
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Saturation Characteristics**



**Fig. 2 - Typical Transfer Characteristics**



**Fig. 4 - Maximum Safe Operating Area**

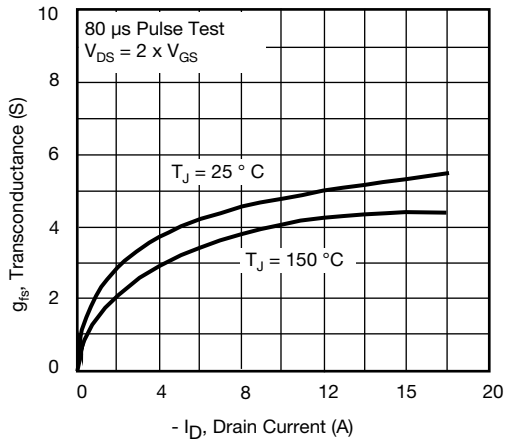


Fig. 5 - Typical Transconductance vs. Drain Current

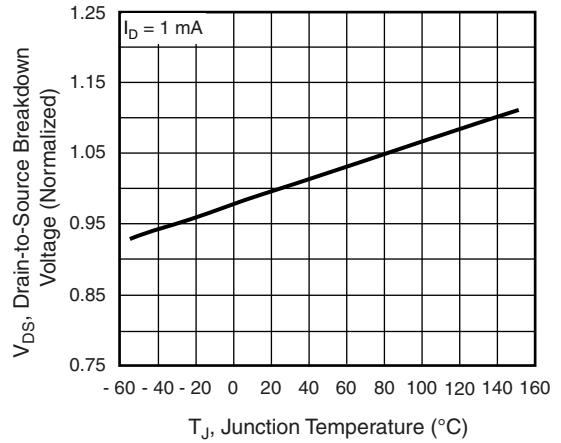


Fig. 7 - Breakdown Voltage vs. Temperature

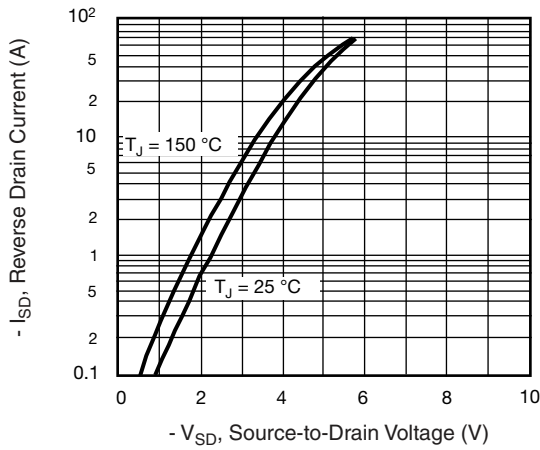


Fig. 6 - Typical Source-Drain Diode Forward Voltage

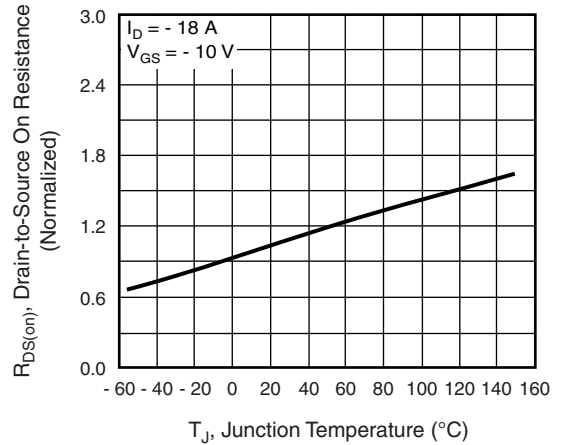


Fig. 8 - Normalized On-Resistance vs. Temperature

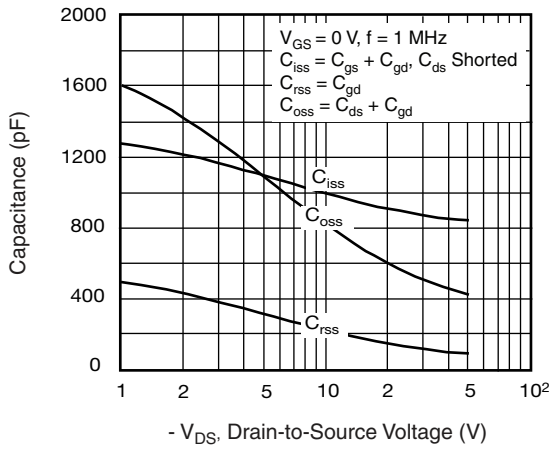


Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

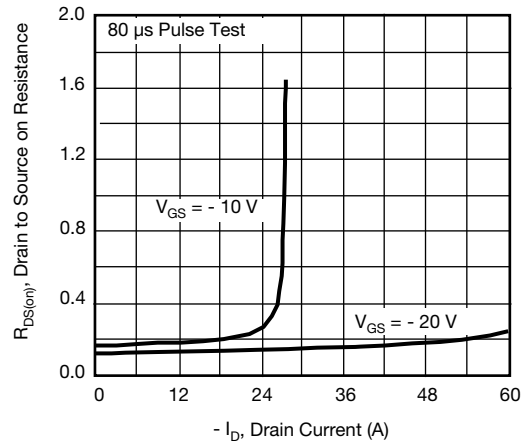


Fig. 11 - Typical On-Resistance vs. Drain Current

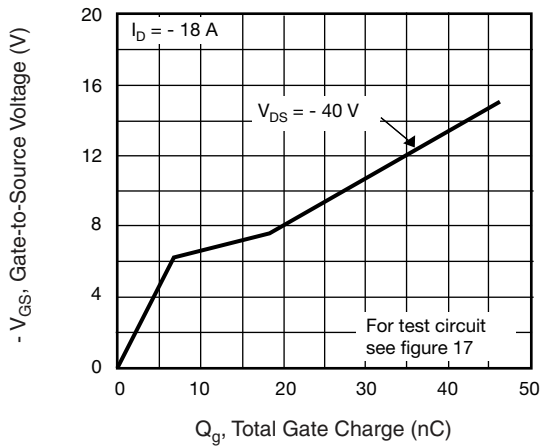


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

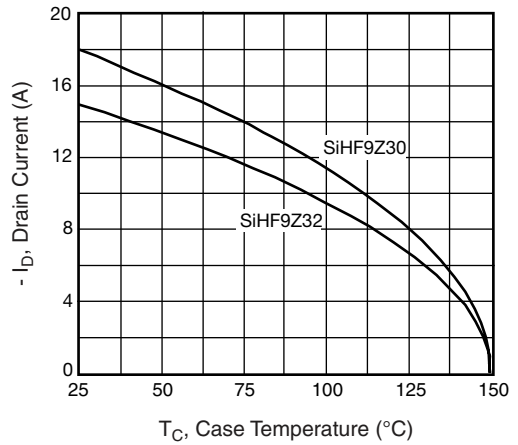


Fig. 12 - Maximum Drain Current vs. Case Temperature

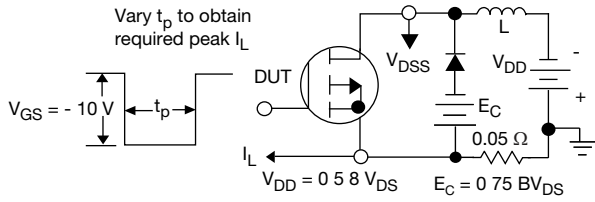


Fig. 13a - Unclamped Inductive Test Circuit

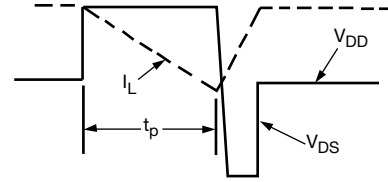


Fig. 13b - Unclamped Inductive Load Test Waveforms

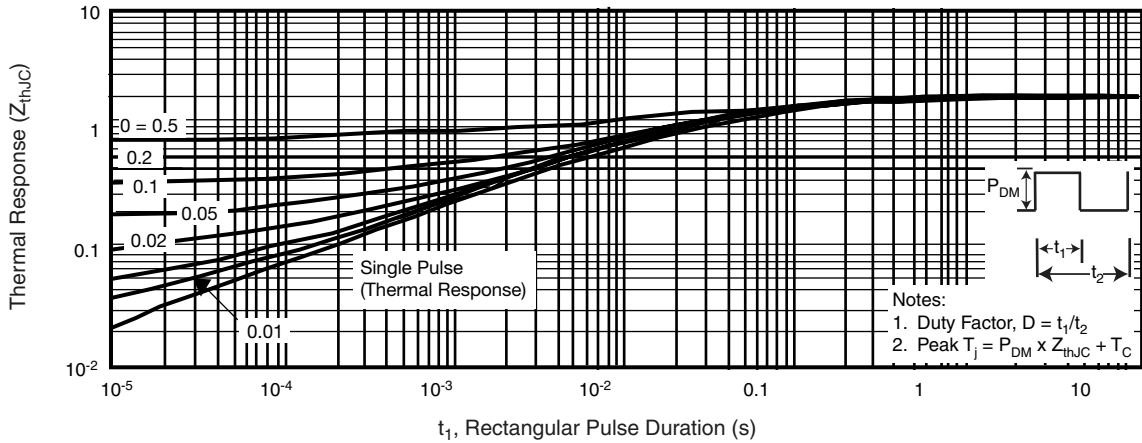


Fig. 14 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

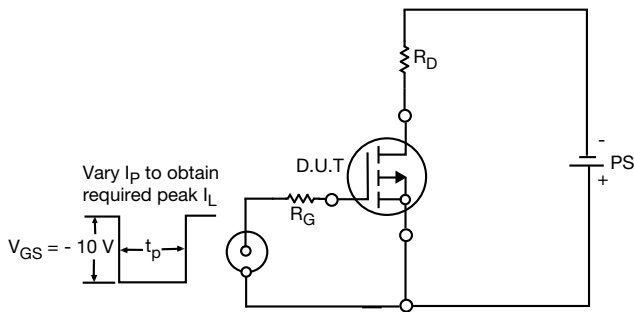


Fig. 15 - Switching Time Test Circuit

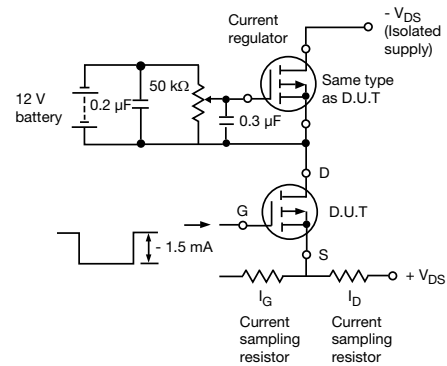


Fig. 16 - Gate Charge Test Circuit

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## TO-220-1

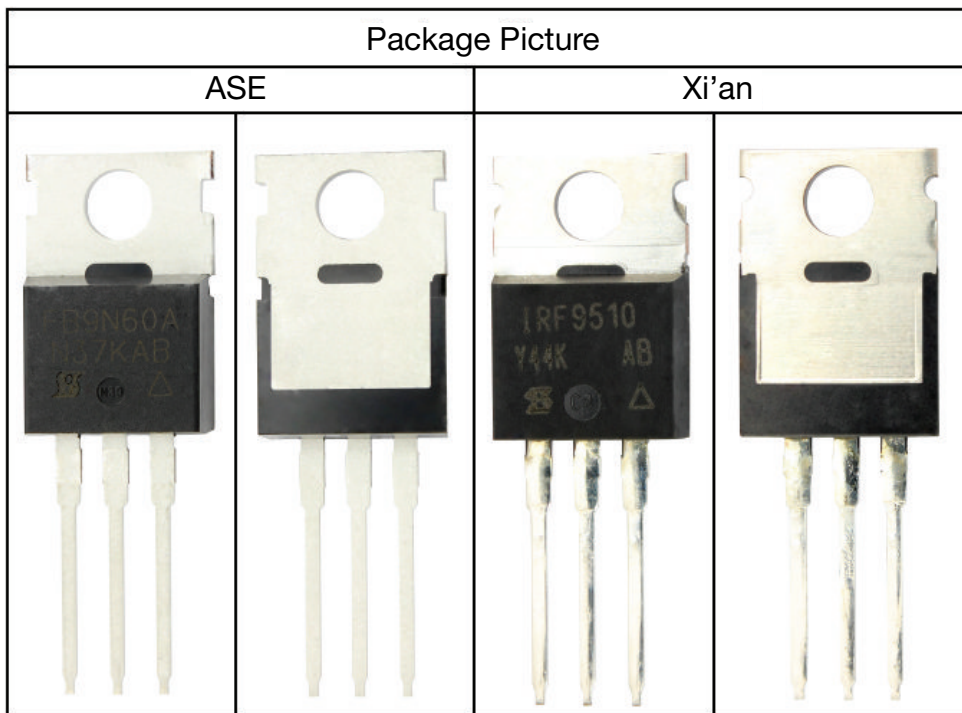


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15  
DWG: 6031

**Note**

- M\* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM





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