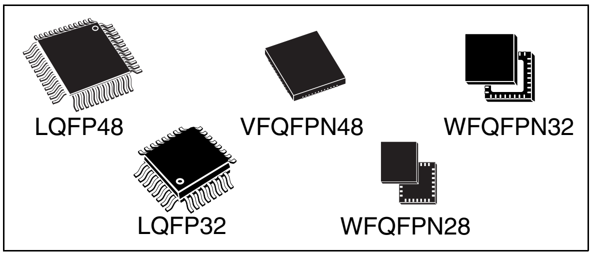
STM8L151xx, STM8L152xx

8-bit ultralow power MCU, up to 32 KB Flash, 1 KB Data EEPROM RTC, LCD, timers, USART, I2C, SPI, ADC, DAC, comparators

Preliminary data

Features

- Operating conditions
  - Operating power supply range 1.8 V to 3.6 V (down to 1.65 V at power down)
  - Temperature range: - 40 °C to 85 or 125 °C
- Low power features
  - 5 low power modes: Wait , Low power run (5.4 µA), Low power wait (3 µA), Active-halt with RTC (1 µA), Halt (400 nA)
  - Dynamic consumption: 192 µA/MHz
  - Ultralow leakage per I/0: 50 nA
  - Fast wakeup from Halt: 5 µs
- Advanced STM8 core
  - Harvard architecture and 3-stage pipeline
  - Max freq. 16 MHz, 16 CISC MIPS peak
  - Up to 40 external interrupt sources
- Reset and supply management
  - Low power, ultrasafe BOR reset with 5 selectable thresholds
  - Ultralow power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 1 to 16 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - Internal 38 kHz low consumption RC
  - Clock security system
- Low power RTC
  - BCD calendar with alarm interrupt
  - Auto-wakeup from Halt w/ periodic interrupt
- LCD: up to 4x28 segments w/ step-up converter
- Memories
  - Up to 32 KB of Flash program memory and 1 Kbyte of data EEPROM with ECC, RWW
  - Flexible write and read protection modes
  - Up to 2 Kbytes of RAM
- DMA
  - 4 channels; supported peripherals: ADC, DAC, SPI, I2C, USART, timers
  - 1 channel for memory-to-memory
- 12-bit DAC with output buffer



- 12-bit ADC up to 1 Msps/25 channels
  - T. sensor and internal reference voltage
- 2 Ultralow power comparators
  - 1 with fixed threshold and 1 rail to rail
  - Wakeup capability
- Timers
  - Two 16-bit timers with 2 channels (used as IC, OC, PWM), quadrature encoder
  - One 16-bit advanced control timer with 3 channels, supporting motor control
  - One 8-bit timer with 7-bit prescaler
  - 2 watchdogs: 1 Window, 1 Independent
  - Beeper timer with 1, 2 or 4 kHz frequencies
- Communication interfaces
  - Synchronous serial interface (SPI)
  - Fast I2C 400 kHz SMBus and PMBus
  - USART (ISO 7816 interface and IrDA)
- Up to 41 I/Os, all mappable on interrupt vectors
- Up to 16 capacitive sensing channels with free firmware
- Development support
  - Fast on-chip programming and non intrusive debugging with SWIM
  - Bootloader using USART
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM8L151xx (without LCD)	STM8L151C6, STM8L151C4, STM8L151K6, STM8L151K4, STM8L151G6, STM8L151G4
STM8L152xx (with LCD)	STM8L152C6, STM8L152C4, STM8L152K6, STM8L152K4

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1 Introduction

This document describes the STM8L15xxx family features, pinout, mechanical data and ordering information.

For more details on the whole STMicroelectronics Ultralow power family please refer to *Section 2.2: Ultralow power continuum on page 11*.

The reference manual and Flash programming manuals will be available soon.

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

2 Description

The STM8L15xxx devices are members of the STM8L Ultralow power 8-bit family. They are referred to as medium-density devices in the STM8L15xxx reference manual (RM0031) and in the STM8L Flash programming manual (PM0054). They provide the following benefits:

- Integrated system
  - Up to 32 Kbytes of medium-density embedded Flash program memory
  - 1 Kbyte of data EEPROM
  - Internal high speed and low-power low speed RC.
  - Embedded reset
- Ultralow power consumption
  - 192 µA/MHZ (dynamic consumption)
  - 1 µA in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low power wait mode and Low power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Wide choice of development tools

The STM8L15xxx family operates from 1.8 V to 3.6 V (down to 1.65 V at power down) and is available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

The STM8L15xxx Ultralow power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive In-Application debugging and ultrafast Flash programming.

All STM8L15xxx microcontrollers feature embedded data EEPROM and low power low-voltage single-supply program Flash memory.

The STM8L15xxx family 8-bit microcontrollers incorporate an extensive range of enhanced I/Os and peripherals. All devices offer 12-bit ADC, DAC, two comparators, Real-time clock three 16-bit timers, one 8-bit timer as well as standard communication interface such as SPI, I2C and USART. A 4x28-segment LCD is available on the STM8L152xx line.

The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

These features make the STM8L15xxx microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors

Figure 1 on page 12 shows the general block diagram of the device family.

Six different packages are proposed from 28 to 48 pins. Depending on the device chosen, different sets of peripherals are included. *Section 3 on page 12* gives an overview of the complete range of peripherals proposed in this family.

All STM8L Ultralow power products are based on the same architecture with the same memory mapping and a coherent pinout.

2.1 Device overview

Table 2. STM8L15x low power device features and peripheral counts

Features		STM8L151Gx		STM8L15xKx		STM8L15xCx	
Flash (Kbytes)		16	32	16	32	16	32
Data EEPROM (Kbytes)		1					
RAM-Kbytes		2		2		2	
LCD		No		4x17 (1)		4x28 (1)	
Timers	Basic	1 (8-bit)		1 (8-bit)		1 (8-bit)	
	General purpose	2 (16-bit)		2 (16-bit)		2 (16-bit)	
	Advanced control	1 (16-bit)		1 (16-bit)		1 (16-bit)	
Communication interfaces	SPI	1		1		1	
	I2C	1		1		1	
	USART	1		1		1	
GPIOs		26(3)		30 (2)(3) or 29 (1)(3)		41(3)	
12-bit synchronized ADC (number of channels)		1 (18)		1 (22 (2) or 21 (1))		1 (25)	
12-Bit DAC (number of channels)		1 (1)		1 (1)		1 (1)	
Comparators COMP1/COMP2		2		2		2	
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator					
CPU frequency		16 MHz					
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power down)					
Operating temperature		-40 to +85 °C / -40 to +125 °C					
Packages		WFQFPN28 (4)(4x4; 0.8 mm thickness)		WFQFPN32 (5)(5x5; 0.8 mm thickness) LQFP32(7x7)		VFQFPN48 (6)(4x4; 1 mm thickness) LQFP48	

1. STM8L152xx versions only
2. STM8L151xx versions only
3. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).
4. WFQFPN28 package used in the sampling phase. In the production phase, the UFQFPN28 package will be used with a thickness equal to 0.6 mm.
5. WFQFPN32 package used in the sampling phase. In the production phase, the UFQFPN32 package will be used with a thickness equal to 0.6 mm.
6. VFQFPN48 package used in the sampling phase. In the production phase, the UFQFPN48 package will be used with a thickness equal to 0.6 mm.

2.2 Ultralow power continuum

The Ultralow power STM8L151xx and STM8L152xx are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers UtraLowPower strategy which also includes STM8L101xx and STM32L15xxx. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13 µm ultralow leakage process.

Note: 1 The STM8L151xx and STM8L152xx are pin-to-pin compatible with STM8L101xx devices.

2 The STM32L family is pin-to-pin compatible with the general purpose STM32F family. Please refer to STM32L15x documentation for more information on these devices.

Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex™-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the Ultralow power performance to range from 5 up to 33.3 DMIPs.

Shared peripherals

STM8L151xx/152xx and STM32L15xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC1, DAC, and comparators COMP1/COMP2
- Digital peripherals: RTC and some communication interfaces

Common system strategy

To offer flexibility and optimize performance, the STM8L151xx/152xx and STM32L15xx devices use a common architecture:

- Same power supply range from 1.8 to 3.6 V, down to 1.65 V at power down
- Architecture optimized to reach ultralow consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy for both STM8L15xxx and STM32L15xxx including power-on reset, power-down reset, brownout reset and programmable voltage detector.

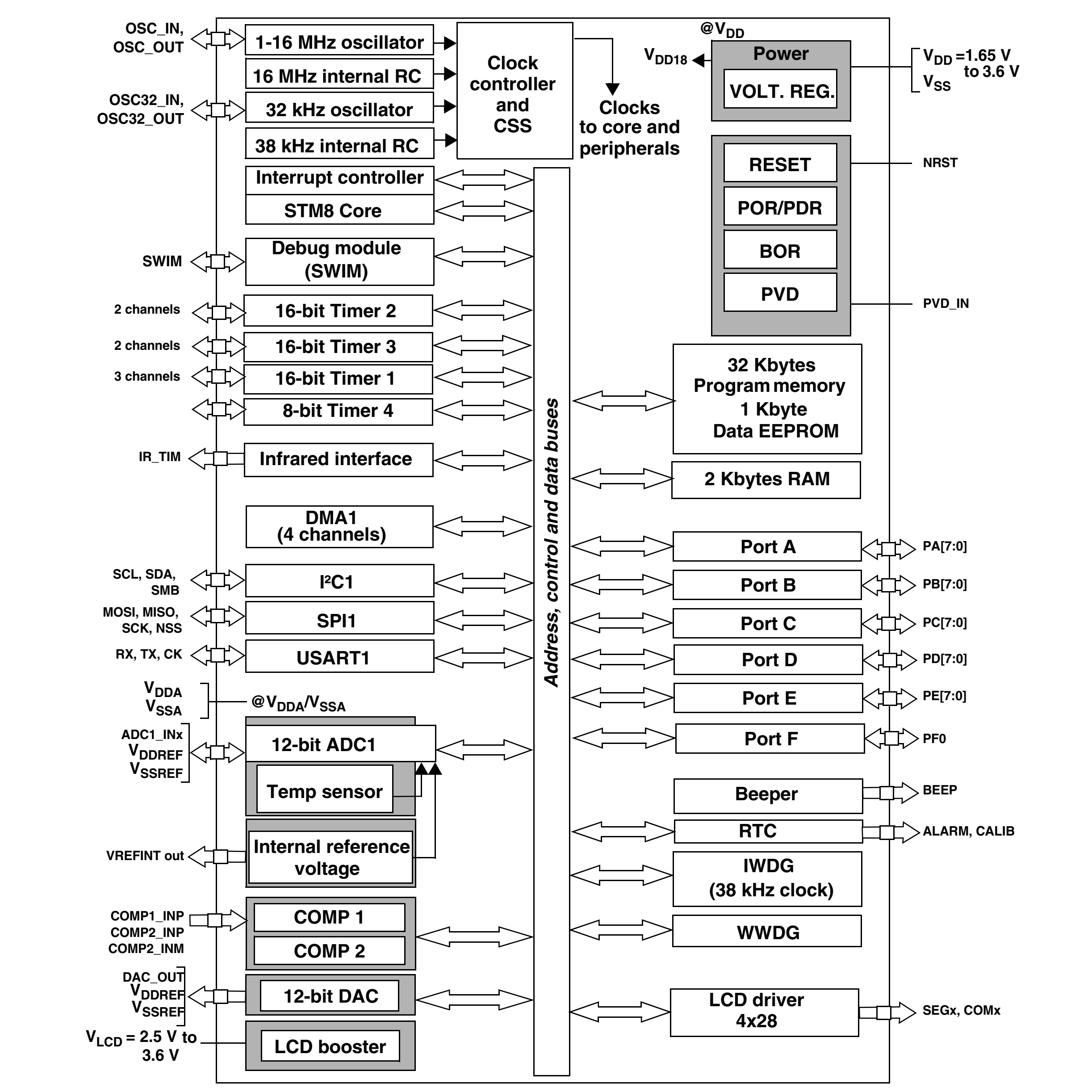
Features

ST UtraLowPower continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbytes

3 Functional overview

Figure 1. STM8L15xxx device block diagram



1. **Legend**:
ADC: Analog-to-digital converter
BOR: Brownout reset
DMA: Direct memory access
DAC: Digital-to-analog converter
I²C: Inter-integrated circuit multimaster interface
IWDG: Independent watchdog
LCD: Liquid crystal display
POR/PDR: Power on reset / power down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

3.1 Low power modes

The STM8L15xxx supports five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode). Wait consumption is around 350 µA.
- **Low power run mode**: CPU clock runs. Flash, data EEPROM, voltage regulator and all peripherals are stopped except RTC and one other peripheral which can remain active (ex: one timer). Execution is done from RAM with a low speed oscillator (LSI or LSE). The microcontroller enters Low power run mode by software and can exit from this mode by software or by a Reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power run mode consumption is around 5.4 µA (peripherals OFF).
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power wait mode consumption is around 3 µA (peripherals OFF).
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset. Active-halt consumption with RTC on LSI is 0.9 µA. Active-halt consumption with RTC on LSE is 1 µA.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 6 µs. Halt consumption is 400 nA.

Dynamic consumption in run mode is 190 µA/MHz.

3.2 Central processing unit STM8

3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without

offset and read-modify-write type data manipulations

- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The STM8L15xxx features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS} ; V_{DD} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD} pins, the corresponding ground pin is V_{SS}.
- V_{SSA} ; V_{DDA} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{SSIO} ; V_{DDIO} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for I/Os. V_{DDIO} and V_{SSIO} must be connected to V_{DD} and V_{SS}, respectively.
- V_{REF+} ; V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.
- V_{REF+} (for DAC): external voltage reference for DAC must be provided externally through V_{REF+}.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min value at power down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains in reset state when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The STM8L15xxx embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

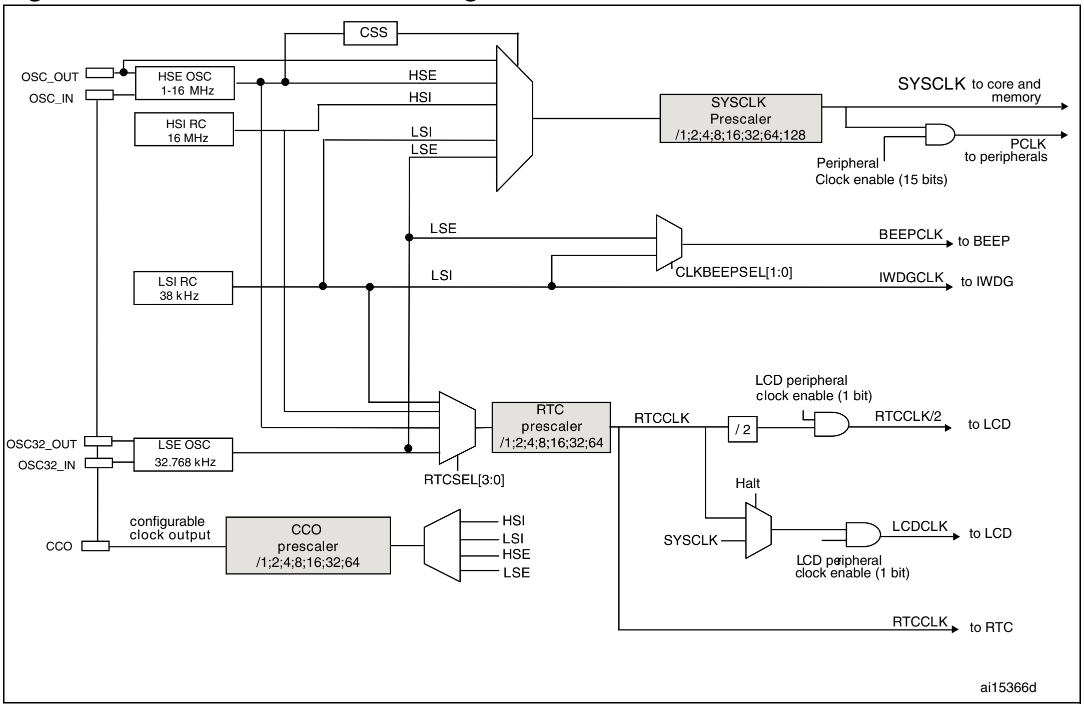
3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources can be used to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC and LCD clock sources:** the above four sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Figure 2. STM8L15x clock tree diagram



3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from every second to every year
- Active-halt consumption with LSI and Auto-wakeup: 0.9 µA
- Active-halt consumption with LSE, calendar and auto-wakeup: 1 µA

3.6 LCD (Liquid crystal display)

The liquid crystal display drives up to 4 common terminals and up to 28 segment terminals to drive up to 112 pixels.

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4 duty supported.
- Static 1/2, 1/3 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 4 pixels which can programmed to blink.
- The LCD controller can operate in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The STM8L15xxx devices have the following main features:

- Up to 2 Kbytes of RAM
- The non-volatile memory is divided into three arrays:
  - Up to 32 Kbytes of medium-density embedded Flash program memory
  - 1 Kbyte of Data EEPROM
  - Option bytes.

The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC, I2C1, SPI1, USART1, the 4 Timers.

3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 25 channels (including 1 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 µs with f_{SYSCLK}= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.10 Digital-to-analog converter (DAC)

- 12-bit DAC with output buffer
- Synchronized update capability using TIM4
- DMA capability
- External triggers for conversion
- Input reference voltage V_{REF+} for better resolution

Note: DAC can be served by DMA1.

3.11 Ultralow power comparators

The STM8L15x embeds two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage or internal reference voltage submultiple (1/4, 1/2, 3/4)

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC and the internal reference voltage V_{REFINT}. Finally, it provides a set of registers for efficiently managing a set of dedicated I/Os supporting up to 16 capacitive sensing channels using the ProxSense^{TM} technology.

3.13 Timers

STM8L15xxx devices contain one advanced control timer (TIM1), two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 3 compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

<table>
<tr><th>Timer</th><th>Counter resolution</th><th>Counter type</th><th>Prescaler factor</th><th>DMA1 request generation</th><th>Capture/compare channels</th><th>Complementary outputs</th></tr>
<tr><td>TIM1</td><td rowspan="3">16-bit</td><td rowspan="3">up/down</td><td>Any integer from 1 to 65536</td><td rowspan="4">Yes</td><td>3 + 1</td><td>3</td></tr>
<tr><td>TIM2</td><td rowspan="2">Any power of 2 from 1 to 128</td><td rowspan="2">2</td><td rowspan="3">None</td></tr>
<tr><td>TIM3</td></tr>
<tr><td>TIM4</td><td>8-bit</td><td>up</td><td>Any power of 2 from 1 to 32768</td><td>0</td></tr>
</table>

3.13.1 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 3 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- 1 additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

3.13.2 16-bit general purpose timers

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

3.13.3 8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow or for DAC trigger generation.

3.14 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

3.14.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.14.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.15 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.16 Communication interfaces

3.16.1 SPI

The serial peripheral interface (SPI1) provides half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s (f_{SYSCLK}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 can be served by the DMA1 Controller.

3.16.2 I²C

The I^2C bus interface (I^2C1) provides multi-master capability, and controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz.
- 7-bit and 10-bit addressing modes.
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.16.3 USART

The USART interface (USART1) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1 can be served by the DMA1 Controller.

3.17 Infrared (IR) interface

The STM8L15x devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.18 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1 interface.

4 Pin description

Figure 3. STM8L151Gx 28-pin package pinout

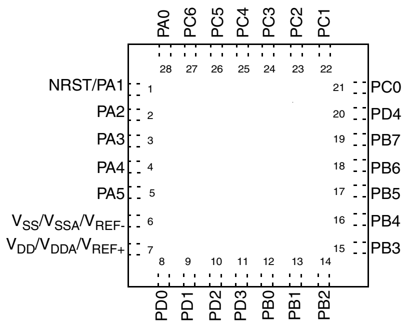
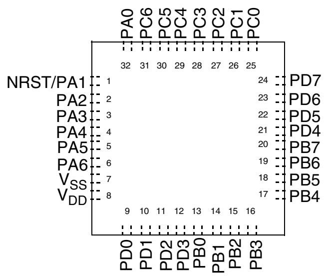
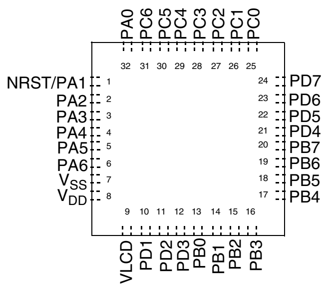


Figure 4. STM8L151Kx 32-pin package pinout (without LCD)



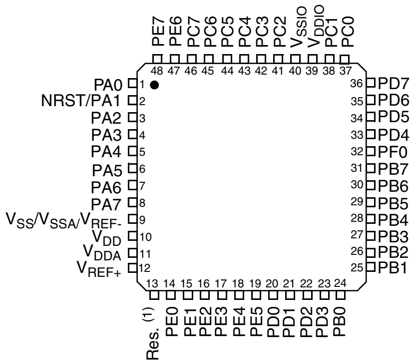
1. Example given for the WFQFPN32 package. The pinout is the same for the LQFP32 package.

Figure 5. STM8L152Kx 32-pin package pinout (with LCD)



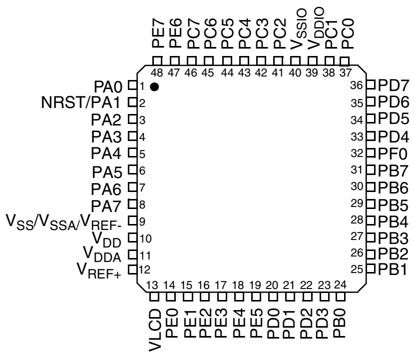
1. Example given for the WFQFPN32 package. The pinout is the same for the LQFP32 package.

Figure 6. STM8L151Cx 48-pin pinout (without LCD)



1. Reserved. Must be tied to V_{DD}.

Figure 7. STM8L152Cx 48-pin pinout (with LCD)



Legend / Abbreviations for *Table 4*:

Type: I = input, O = output, S = power supply

I/O level: FT = 5 V tolerant

Input level: CM = CMOS

Output level: HS = High sink/source (20 mA)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up
- Output: T= true open drain, OD = open drain, PP = push-pull

Reset state is shown in **bold**.

Table 4. STM8L15x pin description

Pin number: VFQFPN48 and LQFP48	Pin number: WFQFPN32	Pin number: WFQFPN28	Pin name	Type	I/O level	Input: floating	Input: wpu	Input: Ext. interrupt	Output: High sink/source	Output: OD	Output: PP	Main function (after reset)	Default alternate function
2	1	1	NRST/PA1(1)	I/O					HS	X	X	**Reset**	PA1
3	2	2	PA2/OSC_IN/ *[USART1_TX]*(3)/ *[SPI1_MISO]*(3)	I/O		**X**	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out] /*
4	3	3	PA3/OSC_OUT/*[USART1_RX]*(3)/*[SPI1_MOSI]*(3)	I/O		**X**	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/*
5	-	-	PA4/TIM2_BKIN/ LCD_COM0(2)/ADC1_IN2/ COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input / LCD COM 0 / ADC1 input 2 / Comparator 1 positive input
-	4	4	PA4/TIM2_BKIN/ *[TIM2_TRIG]*(3)/ LCD_COM0(2)/ ADC1_IN2/COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input / *[Timer 2 - trigger]* / LCD_COM 0 / ADC1 input 2 / Comparator 1 positive input
6	-		PA5/TIM3_BKIN/ LCD_COM1(2)/ADC1_IN1/ COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input / LCD_COM 1 / ADC1 input 1/ Comparator 1 positive input
-	5	5	PA5/TIM3_BKIN/ *[TIM3_TRIG]*(3)/ LCD_COM1(2)/ADC1_IN1/ COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input / *[Timer 3 - trigger]* / LCD_COM 1 / ADC1 input 1 / Comparator 1 positive input
7	6	-	PA6/*[ADC1_TRIG]*(3)/ LCD_COM2(2)/ADC1_IN0/ COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port A6**	*[ADC1 - trigger]* / LCD_COM2 / ADC1 input 0 / Comparator 1 positive input

Table 4. STM8L15x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
VFQFPN48 and LQFP48	WFQFPN32	WFQFPN28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
8	-	-	PA7/LCD_SEG0(2)	I/O	FT	**X**	X	X	HS	X	X	**Port A7**	LCD segment 0
24	13	12	PB0/TIM2_CH1/ LCD_SEG10(2)/ ADC1_IN18/COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port B0**	Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18 / Comparator 1 positive input
25	14	13	PB1/TIM3_CH1/ LCD_SEG11(2)/ ADC1_IN17/COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port B1**	Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17 / Comparator 1 positive input
26	15	14	PB2/ TIM2_CH2/ LCD_SEG12(2)/ ADC1_IN16/COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port B2**	Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16/ Comparator 1 positive input
27	-	-	PB3/TIM2_TRIG/ LCD_SEG13(2)/ ADC1_IN15/COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port B3**	Timer 2 - trigger / LCD segment 13 /ADC1_IN15 / Comparator 1 positive input
-	16	-	PB3/*[TIM2_TRIG]*(3)/ TIM1_CH2N/LCD_SEG13 (2)/ADC1_IN15/ COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port B3**	*[Timer 2 - trigger]* / Timer 1 inverted channel 2 / LCD segment 13 / ADC1_IN15 / Comparator 1 positive input
-	-	15	PB3/*[TIM2_TRIG]*(3)/ TIM1_CH1N/ LCD_SEG13(2)/ ADC1_IN15/RTC_ALARM /COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port B3**	*[Timer 2 - trigger]* / Timer 1 inverted channel 1/ LCD segment 13 / ADC1_IN15 / RTC alarm/ Comparator 1 positive input
28	-	-	PB4/*[SPI1_NSS]*(3)/ LCD_SEG14(2)/ ADC1_IN14/COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port B4**	*[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14 / Comparator 1 positive input
-	17	16	PB4/*[SPI1_NSS]*(3)/ LCD_SEG14(2)/ ADC1_IN14/ COMP1_INP/DAC_OUT	I/O		**X**	X	X	HS	X	X	**Port B4**	*[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14 / DAC output / Comparator 1 positive input
29	-	-	PB5/*[SPI1_SCK]*(3)/ LCD_SEG15(2)/ ADC1_IN13/COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port B5**	*[SPI1 clock]* / LCD segment 15 / ADC1_IN13 / Comparator 1 positive input
-	18	17	PB5/*[SPI1_SCK]*(3)/ LCD_SEG15(2)/ ADC1_IN13/DAC_OUT/ COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port B5**	*[SPI1 clock]* / LCD segment 15 / ADC1_IN13 / DAC output/ Comparator 1 positive input

Table 4. STM8L15x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
VFQFPN48 and LQFP48	WFQFPN32	WFQFPN28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
30	-	-	PB6/[*SPI1_MOSI*](3)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out/slave in]*/ LCD segment 16 / ADC1_IN12 / Comparator 1 positive input
-	19	18	PB6/*[SPI1_MOSI]*(3)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP/ DAC_OUT	I/O		**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out]*/ slave in / LCD segment 16 / ADC1_IN12 / DAC output / Comparator 1 positive input
31	20	19	PB7/*[SPI1_MISO]*(3)/ LCD_SEG17(2)/ ADC1_IN11/COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port B7**	*[SPI1 master in- slave out]* / LCD segment 17 / ADC1_IN11 / Comparator 1 positive input
37	25	21	PC0/I2C1_SDA	I/O	FT	**X**		X		T(4)		**Port C0**	I2C1 data
38	26	22	PC1/I2C1_SCL	I/O	FT	**X**		X		T(4)		**Port C1**	I2C1 clock
41	27	23	PC2/*[USART1_RX]*(3)/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREF_OUT	I/O		**X**	X	X	HS	X	X	**Port C2**	*[USART1 receive]* / LCD segment 22 / ADC1_IN6 / Comparator 1 positive input / Voltage reference output
42	28	24	PC3/*[USART1_TX]*(3)/ LCD_SEG23(2)/ ADC1_IN5/COMP1_INP/ COMP2_INM	I/O		**X**	X	X	HS	X	X	**Port C3**	*[USART1 transmit]* / LCD segment 23 / ADC1_IN5 / Comparator 1 positive input / Comparator 2 negative input
43	29	25	PC4/*[USART1_CK]*(3)/ I2C1_SMB/CCO/ LCD_SEG24(2)/ ADC1_IN4/COMP2_INM/ COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port C4**	*[USART1 synchronous clock]* / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input
44	30	26	PC5/OSC32_IN /*[SPI1_NSS]*(3)/ *[USART1_TX]*(3)	I/O		X	X	X	HS	X	X	**Port C5**	LSE oscillator input / *[SPI1 master/slave select]* / *[USART1 transmit]*
45	31	27	PC6/OSC32_OUT/ *[SPI1_SCK]*(3)/ *[USART1_RX]*(3)	I/O		X	X	X	HS	X	X	**Port C6**	LSE oscillator output / *[SPI1 clock]* / *[USART1 receive]*
46	-	-	PC7/LCD_SEG25(2)/ ADC1_IN3/COMP2_INM/ COMP1_INP	I/O		X	X	X	HS	X	X	**Port C7**	LCD segment 25 /ADC1_IN3/ Comparator negative input / Comparator 1 positive input

Table 4. STM8L15x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
VFQFPN48 and LQFP48	WFQFPN32	WFQFPN28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
20	-	8	PD0/TIM3_CH2/ *[ADC1_TRIG]*(3)/ LCD_SEG7(2)/ADC1_IN22/COMP2_INP/ COMP1_INP	I/O		X	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / LCD segment 7 / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input
-	9	-	PD0/TIM3_CH2/ *[ADC1_TRIG]*(3)/ ADC1_IN22/COMP2_INP/ COMP1_INP	I/O		X	X	X	HS	X	X	**Port D0**(5)	Timer 3 - channel 2 / *[ADC1_Trigger]* / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input
21	-	-	PD1/TIM3_TRIG/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O		X	X	X	HS	X	X	**Port D1**	Timer 3 - trigger / LCD_COM3 / ADC1_IN21 / comparator 2 positive input / Comparator 1 positive input
-	10	-	PD1/TIM1_CH3N/[*TIM3_TRIG*](3)/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O		X	X	X	HS	X	X	**Port D1**	*[Timer 3 - trigger]*/ TIM1 inverted channel 3 / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input
-	-	9	PD1/TIM1_CH3/[*TIM3_TRIG*](3)/LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O		X	X	X	HS	X	X	**Port D1**	Timer 1 channel 3 / *[Timer 3 - trigger]* / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input
22	11	10	PD2/TIM1_CH1 /LCD_SEG8(2)/ ADC1_IN20/COMP1_INP	I/O		X	X	X	HS	X	X	**Port D2**	Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20 / Comparator 1 positive input
23	12	-	PD3/ TIM1_TRIG/ LCD_SEG9(2)/ADC1_IN19/COMP1_INP	I/O		X	X	X	HS	X	X	**Port D3**	Timer 1 - trigger / LCD segment 9 / ADC1_IN19 / Comparator 1 positive input
-	-	11	PD3/ TIM1_TRIG/ LCD_SEG9(2)/ ADC1_IN19/TIM1_BKIN/ COMP1_INP/ RTC_CALIB	I/O		X	X	X	HS	X	X	**Port D3**	Timer 1 - trigger / LCD segment 9 / ADC1_IN19 / Timer 1 break input / RTC calibration / Comparator 1 positive input
33	21	20	PD4/TIM1_CH2 /LCD_SEG18(2)/ ADC1_IN10/COMP1_INP	I/O		X	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/ Comparator 1 positive input

Table 4. STM8L15x pin description (continued)

Pin number: VFQFPN48 and LQFP48	Pin number: WFQFPN32	Pin number: WFQFPN28	Pin name	Type	I/O level	Input: floating	Input: wpu	Input: Ext. interrupt	Output: High sink/source	Output: OD	Output: PP	Main function (after reset)	Default alternate function
34	22	-	PD5/TIM1_CH3 /LCD_SEG19[2]/ ADC1_IN9/COMP1_INP	I/O		X	X	X	HS	X	X	**Port D5**	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ Comparator 1 positive input
35	23	-	PD6/TIM1_BKIN /LCD_SEG20[2]/ ADC1_IN8/RTC_CALIB/ VREF_OUT/ COMP1_INP	I/O		X	X	X	HS	X	X	**Port D6**	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration / Voltage reference output / Comparator 1 positive input
36	24	-	PD7/TIM1_CH1N /LCD_SEG21[2]/ ADC1_IN7/RTC_ALARM/ VREF_OUT/ COMP1_INP	I/O		X	X	X	HS	X	X	**Port D7**	Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm / Voltage reference output /Comparator 1 positive input
14	-	-	PE0/LCD_SEG1[2]	I/O	FT	X	X	X	HS	X	X	**Port E0**	LCD segment 1
15	-	-	PE1/TIM1_CH2N /LCD_SEG2[2]	I/O		X	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2
16	-	-	PE2/TIM1_CH3N /LCD_SEG3[2]	I/O		**X**	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3
17	-	-	PE3/LCD_SEG4[2]	I/O		**X**	X	X	HS	X	X	**Port E3**	LCD segment 4
18	-	-	PE4/LCD_SEG5[2]	I/O		**X**	X	X	HS	X	X	**Port E4**	LCD segment 5
19	-	-	PE5/LCD_SEG6[2]/ ADC1_IN23/COMP2_INP/ COMP1_INP	I/O		**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23 / Comparator 2 positive input / Comparator 1 positive input
47	-	-	PE6/LCD_SEG26[2]/ PVD_IN	I/O		**X**	X	X	HS	X	X	**Port E6**	LCD segment 26/PVD_IN
48	-	-	PE7/LCD_SEG27[2]	I/O		**X**	X	X	HS	X	X	**Port E7**	LCD segment 27
32	-	-	PF0/ADC1_IN24/ DAC_OUT	I/O		**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC_OUT
13	9	-	VLCD[2]	S								LCD booster external capacitor	
13	-	-	Reserved[5]									Reserved. Must be tied to V_{DD}	
10	-	-	V_{DD}	S								Digital power supply	
11	-	-	V_{DDA}	S								Analog supply voltage	
12	-	-	V_{REF+}	S								ADC1 and DAC positive voltage reference	

Table 4. STM8L15x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
VFQFPN48 and LQFP48	WFQFPN32	WFQFPN28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	8	7	$V_{DD}/V_{DDA}/V_{REF+}$	S								Digital power supply / Analog supply voltage / ADC1 positive voltage reference	
9	7	6	$V_{SS}/V_{SSA}/V_{REF-}$	S								I/O ground / Analog ground voltage / ADC1 negative voltage reference	
39	-	-	V_{DDIO}	S								IOs supply voltage	
40	-	-	V_{SSIO}	S								IOs ground voltage	
1	32	28	PA0/*[USART1_CK]*(3)/ SWIM/BEEP/IR_TIM (6)	I/O		**X**	X	X	HS (6)	X	X	**Port A0**	*[USART1 synchronous clock]*(3) / SWIM input and output / Beep output / Infrared Timer output

1. When the PA1/NRST pin is used as general purpose (PA1), it can be configured only as output push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15x reference manual (RM0031).
2. Available on STM8L152xx devices only.
3. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented).
5. Available on STM8L151xx devices only.
6. High Sink LED driver capability available on PA0.

4.1 System configuration options

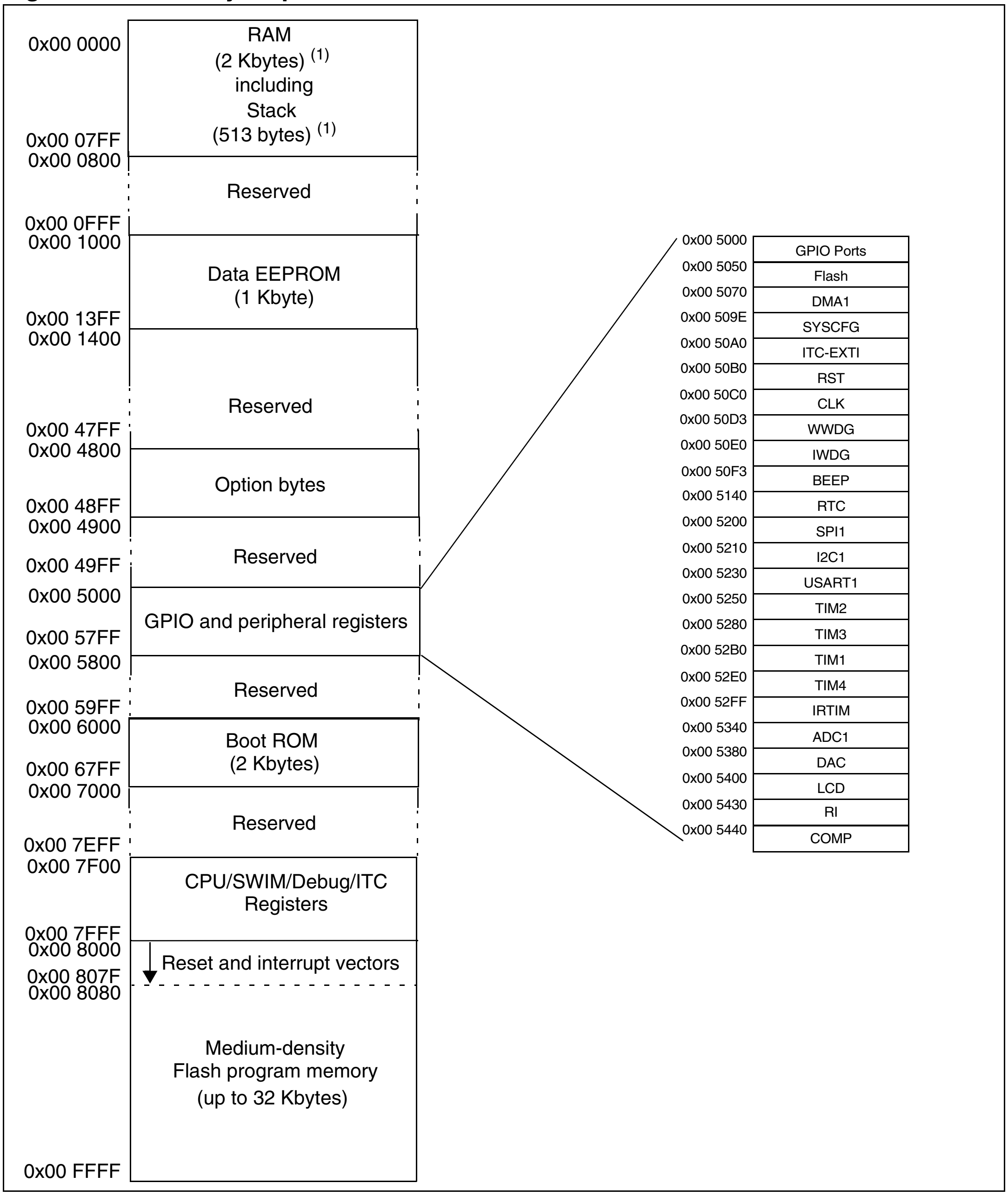
As shown in *Table 4: STM8L15x pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the " Routing interface (RI) and system configuration controller" section in the STM8L15xxx reference manual (RM0031).

5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 8*.

Figure 8. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

Table 5. Flash and RAM boundary addresses

Memory area	Size	Start Address	End address
RAM	2 Kbytes	0x00 0000	0x00 07FF
Flash program memory	16 Kbytes	0x00 8000	0x00 BFFF
	32 Kbytes	0x00 8000	0x00 FFFF

5.2 Register map

Table 6. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0x00
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0x00
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0x00
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0x00
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0x00
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00

Table 6. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0x00
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

Table 7. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 501E to 0x00 5049	Reserved area (44 bytes)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5065 to 0x00 506F	Reserved area (11 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 bytes)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00
0x00 507D to 0x00 507E		Reserved area (2 bytes)		
0x00 507F		DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083		DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5084	DMA1	Reserved area (1 byte)		
0x00 5085		DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088		Reserved area (2 bytes)		
0x00 5089		DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092		Reserved area (2 bytes)		
0x00 5093		DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		Reserved area (1 byte)		
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509D		Reserved area (3 bytes)		
0x00 509E	SYSCFG	SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF	External interrupt port select register	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_DIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00
0x00 50C2		CLK_ICKR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x00
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0bxxxx0000
0x00 50CA		CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0x00
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11100x

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50D0 to 0x00 50D2	Reserved area (3 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0x
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 bytes)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to 0x00 513F	Reserved area (76 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5140	RTC	RTC_TR1	Time register 1	0x00
0x00 5141		RTC_TR2	Time register 2	0x00
0x00 5142		RTC_TR3	Time register 3	0x00
0x00 5143		Reserved area (1 byte)		
0x00 5144		RTC_DR1	Date register 1	0x00
0x00 5145		RTC_DR2	Date register 2	0x00
0x00 5146		RTC_DR3	Date register 3	0x00
0x00 5147		Reserved area (1 byte)		
0x00 5148		RTC_CR1	Control register 1	0x00
0x00 5149		RTC_CR2	Control register 2	0x00
0x00 514A		RTC_CR3	Control register 3	0x00
0x00 514B		Reserved area (1 byte)		
0x00 514C		RTC_ISR1	Initialization and status register 1	0x00
0x00 514D		RTC_ISR2	Initialization and Status register 2	0x00
0x00 514E 0x00 514F		Reserved area (2 bytes)		
0x00 5150		RTC_SPRERH	Synchronous prescaler register high	-
0x00 5151		RTC_SPRERL	Synchronous prescaler register low	-
0x00 5152		RTC_APRER	Asynchronous prescaler register	-
0x00 5153		Reserved area (1 byte)		
0x00 5154		RTC_WUTRH	Wakeup timer register high	-
0x00 5155		RTC_WUTRL	Wakeup timer register low	-
0x00 5156 to 0x00 5158		Reserved area (3 bytes)		
0x00 5159		RTC_WPR	Write protection register	0x00
0x00 515A 0x00 515B		Reserved area (2 bytes)		
0x00 515C		RTC_ALRMAR1	Alarm A register 1	0x00
0x00 515D		RTC_ALRMAR2	Alarm A register 2	0x00
0x00 515E		RTC_ALRMAR3	Alarm A register 3	0x00
0x00 515F		RTC_ALRMAR4	Alarm A register 4	0x00
0x00 5160 to 0x00 51FF	Reserved area (160 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5200	SPI1	SPI1_CR1	SPI1 control register 1	0x00
0x00 5201		SPI1_CR2	SPI1 control register 2	0x00
0x00 5202		SPI1_ICR	SPI1 interrupt control register	0x00
0x00 5203		SPI1_SR	SPI1 status register	0x02
0x00 5204		SPI1_DR	SPI1 data register	0x00
0x00 5205		SPI1_CRCPR	SPI1 CRC polynomial register	0x07
0x00 5206		SPI1_RXCRCR	SPI1 Rx CRC register	0x00
0x00 5207		SPI1_TXCRCR	SPI1 Tx CRC register	0x00
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C1	I2C1_CR1	I2C1 control register 1	0x00
0x00 5211		I2C1_CR2	I2C1 control register 2	0x00
0x00 5212		I2C1_FREQR	I2C1 frequency register	0x00
0x00 5213		I2C1_OARL	I2C1 own address register low	0x00
0x00 5214		I2C1_OARH	I2C1 own address register high	0x00
0x00 5215		Reserved (1 byte)		
0x00 5216		I2C1_DR	I2C1 data register	0x00
0x00 5217		I2C1_SR1	I2C1 status register 1	0x00
0x00 5218		I2C1_SR2	I2C1 status register 2	0x00
0x00 5219		I2C1_SR3	I2C1 status register 3	0x0x
0x00 521A		I2C1_ITR	I2C1 interrupt control register	0x00
0x00 521B		I2C1_CCRL	I2C1 clock control register low	0x00
0x00 521C		I2C1_CCRH	I2C1 clock control register high	0x00
0x00 521D		I2C1_TRISER	I2C1 TRISE register	0x02
0x00 521E		I2C1_PECR	I2C1 packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	USART1	USART1_SR	USART1 status register	0xC0
0x00 5231		USART1_DR	USART1 data register	undefined
0x00 5232		USART1_BRR1	USART1 baud rate register 1	0x00
0x00 5233		USART1_BRR2	USART1 baud rate register 2	0x00
0x00 5234		USART1_CR1	USART1 control register 1	0x00
0x00 5235		USART1_CR2	USART1 control register 2	0x00
0x00 5236		USART1_CR3	USART1 control register 3	0x00
0x00 5237		USART1_CR4	USART1 control register 4	0x00
0x00 5238		USART1_CR5	USART1 control register 5	0x00
0x00 5239		USART1_GTR	USART1 guard time register	0x00
0x00 523A		USART1_PSCR	USART1 prescaler register	0x00
0x00 523B to 0x00 524F	Reserved area (21 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5251		TIM2_CR2	TIM2 control register 2	0x00
0x00 5252		TIM2_SMCR	TIM2 Slave mode control register	0x00
0x00 5253		TIM2_ETR	TIM2 external trigger register	0x00
0x00 5254		TIM2_DER	TIM2 DMA1 request enable register	0x00
0x00 5255		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5256		TIM2_SR1	TIM2 status register 1	0x00
0x00 5257		TIM2_SR2	TIM2 status register 2	0x00
0x00 5258		TIM2_EGR	TIM2 event generation register	0x00
0x00 5259		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 525A		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 525B		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 525C		TIM2_CNTRH	TIM2 counter high	0x00
0x00 525D		TIM2_CNTRL	TIM2 counter low	0x00
0x00 525E		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 525F		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 5260		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5261		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5262		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5263		TIM2_CCR2H	TIM2 capture/compare register 2 high	0x00
0x00 5264		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5265		TIM2_BKR	TIM2 break register	0x00
0x00 5266		TIM2_OISR	TIM2 output idle state register	0x00
0x00 5267 to 0x00 527F	Reserved area (25 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 Slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_DER	TIM3 DMA1 request enable register	0x00
0x00 5285		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5286		TIM3_SR1	TIM3 status register 1	0x00
0x00 5287		TIM3_SR2	TIM3 status register 2	0x00
0x00 5288		TIM3_EGR	TIM3 event generation register	0x00
0x00 5289		TIM3_CCMR1	TIM3 Capture/Compare mode register 1	0x00
0x00 528A		TIM3_CCMR2	TIM3 Capture/Compare mode register 2	0x00
0x00 528B		TIM3_CCER1	TIM3 Capture/Compare enable register 1	0x00
0x00 528C		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528D		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528E		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528F		TIM3_ARRH	TIM3 Auto-reload register high	0xFF
0x00 5290		TIM3_ARRL	TIM3 Auto-reload register low	0xFF
0x00 5291		TIM3_CCR1H	TIM3 Capture/Compare register 1 high	0x00
0x00 5292		TIM3_CCR1L	TIM3 Capture/Compare register 1 low	0x00
0x00 5293		TIM3_CCR2H	TIM3 Capture/Compare register 2 high	0x00
0x00 5294		TIM3_CCR2L	TIM3 Capture/Compare register 2 low	0x00
0x00 5295		TIM3_BKR	TIM3 break register	0x00
0x00 5296		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5297 to 0x00 52AF	Reserved area (25 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52B0	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 52B1		TIM1_CR2	TIM1 control register 2	0x00
0x00 52B2		TIM1_SMCR	TIM1 Slave mode control register	0x00
0x00 52B3		TIM1_ETR	TIM1 external trigger register	0x00
0x00 52B4		TIM1_DER	TIM1 DMA1 request enable register	0x00
0x00 52B5		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 52B6		TIM1_SR1	TIM1 status register 1	0x00
0x00 52B7		TIM1_SR2	TIM1 status register 2	0x00
0x00 52B8		TIM1_EGR	TIM1 event generation register	0x00
0x00 52B9		TIM1_CCMR1	TIM1 Capture/Compare mode register 1	0x00
0x00 52BA		TIM1_CCMR2	TIM1 Capture/Compare mode register 2	0x00
0x00 52BB		TIM1_CCMR3	TIM1 Capture/Compare mode register 3	0x00
0x00 52BC		TIM1_CCMR4	TIM1 Capture/Compare mode register 4	0x00
0x00 52BD		TIM1_CCER1	TIM1 Capture/Compare enable register 1	0x00
0x00 52BE		TIM1_CCER2	TIM1 Capture/Compare enable register 2	0x00
0x00 52BF		TIM1_CNTRH	TIM1 counter high	0x00
0x00 52C0		TIM1_CNTRL	TIM1 counter low	0x00
0x00 52C1		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 52C2		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 52C3		TIM1_ARRH	TIM1 Auto-reload register high	0xFF
0x00 52C4		TIM1_ARRL	TIM1 Auto-reload register low	0xFF
0x00 52C5		TIM1_RCR	TIM1 Repetition counter register	0x00
0x00 52C6		TIM1_CCR1H	TIM1 Capture/Compare register 1 high	0x00
0x00 52C7		TIM1_CCR1L	TIM1 Capture/Compare register 1 low	0x00
0x00 52C8		TIM1_CCR2H	TIM1 Capture/Compare register 2 high	0x00
0x00 52C9		TIM1_CCR2L	TIM1 Capture/Compare register 2 low	0x00
0x00 52CA		TIM1_CCR3H	TIM1 Capture/Compare register 3 high	0x00
0x00 52CB		TIM1_CCR3L	TIM1 Capture/Compare register 3 low	0x00
0x00 52CC		TIM1_CCR4H	TIM1 Capture/Compare register 4 high	0x00
0x00 52CD		TIM1_CCR4L	TIM1 Capture/Compare register 4 low	0x00
0x00 52CE		TIM1_BKR	TIM1 break register	0x00
0x00 52CF		TIM1_DTR	TIM1 dead-time register	0x00
0x00 52D0		TIM1_OISR	TIM1 output idle state register	0x00
0x00 52D1		TIM1_DCR1	DMA1 control register 1	

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52D2		TIM1_DCR2	TIM1 DMA1 control register 2	0x00
0x00 52D3		TIM1_DMA1R	TIM1 DMA1 address for burst mode	0x00
0x00 52D4 to 0x00 52DF	Reserved area (12 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 bytes)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5300 to 0x00 533F	Reserved area (64 bytes)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 534E	ADC1	ADC1_TRIGR1	ADC1 trigger disable 1	0x00
0x00 534F		ADC1_TRIGR2	ADC1 trigger disable 2	0x00
0x00 5350		ADC1_TRIGR3	ADC1 trigger disable 3	0x00
0x00 5351		ADC1_TRIGR4	ADC1 trigger disable 4	0x00
0x00 5352 to 0x00 537F	Reserved area (46 bytes)			
0x00 5380	DAC	DAC_CR1	DAC control register 1	0x00
0x00 5381		DAC_CR2	DAC control register 2	0x00
0x00 5382 to 0x00 5383		Reserved area (2 bytes)		
0x00 5384		DAC_SWTRIGR	DAC software trigger register	0x00
0x00 5385		DAC_SR	DAC status register	0x00
0x00 5386 to 0x00 5387		Reserved area (2 bytes)		
0x00 5388		DAC_RDHRH	DAC right aligned data holding register high	0x00
0x00 5389		DAC_RDHRL	DAC right aligned data holding register low	0x00
0x00 538A to 0x00 538B		Reserved area (2 bytes)		
0x00 538C		DAC_LDHRH	DAC left aligned data holding register high	0x00
0x00 538D		DAC_LDHRL	DAC left aligned data holding register low	0x00
0x00 538E to 0x00 538F		Reserved area (2 bytes)		
0x00 5390		DAC_DHR8	DAC 8-bit data holding register	0x00
0x00 5391 to 0x00 53AB		Reserved area (27 bytes)		
0x00 53AC		DAC_DORH	DAC data output register high	0x00
0x00 53AD		DAC_DORL	DAC data output register low	0x00
0x00 53AE to 0x00 53FF	Reserved area (82 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	LCD	LCD_CR1	LCD control register 1	0x00
0x00 5401		LCD_CR2	LCD control register 2	0x00
0x00 5402		LCD_CR3	LCD control register 3	0x00
0x00 5403		LCD_FRQ	LCD frequency selection register	0x00
0x00 5404		LCD_PM0	LCD Port mask register 0	0x00
0x00 5405		LCD_PM1	LCD Port mask register 1	0x00
0x00 5406		LCD_PM2	LCD Port mask register 2	0x00
0x00 5407		LCD_PM3	LCD Port mask register 3	0x00
0x00 5408 to 0x00 540B	LCD	Reserved area (4 bytes)		
0x00 540C		LCD_RAM0	LCD display memory 0	0x00
0x00 540D		LCD_RAM1	LCD display memory 1	0x00
0x00 540E		LCD_RAM2	LCD display memory 2	0x00
0x00 540F		LCD_RAM3	LCD display memory 3	0x00
0x00 5410		LCD_RAM4	LCD display memory 4	0x00
0x00 5411		LCD_RAM5	LCD display memory 5	0x00
0x00 5412		LCD_RAM6	LCD display memory 6	0x00
0x00 5413		LCD_RAM7	LCD display memory 7	0x00
0x00 5414		LCD_RAM8	LCD display memory 8	0x00
0x00 5415		LCD_RAM9	LCD display memory 9	0x00
0x00 5416		LCD_RAM10	LCD display memory 10	0x00
0x00 5417		LCD_RAM11	LCD display memory 11	0x00
0x00 5418		LCD_RAM12	LCD display memory 12	0x00
0x00 5419		LCD_RAM13	LCD display memory 13	0x00
0x00 541A to 0x00 542F	Reserved area (22 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5430	RI	Reserved area (1 byte)		0x00
0x00 5431		RI_ICR1	Timer input capture routing register 1	0x00
0x00 5432		RI_ICR2	Timer input capture routing register 2	0x00
0x00 5433		RI_IOIR1	I/O input register 1	undefined
0x00 5434		RI_IOIR2	I/O input register 2	undefined
0x00 5435		RI_IOIR3	I/O input register 3	undefined
0x00 5436		RI_IOCMR1	I/O control mode register 1	0x00
0x00 5437		RI_IOCMR3	I/O control mode register 2	0x00
0x00 5438		RI_IOCMR3	I/O control mode register 3	0x00
0x00 5439		RI_IOSR1	I/O switch register 1	0x00
0x00 543A		RI_IOSR2	I/O switch register 2	0x00
0x00 543B		RI_IOSR3	I/O switch register 3	0x00
0x00 543C		Reserved area (1 byte)		0x3F
0x00 543D		RI_ASCR1	Analog switch register 1	0x00
0x00 543E		RI_ASCR2	Analog switch register 2	0x00
0x00 543F		RI_RCR	Resistor control register 1	0x00
0x00 5440	COMP	COMP_CSR1	Comparator control and status register 1	0x00
0x00 5441		COMP_CSR2	Comparator control and status register 2	0x00
0x00 5442		COMP_CSR3	Comparator control and status register 3	0x00
0x00 5443		COMP_CSR4	Comparator control and status register 4	0x00
0x00 5444		COMP_CSR5	Comparator control and status register 5	0x00

Table 8. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register Label	Register Name	Reset Status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	CPU	Reserved area (85 bytes)		
0x00 7F60		CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC-SPR	ITC_SPR1	Interrupt Software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt Software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt Software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt Software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt Software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt Software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt Software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt Software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			

Table 8. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register Label	Register Name	Reset Status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM Debug module control register 1	0x00
0x00 7F97		DM_CR2	DM Debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only

6 Interrupt vector mapping

Table 9. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
	TRAP	Software interrupt	-	-	-	-	0x00 8004
1	FLASH	EOP/WR_PG_DIS	-	-	Yes	Yes(2)	0x00 800C
2	DMA1 0/1	DMA1 channels 0/1	-	-	Yes	Yes(2)	0x00 8010
3	DMA1 2/3	DMA1 channels 2/3	-	-	Yes	Yes(2)	0x00 8014
4	RTC	RTC alarm interrupt	Yes	Yes	Yes	Yes	0x00 8018
5	EXTI E/F/PVD(3)	PortE/F interrupt/PVD interrupt	Yes	Yes	Yes	Yes(2)	0x00 801C
6	EXTIB	External interrupt port B	Yes	Yes	Yes	Yes(2)	0x00 8020
7	EXTID	External interrupt port D	Yes	Yes	Yes	Yes(2)	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes(2)	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes(2)	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes(2)	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes(2)	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes(2)	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes(2)	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes(2)	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes(2)	0x00 8044
16	LCD	LCD interrupt	-	-	Yes	Yes	0x00 8048
17	CLK/ TIM1/ DAC	System clock switch/CSS interrupt/TIM1 Break/DAC	-	-	Yes	Yes	0x00 804C
18	COMP /ADC1	Comparator interrupt/ADC1	Yes	Yes	Yes	Yes(2)	0x00 8050
19	TIM2	Update /Overflow/Trigger/Break	-	-	Yes	Yes(2)	0x00 8054
20	TIM2	Capture/Compare	-	-	Yes	Yes(2)	0x00 8058
21	TIM3	Update /Overflow/Trigger/Break	-	-	Yes	Yes(2)	0x00 805C
22	TIM3	Capture/Compare	-	-	Yes	Yes(2)	0x00 8060
23	TIM1	Update /Overflow/Trigger/ COM	-	-	-	Yes(2)	0x00 8064
24	TIM1	Capture/Compare	-	-	-	Yes(2)	0x00 8068

Table 9. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
25	TIM4	Update/overflow/trigger	-	-	Yes	Yes(2)	0x00 806C
26	SPI1	End of Transfer	Yes	Yes	Yes	Yes(2)	0x00 8070
27	USART 1	Transmission complete/transmit data register empty	-	-	Yes	Yes(2)	0x00 8074
28	USART 1	Receive Register Data full/overrun/idle line detected/parity error	-	-	Yes	Yes(2)	0x00 8078
29	I^2C1	I^2C1 interrupt(4)	Yes	Yes	Yes	Yes(2)	0x00 807C

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode.
2. In WFE mode, this interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When this interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
3. The interrupt from PVD is logically OR-ed with Port E and F interrupts. Register EXTI_CONF allows to select between Port E and Port F interrupt (see *External interrupt port select register (EXTI_CONF)* in the RM0031).
4. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 10* for details on option byte addresses.

The option bytes can also be modified 'on the fly' by the application in IAP mode, except for the ROP, UBC and PCODESIZE values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x Flash programming manual (PM0051) and STM8 SWIM and Debug Manual (UM0320) for information on SWIM programming procedures.

Table 10. Option byte addresses

<table>
<tr><th rowspan="2">Addr.</th><th rowspan="2">Option name</th><th rowspan="2">Option byte No.</th><th colspan="8">Option bits</th><th rowspan="2">Factory default setting</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>00 4800</td><td>Read-out protection (ROP)</td><td>OPT1</td><td colspan="8">ROP[7:0]</td><td>0x00</td></tr>
<tr><td>00 4802</td><td>UBC(User Boot code size)</td><td>OPT3</td><td colspan="8">UBC[7:0]</td><td>0x00</td></tr>
<tr><td>00 4807</td><td>PCODESIZE</td><td>OPT8</td><td colspan="8">PCODE[7:0]</td><td>0x00</td></tr>
<tr><td>00 4808</td><td>Independent watchdog option</td><td>OPT5 [3:0]</td><td colspan="4">Reserved</td><td>WWDG _HALT</td><td>WWDG _HW</td><td>IWDG _HALT</td><td>IWDG _HW</td><td>0x00</td></tr>
<tr><td>00 4809</td><td>Number of stabilization clock cycles for HSE and LSE oscillators</td><td>OPT10</td><td colspan="4">Reserved</td><td colspan="4">HSECNT[1:0]
LSECNT[1:0]</td><td>0x00</td></tr>
<tr><td>00 480A</td><td>Brownout reset (BOR)</td><td>OPT11 [3:0]</td><td colspan="4">Reserved</td><td colspan="3">BOR_TH</td><td>BOR_ ON</td><td>0x01</td></tr>
</table>

Table 11. Option byte description

Option byte No.	Option description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Enable Readout protection (write access via SWIM protocol) Refer to Readout protection section in the STM8L15x reference manual (RM0031).
OPT1	**UBC[7:0]** Size of the user boot code area 0x00: no UBC 0x01: the UBC contains only the interrupt vectors. 0x02: Page 0 and 1 reserved for the UBC and read/write protected. Page 0 contains only the interrupt vectors. 0x03 - Page 0 to 3 reserved for UBC, memory write-protected ≥ 0xFF - Page 0 to 255 reserved for UBC, memory write-protected Refer to User boot code section in the STM8L15x reference manual (RM0031).
OPT2	**PCODESIZE[7:0]** Size of the proprietary code area 0x00: no proprietary code area 0x02: Page 0 and 1 reserved for the proprietary code and read/write protected. Page 0 contains only the interrupt vectors. ≥ 0xFF - Page 0 o 254 reserved for the proprietary code. Only page 1 to 254 are read/write protected. Page 255 is always left free. Refer to Proprietary code area (PCODE) section in the STM8L reference manual (RM0013) for more details.
OPT3	**IWDG_HW:** Independent watchdog 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: Independent window watchdog reset on Halt/Active-halt 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode
	WWDG_HW: Window watchdog 0: Window watchdog activated by software 1: Window watchdog activated by hardware
	WWDG_HALT: Window window watchdog reset on Halt/Active-halt 0: Window watchdog stopped in Halt mode 1: Window watchdog generates a reset when MCU enters Halt mode
OPT4	**HSECNT**: Number of HSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles
	LSECNT: Number of LSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles

Table 11. Option byte description (continued)

Option byte No.	Option description
OPT5	**BOR_ON**: 0 - Brownout reset off 1 - Brownout reset on
	BOR_TH[3:1]: Brownout reset thresholds. Refer to *Table 16* for details on the thresholds according to the value of BOR_TH bits.

8 Electrical parameters

8.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

8.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

8.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

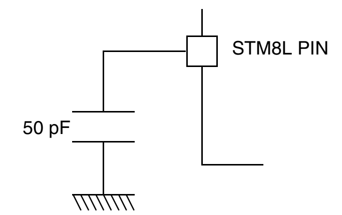
8.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

8.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

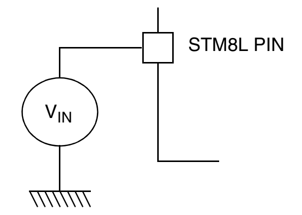
Figure 9. Pin loading conditions



8.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



8.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 12. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	4.0	V
V_{IN}	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS}-0.3	V_{DD} + 4.6	V
	Input voltage on FT pins (PA7 and PE0)	V_{SS}-0.3	V_{DD} + 4.6	V
	Input voltage on any other pin (2)	V_{SS}-0.3	4.6	V
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 90*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply.

2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} max imum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by V_{IN}>V_{DD} while a negative injection is induced by V_{IN}<V_{SS}. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected.

Table 13. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ (1)	Injected current on any pin (2)	± 5	
$\Sigma I_{INJ(PIN)}$ (1)	Total injected current (sum of all I/O and control pins) (2)	± 25	

1. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected.
2. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 14. Thermal characteristics

Symbol	Ratings	Min	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

8.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

8.3.1 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SYSCLK}(1)	System clock frequency	1.65 V ≤V_{DD} < 3.6 V		0	16	MHz
V_{DD}	Standard operating voltage			1.65(2)	3.6	V
V_{DDA}	Analog operating voltage	ADC not used	Must be at the same potential as V_{DD}	1.65(2)	3.6	V
		ADC used		1.8	3.6	V
P_D(3)	Power dissipation at T_A= 85 °C for suffix 6 devices	VFQFPN48 (4)			TBD	mW
		LQFP48			TBD	
		WFQFPN32 (5)			TBD	
		LQFP32			TBD	
		WFQFPN28 (6)			TBD	
	Power dissipation at T_A= 125 °C for suffix 3 devices	VFQFPN48(4)			TBD	
		LQFP48			TBD	
		WFQFPN32(5)			TBD	
		LQFP32			TBD	
		WFQFPN28(6)			TBD	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (6 suffix version)		-40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (3 suffix version)		-40	125	
T_J	Junction temperature range	-40 °C ≤T_A < 85 °C (6 suffix version)		-40	105	°C
		-40 °C≤ T_A < 125 °C (3 suffix version)		-40	130	

1. $f_{SYSCLK} = f_{CPU}$
2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in "Thermal characteristics" table.
4. VFQFPN48 package is used in the sampling phase. In the production phase, the UFQFPN48 package will be used (with a thickness equal to 0.6 mm).
5. WFQFPN32 package is used in the sampling phase. In the production phase, the UFQFPN32 package will be used (with a thickness equal to 0.6 mm).
6. WFQFPN28 package is used in the sampling phase. In the production phase, the UFQFPN28 package will be used (with a thickness equal to 0.6 mm).

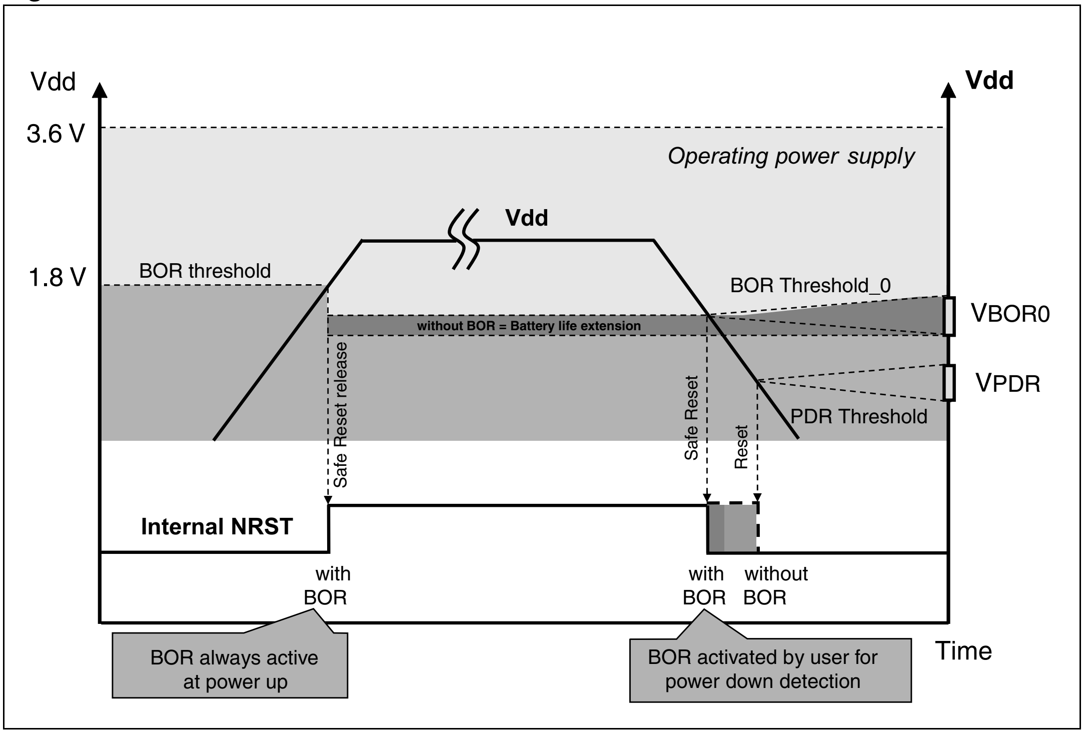
8.3.2 Power-up / power-down operating conditions

Table 16. Operating conditions at power-up / power-down (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate		0(2)		∞	µs/V
	V_{DD} fall time rate		0(2)		∞	
t_{TEMP}	Reset release delay	V_{DD} rising		TBD	TBD	ms
V_{PDR}	Power-down reset threshold	Falling edge	TBD	1.5	TBD	V
V_{BOR0}	Brown-out reset threshold 0 (BOR_TH[2:0]=000)	Falling edge	TBD	1.7	TBD	
		Rising edge	TBD	1.76	TBD	
V_{BOR1}	Brown-out reset threshold 1 (BOR_TH[2:0]=001)	Falling edge	TBD	1.93	TBD	
		Rising edge	TBD	2.03	TBD	
V_{BOR2}	Brown-out reset threshold 2 (BOR_TH[2:0]=010)	Falling edge	TBD	2.30	TBD	
		Rising edge	TBD	2.41	TBD	
V_{BOR3}	Brown-out reset threshold 3 (BOR_TH[2:0]=011)	Falling edge	TBD	2.55	TBD	
		Rising edge	TBD	2.66	TBD	
V_{BOR4}	Brown-out reset threshold 4 (BOR_TH[2:0]=100)	Falling edge	TBD	2.80	TBD	
		Rising edge	TBD	2.90	TBD	
V_{PVD0}	PVD threshold 0	Falling edge	TBD	1.85	TBD	
		Rising edge	TBD	1.94	TBD	
V_{PVD1}	PVD threshold 1	Falling edge	TBD	2.04	TBD	
		Rising edge	TBD	2.14	TBD	
V_{PVD2}	PVD threshold 2	Falling edge	TBD	2.24	TBD	
		Rising edge	TBD	2.34	TBD	
V_{PVD3}	PVD threshold 3	Falling edge	TBD	2.44	TBD	
		Rising edge	TBD	2.54	TBD	
V_{PVD4}	PVD threshold 4	Falling edge	TBD	2.64	TBD	
		Rising edge	TBD	2.74	TBD	
V_{PVD5}	PVD threshold 5	Falling edge	TBD	2.83	TBD	
		Rising edge	TBD	2.94	TBD	
V_{PVD6}	PVD threshold 6	Falling edge	TBD	3.05	TBD	
		Rising edge	TBD	3.15	TBD	

1. Based on characterization results, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Figure 11. POR/BOR thresholds



8.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Table 17. Total current consumption in Run mode(1)

Symbol	Parameter	Conditions(2)			Typ	Max 55°C	Max 85 °C (3)	Max 105 °C (4)	Max 125 °C (4)	Unit
$I_{DD(RUN)}$	Supply current in run mode(5)	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)	f_{CPU} = 125 kHz	0.5	TBD	TBD	TBD	TBD	mA
				f_{CPU} = 1 MHz	0.6	TBD	TBD	TBD	TBD	
				f_{CPU} = 4 MHz	0.9	TBD	TBD	TBD	TBD	
				f_{CPU} = 8 MHz	1.3	TBD	TBD	TBD	TBD	
				f_{CPU} = 16 MHz	2	TBD	TBD	TBD	TBD	
			HSE external clock (16 MHz)	f_{CPU} = 125 kHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 1 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 4 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 8 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 16 MHz	TBD	TBD	TBD (6)	TBD	TBD (6)	
			LSI RC osc. (typ. 38 kHz)	f_{CPU} = LSI	TBD					
			LSE external clock (32.768 kHz)	f_{CPU} = LSE	TBD	TBD	TBD (6)	TBD	TBD (6)	

Table 17. Total current consumption in Run mode(1) (continued)

Symbol	Parameter	Conditions(2)			Typ	Max 55°C	Max 85 °C (3)	Max 105 °C (4)	Max 125 °C (4)	Unit
$I_{DD(RUN)}$	Supply current in run mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI RC osc.	f_{CPU} = 125 kHz	TBD	TBD	TBD	TBD	TBD	mA
				f_{CPU} = 1 MHz	0.7	TBD	TBD	TBD	TBD	
				f_{CPU} = 4 MHz	1.4	TBD	TBD	TBD	TBD	
				f_{CPU} = 8 MHz	2.3	TBD	TBD	TBD	TBD	
				f_{CPU} = 16 MHz	TBD	TBD	TBD	TBD	TBD	
			HSE external clock (16 MHz)	f_{CPU} = 125 kHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 1 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 4 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 8 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 16 MHz	TBD	TBD	TBD	TBD	TBD	
			LSI RC osc.	f_{CPU} = LSI	TBD					
			LSE external clock (32.768 kHz)	f_{CPU} = LSE	TBD	TBD	TBD	TBD	TBD	

1. Based on characterization results, unless otherwise specified
2. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc. , $f_{CPU}=f_{SYSCLK}$
3. For devices with suffix 6.
4. For devices with suffix 3.
5. CPU executing typical data processing
6. Data guaranteed, each individual device tested in production.

Table 18. Total current consumption in Wait mode(1)

Symbol	Parameter	Conditions(2)			Typ	Max 55°C	Max 85 °C (3)	Max 105 °C (4)	Max 125 °C (4)	Unit
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from RAM with Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	430	TBD	TBD	TBD	TBD	µA
				f_{CPU} = 1 MHz	450	TBD	TBD	TBD	TBD	
				f_{CPU} = 4 MHz	515	TBD	TBD	TBD	TBD	
				f_{CPU} = 8 MHz	600	TBD	TBD	TBD	TBD	
				f_{CPU} = 16 MHz	770	TBD	TBD	TBD	TBD	
			HSE crystal oscillator (16 MHz)	f_{CPU} = 125 kHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 1 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 4 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 8 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 16 MHz	TBD	TBD	TBD	TBD	TBD	
			LSI	f_{CPU} = LSI	32					
			LSE crystal oscillator (32.768 kHz)	f_{CPU} = LSE	TBD	TBD	TBD	TBD	TBD	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	480	TBD	TBD	TBD	TBD	µA
				f_{CPU} = 1 MHz	500	TBD	TBD	TBD	TBD	
				f_{CPU} = 4 MHz	560	TBD	TBD	TBD	TBD	
				f_{CPU} = 8 MHz	660	TBD	TBD	TBD	TBD	
				f_{CPU} = 16 MHz	840	TBD	TBD	TBD	TBD	
			HSE crystal oscillator (16 MHz)	f_{CPU} = 125 kHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 1 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 4 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 8 MHz	TBD	TBD	TBD	TBD	TBD	
				f_{CPU} = 16 MHz	TBD	TBD	TBD	TBD	TBD	
			LSI	f_{CPU} = LSI	83					
			LSE crystal oscillator (32.768 kHz)	f_{CPU} = LSE	TBD	TBD	TBD	TBD	TBD	

1. Based on characterization results, unless specified
2. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc. , $f_{CPU} = f_{SYSCLK}$
3. For temperature range 6.
4. For temperature range 3.

Table 19. Total current consumption and timing in Low power run mode at V_{DD} = 1.65 V to 3.6 V [1][2]

Symbol	Parameter	Conditions			Typ	Max	Unit
$I_{DD(LPR)}$	Supply current in Low power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.4		µA
				T_A = 55 °C	TBD		
				T_A = 85 °C	6.8		
				T_A = 105 °C	9.2		
				T_A = 125 °C	13.4		
			with TIM2 active[3]	T_A = -40 °C to 25 °C	5.7		
				T_A = 55 °C	TBD		
				T_A = 85 °C	7.2		
				T_A = 105 °C	9.4		
				T_A = 125 °C	13.8		
		LSE external clock (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	TBD	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
				T_A = 125 °C	TBD	TBD	
			with TIM2 active [3]	T_A = -40 °C to 25 °C	TBD	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
				T_A = 125 °C	TBD	TBD	

1. No floating I/Os
2. Based on characterization results, unless otherwise specified
3. Timer 2 clock enabled and counter running

Table 20. Total current consumption in Low power wait mode at V_{DD} = 1.65 V to 3.6 V [1][2]

Symbol	Parameter	Conditions			Typ	Max	Unit
$I_{DD(LPW)}$	Supply current in Low power wait mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	3		µA
				T_A = 55 °C	TBD		
				T_A = 85 °C	4.4		
				T_A = 105 °C	6.7		
				T_A = 125 °C	11		
			with TIM2 active[3]	T_A = -40 °C to 25 °C	3.4		
				T_A = 55 °C	TBD		
				T_A = 85 °C	4.8		
				T_A = 105 °C	7		
				T_A = 125 °C	11.3		
		LSE external clock (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	TBD	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
				T_A = 125 °C	TBD	TBD	
			with TIM2 active [3]	T_A = -40 °C to 25 °C	TBD	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
				T_A = 125 °C	TBD	TBD	

1. No floating I/Os.
2. Based on characterization results, unless otherwise specified.
3. Timer 2 clock enabled and counter running.

Table 21. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V (1)(2)

Symbol	Parameter	Conditions			Typ	Max	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC (at 38 kHz)	LCD OFF	T_A = -40 °C to 25 °C	TBD		µA
				T_A = 55 °C	TBD		
				T_A = 85 °C	TBD		
				T_A = 105 °C	TBD		
				T_A = 125 °C	TBD		
			LCD ON (static duty) (3)	T_A = -40 °C to 25 °C	TBD		
				T_A = 55 °C	TBD		
				T_A = 85 °C	TBD		
				T_A = 105 °C	TBD		
				T_A = 125 °C	TBD		
			LCD ON (1/4 duty) (4)	T_A = -40 °C to 25 °C	TBD		
				T_A = 55 °C	TBD		
				T_A = 85 °C	TBD		
				T_A = 105 °C	TBD		
				T_A = 125 °C	TBD		
		LSE external clock (32.768 kHz)	LCD OFF	T_A = -40 °C to 25 °C	TBD	TBD	µA
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
				T_A = 125 °C	TBD	TBD	
			LCD ON (static duty) (3)	T_A = -40 °C to 25 °C	TBD	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
				T_A = 125 °C	TBD	TBD	
			LCD ON (1/4 duty) (4)	T_A = -40 °C to 25 °C	TBD	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
				T_A = 125 °C	TBD	TBD	
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode (using HSI)					TBD	mA

Table 21. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V [1][2] (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WU\_HSI(AH)}$ [5][6]	Wakeup time from Active-halt mode to Run mode (using HSI)		5	TBD	µs
$t_{WU\_LSI(AH)}$ [5][6]	Wakeup time from Active-halt mode to Run mode (using LSI)		TBD	TBD	µs

1. No floating I/O, unless otherwise specified.
2. Based on characterization results, unless otherwise specified.
3. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected.
4. LCD enabled with external VLCD, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.
6. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

Table 22. Total current consumption and timing in Halt mode at V_{DD} = 2 V [1][2]

Symbol	Parameter	Condition	Typ	Max	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (Ultra low power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	400	TBD	nA
		T_A = 55 °C	TBD	TBD[3]	
		T_A = 85 °C	TBD	TBD	
		T_A = 105 °C	TBD	TBD[3]	
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)		TBD		mA
$t_{WU\_HSI(Halt)}$ [4][5]	Wakeup time from Halt to Run mode (using HSI)		5	TBD	µs
$t_{WU\_LSI(Halt)}$ [4][5]	Wakeup time from Halt mode to Run mode (using LSI)		TBD	TBD	µs

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified
2. Based on characterization results, unless otherwise specified
3. Tested in production
4. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register
5. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}

Current consumption of on-chip peripherals

Table 23. Peripheral current consumption

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)		13	µA/MHz
$I_{DD(TIM2)}$	TIM2 supply current (1)		8	
$I_{DD(TIM3)}$	TIM3 supply current (1)		8	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (2)		6	
$I_{DD(SPI1)}$	SPI1 supply current (2)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (2)		5	
$I_{DD(DMA1)}$	DMA1 supply current		3	
$I_{DD(WWDG)}$	WWDG supply current		2	
$I_{DD(ALL)}$	Peripherals ON(3)		44	µA/MHz
$I_{DD(RTC)}$	RTC supply current when clocked by LSI		TBD	µA
	RTC supply current when clocked at 1 MHz		TBD	
$I_{DD(LCD)}$	LCD supply current when clocked at 32 kHz /2		TBD	
	LCD supply current when clocked at 1 MHz /2		TBD	
$I_{DD(ADC1)}$	ADC1 supply current(4)		1500	µA
$I_{DD(DAC)}$	DAC supply current(5)		370	
$I_{DD(COMP1)}$	Comparator 1 supply current(6)		0.160	
$I_{DD(COMP2)}$	Comparator 2 supply current(6)	Slow mode	2	
		Fast mode	5	
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (7)		2.8	
$I_{DD(IDWDG)}$	Independent watchdog supply current		TBD	

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, USART1, SPI1, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.
5. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of V_{DD} /2. DAC output is in high-impedance.
6. Data based on a differential I_{DD} measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
7. Including supply current of internal reference voltage.

8.3.4 Clock and timing characteristics

HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 24. HSE external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency(1)		1		16	MHz
V_{HSEH}(2)	OSC_IN input pin high level voltage		0.7 x V_{DD}		TBD	V
V_{HSEL}(2)	OSC_IN input pin low level voltage		V_{SS}		0.3 x V_{DD}	V
$C_{in(HSE)}$	OSC_IN input capacitance(1)			TBD		pF
I_{LEAK_HSE}	OSC_IN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	TBD		TBD	nA

1. Guarenteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

LSE external clock (LSEBYP=1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 25. LSE external clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency(1)	1	32.768	TBD	kHz
V_{LSEH}(2)	OSC32_IN input pin high level voltage	0.7 x V_{DD}		TBD	V
V_{LSEL}(2)	OSC32_IN input pin low level voltage	V_{SS}		0.3 x V_{DD}	V
$C_{in(HSE)}$	OSC32_IN input capacitance(1)		TBD		pF
I_{LEAK_HSE}	OSC32_IN input leakage current	TBD		TBD	nA

1. Guarenteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

HSE crystal/ceramic resonator oscillator

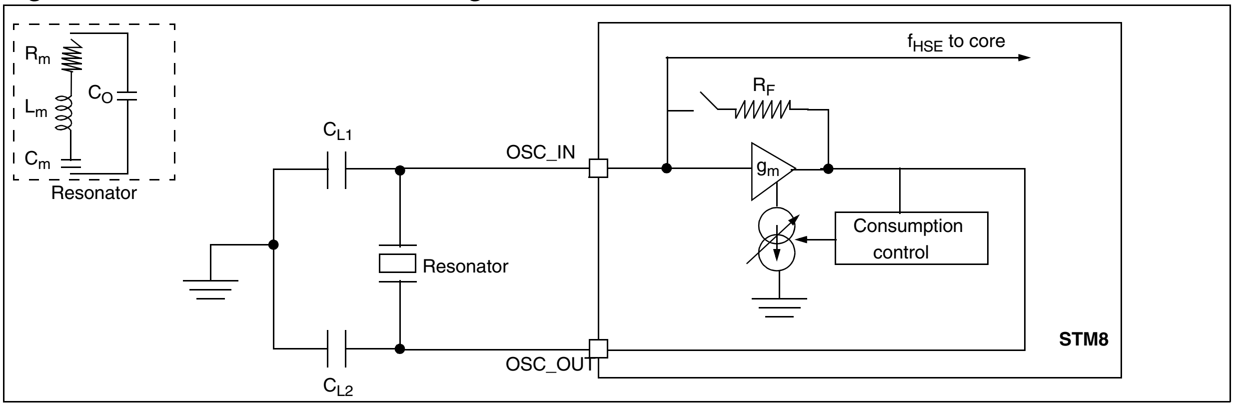
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 26. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High speed external oscillator frequency		1		16	MHz
R_F	Feedback resistor			TBD		kΩ
C(1)	Recommended load capacitance (2)			TBD		pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz			TBD (startup) TBD (stabilized)(3)	mA
		C = 10 pF, f_{OSC} =16 MHz			TBD (startup) TBD (stabilized)(3)	
g_m	Oscillator transconductance		3.5			mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized		1		ms

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 12. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification), L_m: Notional inductance (see crystal specification),
C_m: Notional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification),
$C_{L1}=C_{L2}=C$: Grounded external capacitance
$g_m >> g_{mcrit}$

LSE crystal/ceramic resonator oscillator

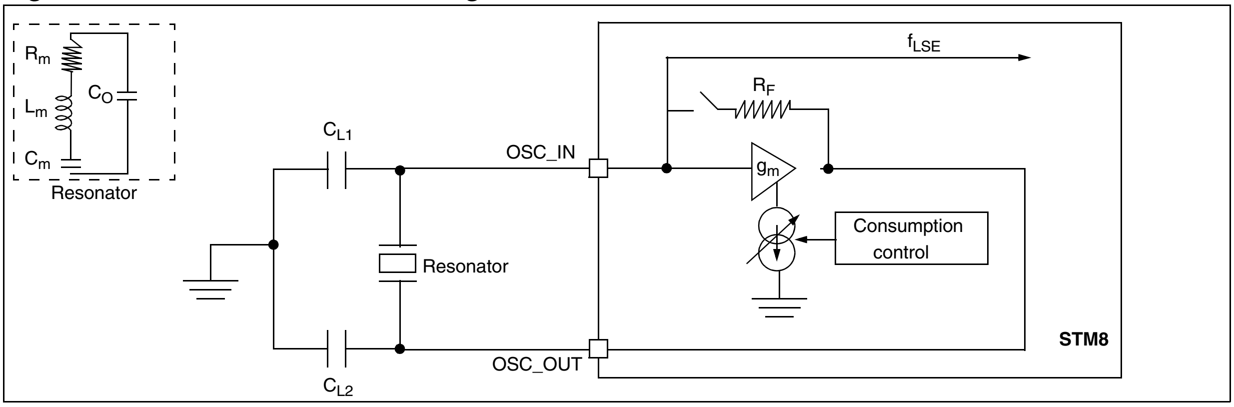
The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 27. LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency			32.768		kHz
R_F	Feedback resistor			TBD		kΩ
C(1)	Recommended load capacitance (2)			TBD		pF
$I_{DD(LSE)}$	LSE oscillator power consumption				TBD(3)	µA
g_m	Oscillator transconductance		TBD			µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized				ms

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 13. LSE oscillator circuit diagram



Internal clock sources

Subject to general operating conditions for V_{DD}, and T_A.

High speed internal RC oscillator (HSI)

Table 28. HSI oscillator characteristics [(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V		16		MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	-1 [(2)]		1 [(2)]	%
		V_{DD} = 3.0 V, 0 °C ≤ T_A ≤ 55 °C	-1.5 [(2)]		1.5 [(2)]	%
		V_{DD} = 3.0 V, -10 °C ≤ T_A ≤ 70 °C	-2 [(2)]		2 [(2)]	%
		V_{DD} = 3.0 V, -10 °C ≤ T_A ≤ 85 °C	-2.5 [(2)]		2[(2)]	%
		V_{DD} = 3.0 V, -10 °C ≤ T_A ≤ 125 °C	-4.5 [(2)]		2 [(2)]	%
		1.65 V ≤ V_{DD} ≤ 3.6 V, -40 °C ≤ T_A ≤ 125 °C	-4.5		3	%
TRIM	HSI user trim resolution	1.65 V ≤ V_{DD} ≤ 3.6 V, -40 °C ≤ T_A ≤ 125 °C		±0.4 [(2)]	±0.5	%
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)			3.7	7.4 [(2)]	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			100	140 [(2)]	µA

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.

Low speed internal RC oscillator (LSI)

Table 29. LSI oscillator characteristics [(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency		26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time			TBD	TBD[(2)]	µs
$I_{DD(LSI)}$	LSI oscillator frequency drift[(3)]	0 °C ≤ T_A ≤ 85 °C	-10		4	%

1. V_{DD} = 1.8 V to 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. This is a deviation for an individual part, once the initial frequency has been measured.

8.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 30. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.4			V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory

Table 31. Flash program memory

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65		3.6	V
t_{prog}	Programming time for 1 or 128 bytes (block) erase/write cycles (on programmed byte)				TBD	ms
	Programming time for 1 to 128 bytes (block) write cycles (on erased byte)				TBD	ms
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V		TBD		mA
		T_A=+25 °C, V_{DD} = 1.8 V		TBD		
t_{RET}	Data retention (program memory) after 10000 erase/write cycles at T_A=+85 °C	T_{RET}=+55 °C	TBD(1)			years
	Data retention (data memory) after 10000 erase/write cycles at T_A=+85 °C	T_{RET}=+55 °C	TBD(1)			
	Data retention (data memory) after 10000 erase/write cycles at T_A=+85 °C	T_{RET}=+85 °C	TBD(1)			
N_{RW}	Erase/write cycles (program memory)	See notes (1)(2)	TBD(1)			kcycles
	Erase/write cycles (data memory)	See notes (1)(3)	TBD(1) (4)			

1. Data based on characterization results, not tested in production.
2. Retention guaranteed after cycling is 10 years @ 55 °C.
3. Retention guaranteed after cycling is 1 year @ 55 °C.
4. Data based on characterization performed on the whole data memory.

8.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 32. I/O static characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS} -0.3		0.3 x V_{DD}	V
		Input voltage on FT pins (PA7 and PE0)	V_{SS} -0.3		0.3 x V_{DD}	
		Input voltage on any other pin	V_{SS} -0.3		0.3 x V_{DD}	
V_{IH}	Input high level voltage (2)	Input voltage on true open-drain pins (PC0 and PC1)	0.70 x V_{DD}		V_{DD}+3.6	V
		Input voltage on FT pins (PA7 and PE0)	0.70 x V_{DD}		V_{DD}+3.6	
		Input voltage on any other pin	0.70 x V_{DD}		V_{DDmax}+0.3	
V_{hys}	Schmitt trigger voltage hysteresis (3)	Standard I/Os		200		mV
		True open drain I/Os		250		
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	50 (5)	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200(5)	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200(5)	
R_{PU}	Weak pull-up equivalent resistor(6)	$V_{IN}=V_{SS}$	30	45	60	kΩ
C_{IO}(7)	I/O pin capacitance			5		pF

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. R_{PU} pull-up equivalent resistor based on a resistive transistor.
7. Data guaranteed by Design, not tested in production.

Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 33. Output driving current (standard ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Standard	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V		0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V		0.45	V
			I_{IO} = +10 mA, V_{DD} = 3.0 V		0.7	V
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45		V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45		V
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7		V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 34. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V		0.45	
			I_{IO} = +1 mA, V_{DD} = 1.8 V		0.45	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 35. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V		TBD	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

NRST pin

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

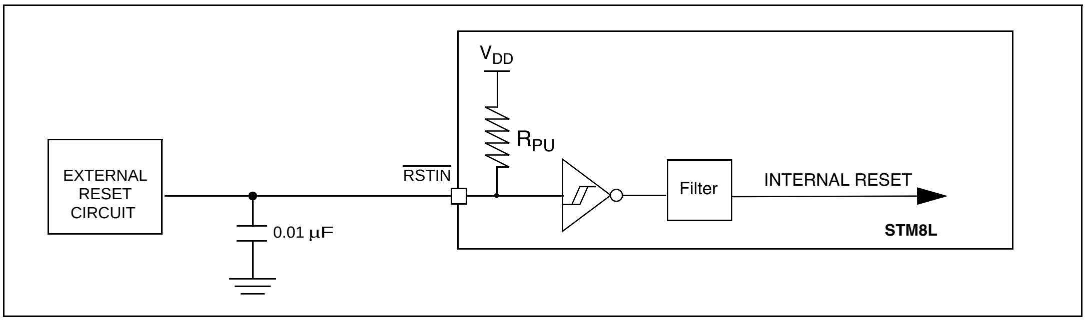
Table 36. $\overline{\text{NRST}}$ pin characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage [1]		V_{SS}		0.8	V
$V_{IH(NRST)}$	NRST Input high level voltage [1]		1.4		V_{DD}	
$V_{OL(NRST)}$	NRST Output low level voltage	I_{OL} = 2 mA			V_{DD}-0.8	
$R_{PU(NRST)}$	NRST Pull-up equivalent resistor [2]		30	45	60	kΩ
$V_{F(NRST)}$	NRST Input filtered pulse [3]				50	ns
$V_{NF(NRST)}$	NRST Input not filtered pulse [3]		300			

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor
3. Data guaranteed by design, not tested in production.

The reset network shown in *Figure 14* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 36*. Otherwise the reset is not taken into account internally.

Figure 14. Recommended NRST pin configuration



8.3.7 Communication interfaces

SPI1 - Serial peripheral interface

Unless otherwise specified, the parameters given in Table 37 are derived from tests performed under ambient temperature, f_{SYSCLK} frequency and V_{DD} supply voltage conditions summarized in Section 8.3.1. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 37. SPI1 characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	TBD	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x $1/f_{SYSCLK}$	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	TBD	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{SYSCLK} = 8 MHz, f_{SCK}= 4 MHz	TBD	TBD	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	TBD	-	
		Slave mode	TBD	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	TBD	-	
		Slave mode	TBD	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x $1/f_{SYSCLK}$	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	TBD	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	TBD	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	TBD	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	TBD	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	TBD	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 15. SPI timing diagram - slave mode and CPHA=0

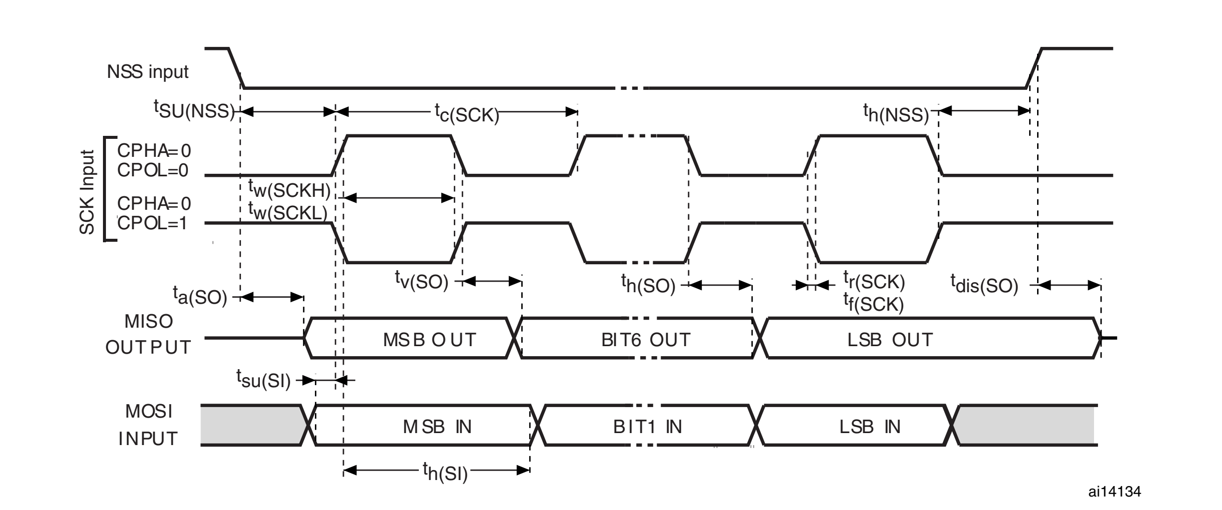
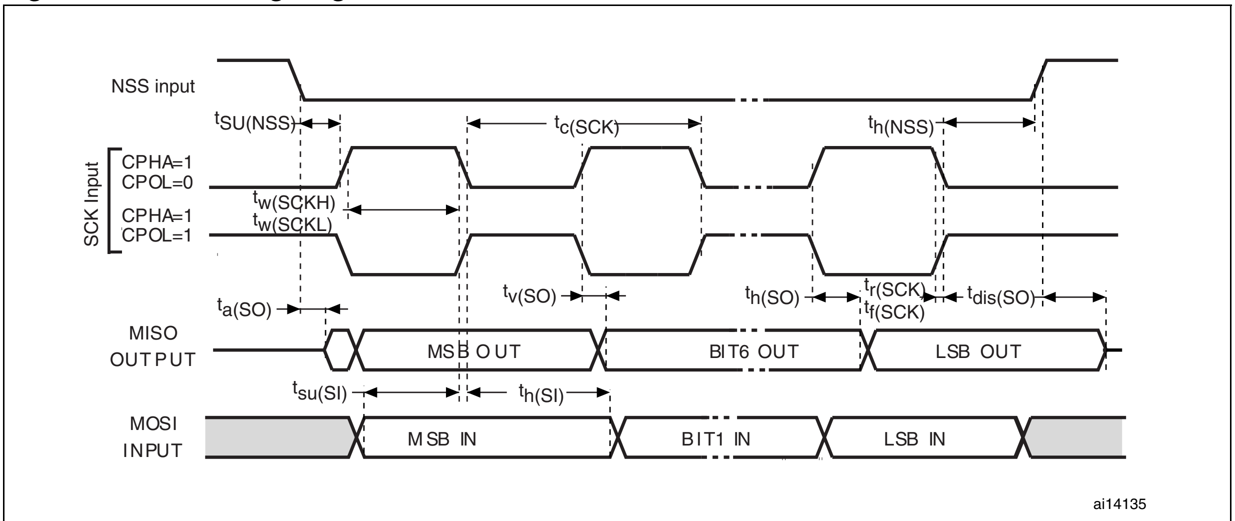
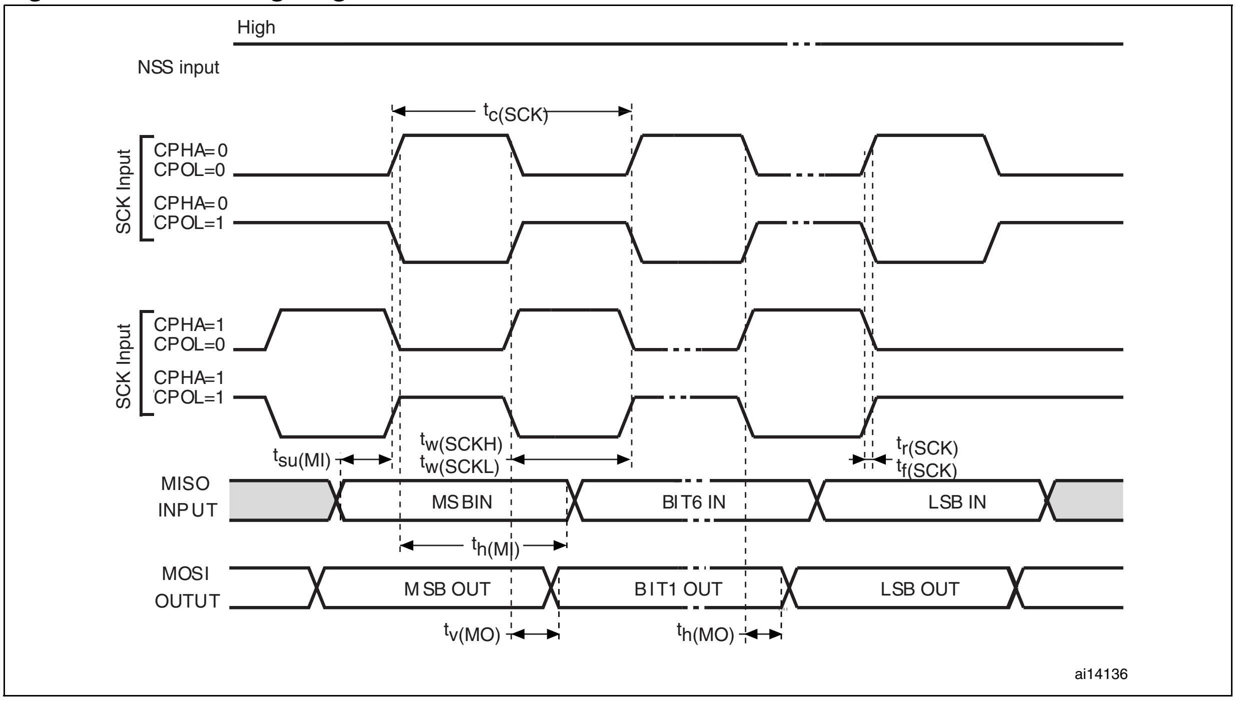


Figure 16. SPI timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 17. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

I^2C - Inter IC control interface

Subject to general operating conditions for V_{DD}, f_{SYSCLK}, and T_A unless otherwise specified.

The STM8L I^2C interface (I2C1) meets the requirements of the Standard I^2C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

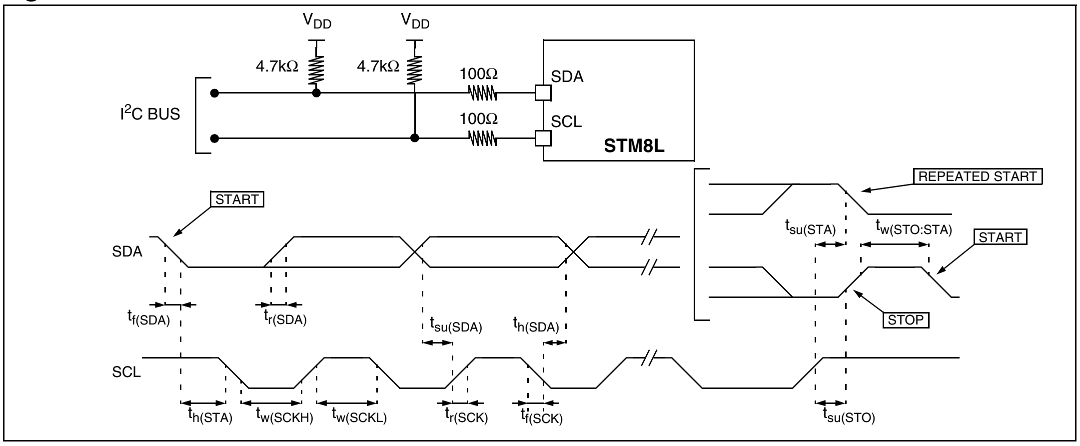
Table 38. I2C characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C(1)		Unit
		Min(2)	Max (2)	Min (2)	Max (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000		300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	ns
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		µs
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{SYSCLK} must be at least equal to 8 MHz to achieve max fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.

Note: For speeds around 200 kHz, the achieved speed can have a±5% tolerance
For other speed ranges, the achieved speed can have a±2% tolerance
The above variations depend on the accuracy of the external components used.

Figure 18. Typical application with I²C bus and timing diagram 1)



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

8.3.8 LCD controller (STM8L152xx only)

Table 39. LCD characteristics(1)

Symbol	Parameter	Min	Typ	Max.	Unit
V_{LCD}	LCD external voltage			3.6	V
V_{LCD0}	LCD internal reference voltage 0		2.6		V
V_{LCD1}	LCD internal reference voltage 1		2.7		V
V_{LCD2}	LCD internal reference voltage 2		2.8		V
V_{LCD3}	LCD internal reference voltage 3		2.9		V
V_{LCD4}	LCD internal reference voltage 4		3.0		V
V_{LCD5}	LCD internal reference voltage 5		3.1		V
V_{LCD6}	LCD internal reference voltage 6		3.2		V
V_{LCD7}	LCD internal reference voltage 7		3.3		V
Cext	V_{LCD} external capacitance	0.1		2	µF
I_{DD}	Supply current(2) at V_{DD} = 1.8 V		TBD		
	Supply current(2) at V_{DD} = 3 V		TBD		
R_H	Low drive resistive network		TBD		MΩ
R_L	High drive resistive network		TBD		kΩ
V_{33}	Segment/Common higher level voltage			V_{LCDx}	V
V_{23}	Segment/Common 2/3 level voltage		2/3V_{LCDx}		V
V_{12}	Segment/Common 1/2 level voltage		1/2V_{LCDx}		V
V_{13}	Segment/Common 1/3 level voltage		1/3V_{LCDx}		V
V_0	Segment/Common lowest level voltage	0			V

1. Data guaranteed by Design, not tested in production.
2. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.

VLCD external capacitor (STM8L152xx only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 39*.

8.3.9 Embedded reference voltage

Table 40. Reference voltage characteristics[1]

Symbol	Parameter	Min	Typ	Max.	Unit
I_{REFINT}	Internal reference voltage consumption		1.4		µA
$T_{S\_VREFINT}$	ADC sampling time when reading the internal reference voltage[2]		5	10	µs
I_{BUF}	Internal reference voltage buffer consumption (used for ADC)		13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	TBD	1.225	TBD	V
V_{REFINT_DIV1}	1/4 reference voltage		25		$\%V_{REFINT\_COMP}$
V_{REFNT_DIV2}	1/2 reference voltage		50		
V_{REFNT_DIV3}	3/4 reference voltage		75		
I_{LPBUF}	Internal reference voltage low power buffer consumption (used for comparators or output)		730	1200	nA
I_{REFOUT}	Buffer ouptut current[3]			1	µA
C_{REFOUT}	Reference voltage output load			50	pF
$t_{VREFINT}$	Internal reference voltage startup time		2	TBD	ms
t_{BUFEN}	Internal reference voltage buffer startup time once enabled [2]			10	µs
$ACC_{VREFINT}$	Accuracy of V_{REFINT} stored in engibyte			± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} in temperature		20	50	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours			TBD	ppm

1. Based on characterization results, unless otherwise specified
2. Defined when ADC output reaches its final value ±1/2LSB
3. To guaranty less than 1% V_{REFOUT} deviation

8.3.10 Temperature sensor

Table 41. TS characteristics[1]

Symbol	Parameter	Min	Typ	Max.	Unit
V_{25}	Sensor reference voltage at 25°C	TBD	0.495	TBD	V
T_L	V_{SENSOR} linearity with temperature		TBD	TBD	°C
Avg_slope	Average slope	TBD	TBD	TBD	mV/°C
$IDD_{(TEMP)}$	Consumption		3.4	6	µA

Table 41. TS characteristics(1) (continued)

Symbol	Parameter	Min	Typ	Max.	Unit
T_{START}	Temperature sensor startup time (2)			10	µs
T_{S_TEMP}	ADC sampling time when reading the temperature sensor		5	10	µs

1. Based on characterization results, unless otherwise specified.
2. Defined for ADC output reaches its final value ±1/2LSB.

8.3.11 Comparator characteristics

Table 42. Comparator 1 characteristics

Symbol	Parameter	Min (1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	1.65		3.6	V
T_A	Temperature range	-40		125	°C
R_{400}	R_{400} value	TBD	400	TBD	kΩ
Err_{400}	Error on R_{400}			TBD	%
R_{10}	R_{10} value	TBD	10	TBD	kΩ
Err_{10}	Error on R_{10}			TBD	%
V_{IN}	Comparator input voltage range	0		V_{DDA}	V
V_{REFINT}	Internal reference reference voltage	TBD	1.225	TBD	
t_{START}	Startup time after enable		7	TBD	µs
t_d	Propagation delay(2)		3	TBD	µs
V_{offset}	Comparator offset error	TBD	3	TBD	mV
I_{CMP1}	Consumption(3)		160	TBD	nA

1. Data guaranteed by design, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Table 43. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min (1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage		1.65		3.6	V
T_A	Temperature range		-40		125	°C
V_{IN}	Comparator input voltage range		0		V_{DDA}	V
t_{START}	Startup time after enable in fast mode	1.65 V to 2.7 V			TBD	µs
		2.7 V to 3.6 V			TBD	
	Startup time after enable in slow mode	1.65 V to 2.7 V			TBD	µs
		2.7 V to 3.6 V			TBD	

Table 43. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min [1]	Typ	Max[1]	Unit
t_{df}	Propagation delay in fast mode[2]	1.65 V to 2.7 V		TBD	TBD	µs
		2.7 V to 3.6 V		TBD	TBD	
t_{ds}	Propagation delay in slow mode[2]	1.65 V to 2.7 V		TBD	TBD	µs
		2.7 V to 3.6 V		TBD	TBD	
V_{offset}	Comparator offset error	1.65 V to 2.7 V		TBD	TBD	mV
		2.7 V to 3.6 V		TBD	TBD	
$I_{DD(CMP2F)}$	Consumption in fast mode	1.65 V to 2.7 V		TBD	TBD	µA
		2.7 V to 3.6 V		TBD	TBD	
$I_{DD(CMP2S)}$	Consumption in slow mode	1.65 V to 2.7 V		TBD	TBD	µA
		2.7 V to 3.6 V		TBD	TBD	

1. Data guaranteed by design, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

8.3.12 12-bit DAC characteristics

Table 44. DAC characteristics, output on PF0[1]

Symbol	Parameter	Conditions	Min [2]	Typ	Max[1]	Unit
V_{DDA}	Analog supply voltage		1.8		3.6	V
V_{REF+}	Reference supply voltage		1.8		3.6	V
T_A	Temperature range		-40		125	°C
I_{VDDA}	Current on V_{DDA} supply	No load, middle code 0x800 on the inputs		370	TBD	µA
		No load, worst code 0xF1C @ V_{REF+}=3.6V on the inputs		500	TBD	
I_{VREF+}	Current on V_{REF+} supply			210	TBD	
R_L	Resistive load[3]	DACOUT buffer ON	5			kΩ
R_O	Output impedance	DACOUT buffer OFF			TBD	kΩ
C_L	Capacitive load[4]				50	pF
DAC_OUT	DAC_OUT voltage[5]	DACOUT buffer ON	0.2		V_{REF+}-0.2	V
		DACOUT buffer OFF	0		V_{REF+}	V
DNL	Differential non linearity[6]	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF DACOUT buffer ON		± 1	TBD	12-bit LSB
		$C_L \leq 50$ pF DACOUT buffer OFF	-	TBD	TBD	

Table 44. DAC characteristics, output on PF0[1] (continued)

Symbol	Parameter	Conditions	Min [2]	Typ	Max[1]	Unit
INL	Integral non linearity[7]	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF DACOUT buffer ON		± 2	TBD	12-bit LSB
		$C_L \leq 50$ pF DACOUT buffer OFF		TBD	TBD	
Offset	Offset error[8]	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF DACOUT buffer ON		± 20	TBD	mV
		$C_L \leq 50$ pF DACOUT buffer OFF		TBD	TBD	
Gain error	Gain error	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF DACOUT buffer ON		0.5	TBD	%
		$C_L \leq 50$ pF DACOUT buffer OFF		TBD	TBD	
TUE	Total unadjusted error	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF DACOUT buffer ON		TBD	TBD	12-bit LSB
		$C_L \leq 50$ pF DACOUT buffer OFF		TBD	TBD	
$t_{settling}$	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches the final value ±1LSB	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF		7	TBD	µs
Update rate	Max frequency for a correct DAC_OUT (@95%) change when small variation of the input code (from code i to i+1LSB).	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF			1	Msps
t_{WAKEUP}	Wakeup time from OFF state. Input code between lowest and highest possible codes.	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF		9	TBD	µs
PSRR+	Power supply rejection ratio (to VDDA) (static DC measurement)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF		-60	-35	dB

1. For 48-pin package only.
2. Data guaranteed by design, not tested in production.
3. Resistive load between DACOUT and GNDA.
4. Capacitive load at DACOUT pin.
5. It gives the output excursion of the DAC.
6. Difference between two consecutive codes - 1 LSB.
7. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
8. Difference between measured value and ideal value=$V_{REF}/2$.

Table 45. DAC output on PB4-PB5-PB6(1)

Symbol	Parameter	Min (2)	Typ	Max(1)	Unit
R_{int}	Internal resistance between DAC output and PB4-PB5-PB6 output		TBD	TBD	kΩ

1. 32 or 28-pin packages only. The DAC channel can be routed either on PB4, PB5 or PB6 using the routing interface I/O switch registers.
2. Data guaranteed by design, not tested in production.

8.3.13 12-bit ADC1 characteristics

Table 46. ADC1 characteristics

Symbol	Parameter	Conditions	Min [1]	Typ	Max[1]	Unit
V_{DDA}	Analog supply voltage		1.8		3.6	V
V_{REF+}	Reference supply voltage	2.4 V ≤V_{DDA}≤ 3.6 V	2.4		V_{DDA}	V
		1.8 V≤V_{DDA}≤ 2.4 V		V_{DDA}		V
V_{REF-}	Lower reference voltage			V_{SSA}		V
I_{VDDA}	Current on the VDDA input pin			1000		µA
I_{VREF+}	Current on the VREF+ input pin			400	TBD	µA
V_{AIN}	Conversion voltage range		0[2]		V_{REF+}	
T_A	Temperature range		-40		125	°C
R_{AIN}	External resistance on V_{AIN}				TBD[3]	kΩ
R_{ADC}	Sampling switch resistance	on PF0 fast channel			TBD	kΩ
		on all other channels			TBD	kΩ
C_{ADC}	Internal sample and hold capacitor	on PF0 fast channel			TBD	pF
		on all other channels			TBD	pF
f_{ADC}	ADC sampling clock frequency	2.4 V≤V_{DDA}≤3.6 V without zooming	0.320		16	MHz
		1.8 V≤V_{DDA}≤2.4 V with zooming	0.320		8	MHz
f_S	Sampling rate	V_{AIN} on PF0 fast channel	0.02		1[4]	MHz
		V_{AIN} on all other channels				
f_{TRIG}	External trigger frequency				TBD	$1/f_{ADC}$
t_{LAT}	External trigger latency				TBD	$1/f_{ADC}$
t_S	Sampling time	V_{AIN} on fast channel PF0	4[4]			$1/f_{ADC}$
		V_{AIN} on slow channels	TBD			$1/f_{ADC}$
t_{conv}	Conversion time			$12 + t_S$		$1/f_{ADC}$
		16 MHz		1[3]		µs
t_{WKUP}	Wakeup time from OFF state				3	µs
$t_{VREFINT}$	Internal reference voltage startup time				refer to Table 40	ms

1. Data guaranteed by design, not tested in production.
2. V_{REF-} or V_{DDA} must be tied to ground.
3. For 1 Msps, maximum Rext is 0.5 kΩ.
4. Value obtained for continous conversion on fast channel.

Table 47. ADC1 accuracy

Symbol	Parameter	Typ	Max[1]	Unit
DNL	Differential non linearity	TBD	± 1	LSB
INL	Integral non linearity	TBD	± 2	LSB
TUE	Total unadjusted error	TBD	± 5	LSB
Offset	Offset error	TBD	± 2	LSB
Gain	Gain error	TBD	± 3.5	LSB
ENOB	Effective number of bits	TBD	± 9.5	Bits
SINAD	Signal-to-noise and distortion ratio	TBD	TBD	dB
SNR	Signal-to-noise ratio	TBD	TBD	dB
THD	Total harmonic distorsion	TBD	TBD	dB

1. Data based on characterization, not tested in production.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 19* or *Figure 20*, depending on whether V_{REF+} is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

Figure 19. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

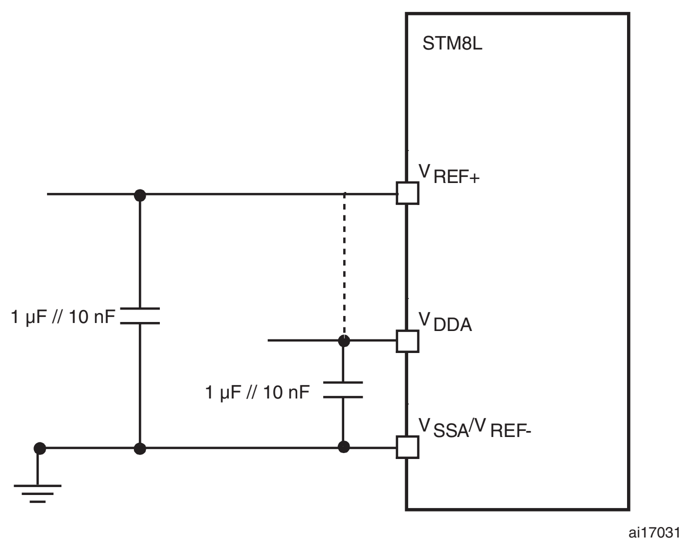
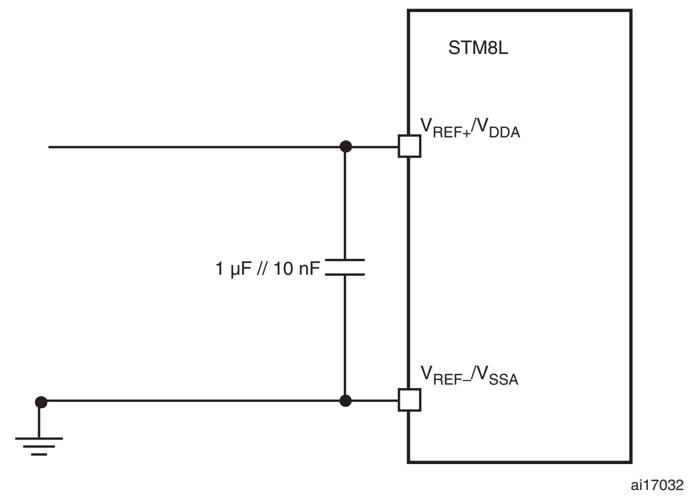


Figure 20. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



8.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 48. EMS data

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU}= 16 MHz, conforms to IEC 61000	TBD
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU} = 16 MHz, conforms to IEC 61000	TBD

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC61967-2 which specifies the board and the loading of each pin.

Table 49. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. 16 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP32 conforming to IEC61967-2	0.1 MHz to 30 MHz	TBD	dBµV
			30 MHz to 130 MHz	TBD	
			130 MHz to 1 GHz	TBD	
			SAE EMI Level	1	-

1. Not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and charge device model. This test conforms to the JESD22-A114A/A115A standard.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25\ °C$	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		1000	

1. Data based on characterization results, not tested in production.

Static latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 51. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

8.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 15: General operating conditions on page 58*.

The maximum chip-junction temperature, T_{Jmax}, in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma\ (V_{OL}{*}I_{OL}) + \Sigma((V_{DD}\text{-}V_{OH}){*}I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 52. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient WFQFPN28 - 4 x 4 mm	TBD	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	TBD	°C/W
Θ_{JA}	Thermal resistance junction-ambient VFQFPN 32 - 5 x 5 mm	TBD	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 48- 7 x 7 mm	TBD	°C/W
Θ_{JA}	Thermal resistance junction-ambient VFQFPN 48- 7 x 7mm	TBD	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

9 Package characteristics

9.1 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

9.2 Package mechanical data

Figure 21. WFQFPN28 – 28-lead very very thin fine pitch quad flat no-lead package outline (4 x 4)(1)

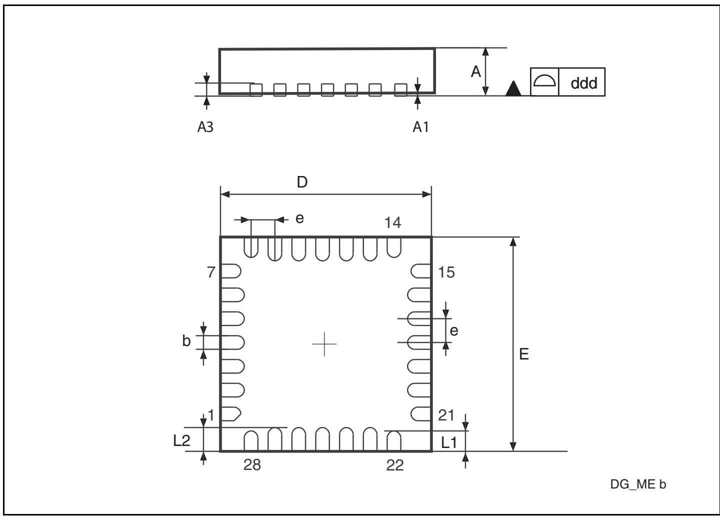
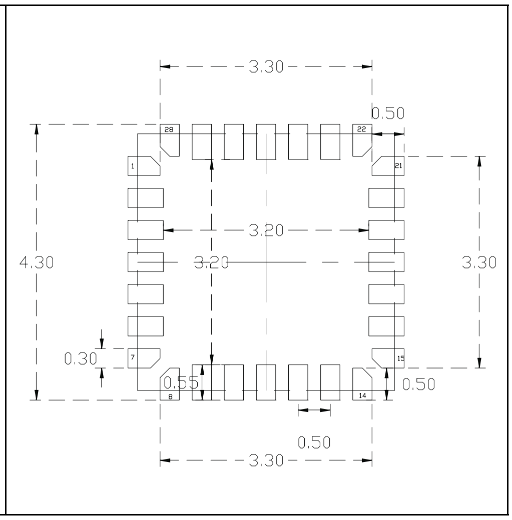


Figure 22. Recommended footprint (dimensions in mm)(1)



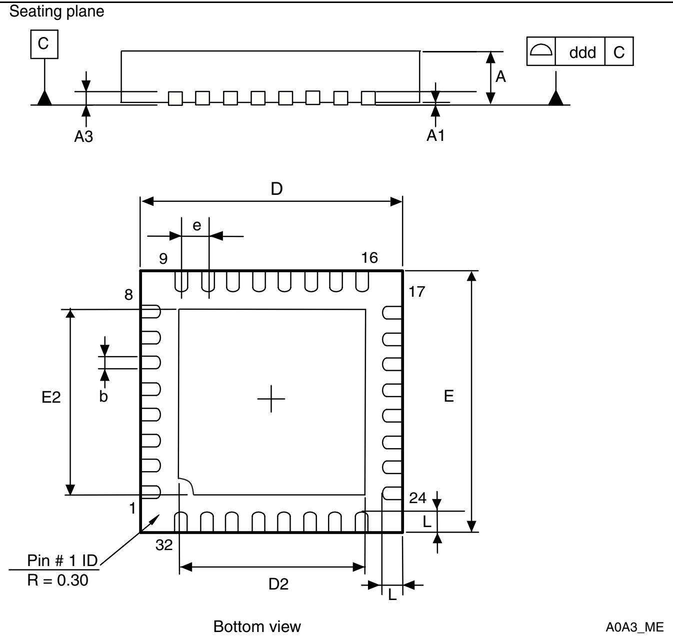
1. Drawing is not to scale.

Table 53. WFQFPN28 – 28-lead very very thin fine pitch quad flat no-lead package (4 x 4), package mechanical data(1)

Dim.	mm			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A(1)	0.7	0.75	0.8	0.0276	0.0295	0.0315
A1	0	0.02	0.05	0	0.0008	0.002
A3		0.2			0.0079	
b	0.18	0.25	0.3	0.0071	0.0098	0.0118
D		4			0.1575	
E		4			0.1575	
e		0.5			0.0197	
L1	0.25	0.35	0.45	0.0098	0.0138	0.0177
L2	0.3	0.4	0.5	0.0118	0.0157	0.0197
ddd		0.08			0.0031	
	Number of pins					
N	28					

1. Thickness valid for the WFQFPN28 package in the sampling phase. In the production phase, the UFQFPN28 package will be used with a thickness equal to 0.6 mm.
2. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 23. WFQFPN32 – 32-lead very very thin fine pitch quad flat no-lead package outline (5 x 5)



1. The exposed pad must be soldered to the PCB. It is recommended to connect it to V_{SS}.

Table 54. WFQFPN32 – 32-lead very very thin fine pitch quad flat no-lead package (5 x 5), package mechanical data(1)

Dim.	mm			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A(1)	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0	0.02	0.05		0.0008	0.0020
A3		0.20			0.0079	
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D	4.85	5.00	5.15	0.1909	0.1969	0.2028
D2	3.20	3.45	3.70	0.1260	0.1358	0.1457
E	4.85	5.00	5.15	0.1909	0.1969	0.2028
E2	3.20	3.45	3.70	0.1260	0.1358	0.1457
e		0.50			0.0197	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd	0.08			0.0031		
	Number of pins					
N	32					

1. Thickness valid for the WFQFPN32 package in the sampling phase. In the production phase, the UFQFPN32 package will be used with a thickness equal to 0.6 mm.
2. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 24. LQFP32 – 32-pin low profile quad flat package outline

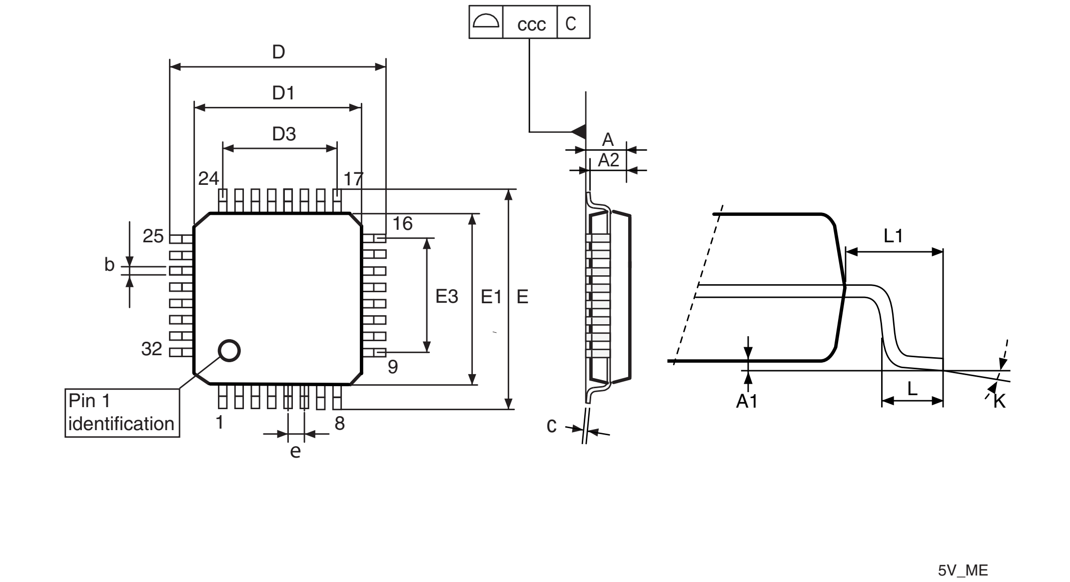


Table 55. LQFP32 – 32-pin low profile quad flat package, package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.6			0.063
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571
b	0.3	0.37	0.45	0.0118	0.0146	0.0177
c	0.09		0.2	0.0035		0.0079
D	8.8	9	9.2	0.3465	0.3543	0.3622
D1	6.8	7	7.2	0.2677	0.2756	0.2835
D3		5.6			0.2205	
E	8.8	9	9.2	0.3465	0.3543	0.3622
E1	6.8	7	7.2	0.2677	0.2756	0.2835
E3		5.6			0.2205	
e		0.8			0.0315	
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1		1			0.0394	
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
ccc	0.1			0.0039		
	Number of pins					
N	32					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 25. VFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline(1)(2)

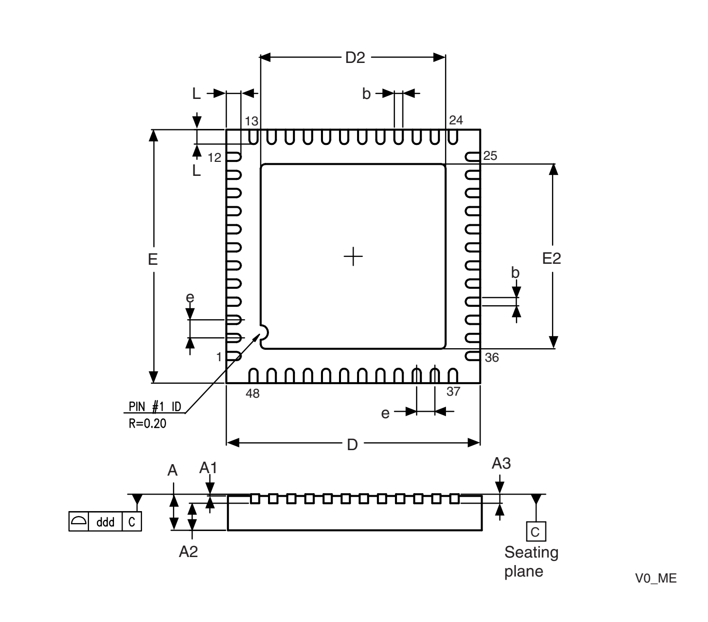
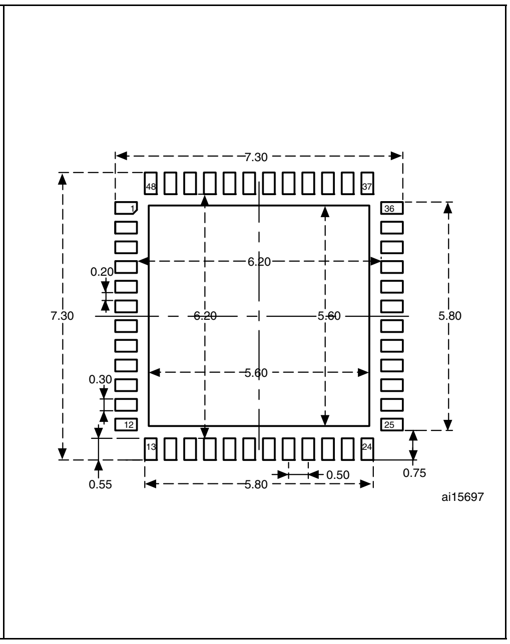


Figure 26. Recommended footprint (dimensions in mm)(1)



1. Drawing is not to scale.
2. The exposed pad must be soldered to the PCB. It is recommended to connect it to V_{SS}.

Table 56. VFQFPN48 – very thin fine pitch quad flat pack no-lead 7 × 7 mm, 0.5 mm pitch package mechanical data(1)

Symbol	millimeters			inches(2)		
	Typ	Min	Max	Typ	Min	Max
A(1)	0.900	0.800	1.000	0.0354	0.0315	0.0394
A1	0.020		0.050	0.0008		0.0020
A2	0.650		1.000	0.0256		0.0394
A3	0.250			0.0098		
b	0.230	0.180	0.300	0.0091	0.0071	0.0118
D	7.000	6.850	7.150	0.2756	0.2697	0.2815
D2	4.700	2.250	5.250	0.1850	0.0886	0.2067
E	7.000	6.850	7.150	0.2756	0.2697	0.2815
E2	4.700	2.250	5.250	0.1850	0.0886	0.2067
e	0.500	0.450	0.550	0.0197	0.0177	0.0217
L	0.400	0.300	0.500	0.0157	0.0118	0.0197
ddd	0.080			0.0031		

1. Thickness valid for the VFQFPN48 package in the sampling phase. In the production phase, the UFQFPN48 package will be used with a thickness equal to 0.6 mm.
2. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 27. LQFP48 – 48-pin low profile quad flat package outline (7x7)

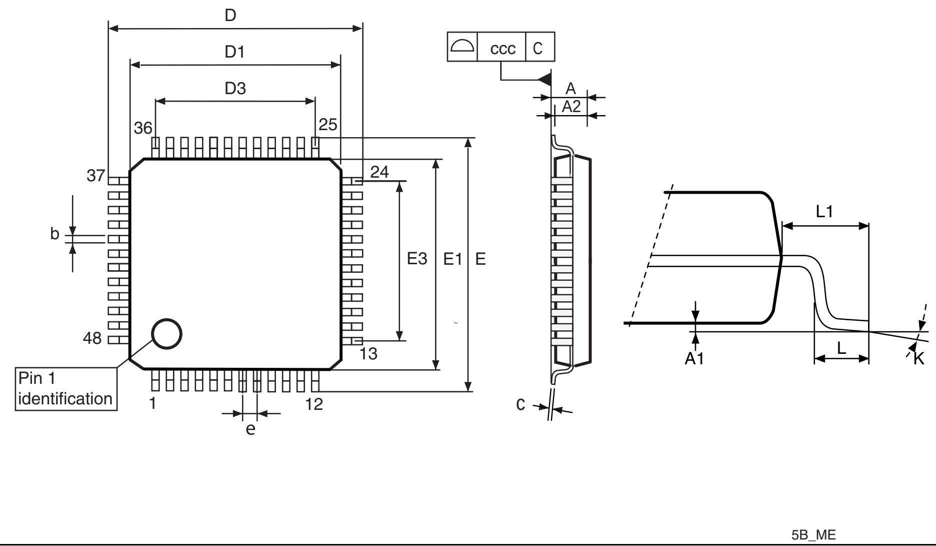


Table 57. LQFP48 – 48-pin low profile quad flat package (7x7), package mechanical data

Dim.	mm			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A			1.6			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.2	0.0035		0.0079
D	8.8	9	9.2	0.3465	0.3543	0.3622
D1	6.8	7	7.2	0.2677	0.2756	0.2835
D3		5.5			0.2165	
E	8.8	9	9.2	0.3465	0.3543	0.3622
E1	6.8	7	7.2	0.2677	0.2756	0.2835
E3		5.5			0.2165	
e		0.5			0.0197	
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1		1			0.0394	
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc			0.08			0.0031
	Number of pins					
N	48					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

10 Device ordering information

Figure 28. STM8L15xxx ordering information scheme

Example: STM8 L 151 C 4 U 6

Product class

STM8 microcontroller

Family type

L = Low power

Sub-family type

151 = Ultralow power

152 = Ultralow power with LCD

Pin count

C = 48 pins

K = 32 pins

G = 28 pins

Program memory size

4 = 16 Kbytes

6 = 32 Kbytes

Package

U = WFQFPN or VFQFPN

T = LQFP

Temperature range

3 = - 40 °C to 125 °C

6 = - 40 °C to 85 °C

For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please contact the ST sales office nearest to you.

11 Revision history

Table 58. Document revision history

Date	Revision	Changes
06-Aug-2009	1	Initial release
10-Sep-2009	2	Updated peripheral naming throughout document. Added *Figure 6: STM8L151Cx 48-pin pinout (without LCD) on page 24* Added capacitive sensing channels in *Features on page 1* Updated PA7, PC0 and PC1 in *Table 4: STM8L15x pin description* Changed CLK and REMAP register names in *Table 7* Changed description of WDGHALT in *Table 11* Added typical power consumption values in *Table 16* to *Table 23* Correct VIH max in *Table 32*