

Low Power Dual Operational Amplifier

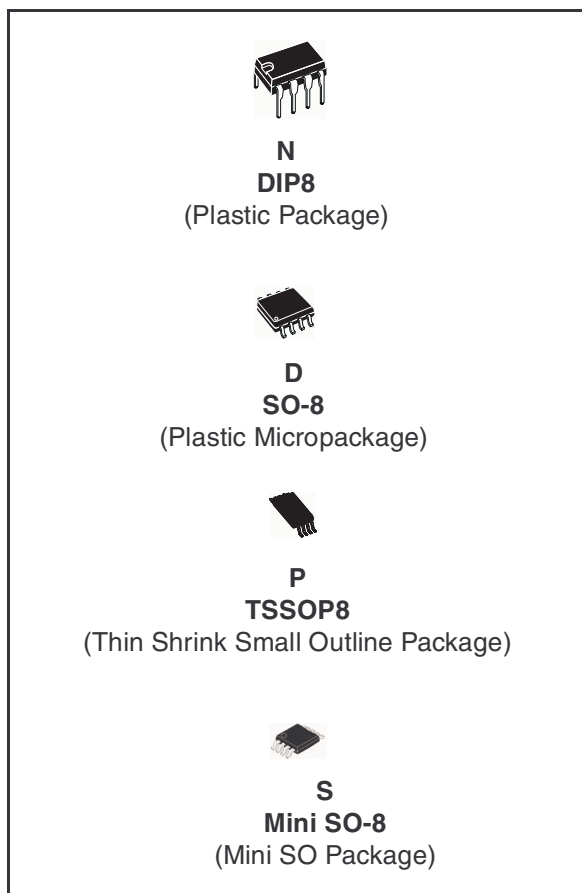
- Internally frequency compensated
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1.1MHz (temperature compensated)
- Very low supply current/op (500µA) essentially independent of supply voltage
- Low input bias current: 20nA (temperature compensated)
- Low input offset current: 2nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to ($V_{CC} - 1.5V$)

Description

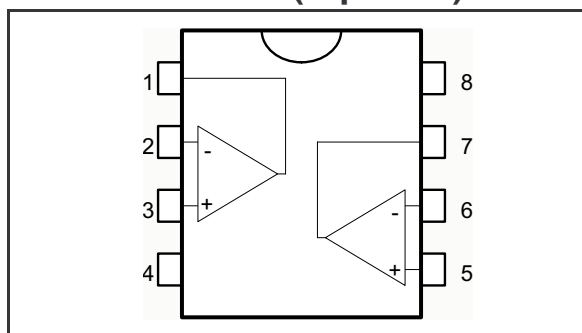
This circuit consists of two independent, high gain, internally frequency compensated which were designed specifically for automotive and industrial control system. It operates from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with off the standard +5V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.



Pin Connection (top view)



Order Codes

Part Number	Temperature Range	Package	Packing	Marking
LM2904N	-40, +125°C	DIP8	Tube	LM2904N
LM2904D/DT		SO-8	Tube or Tape & Reel	2904
LM2904PT		TSSOP8 (Thin Shrink Outline Package)	Tape & Reel	
LM2904ST		mini SO-8	Tape & Reel	K403
LM2904YD/YDT		SO-8 (automotive grade level)	Tube or Tape & Reel	2904Y
LM2904YPT		TSSOP8 (automotive grade level)	Tape & Reel	
LM2904YST		mini SO-8 (automotive grade level)	Tape & Reel	k409

1 Absolute Maximum Ratings

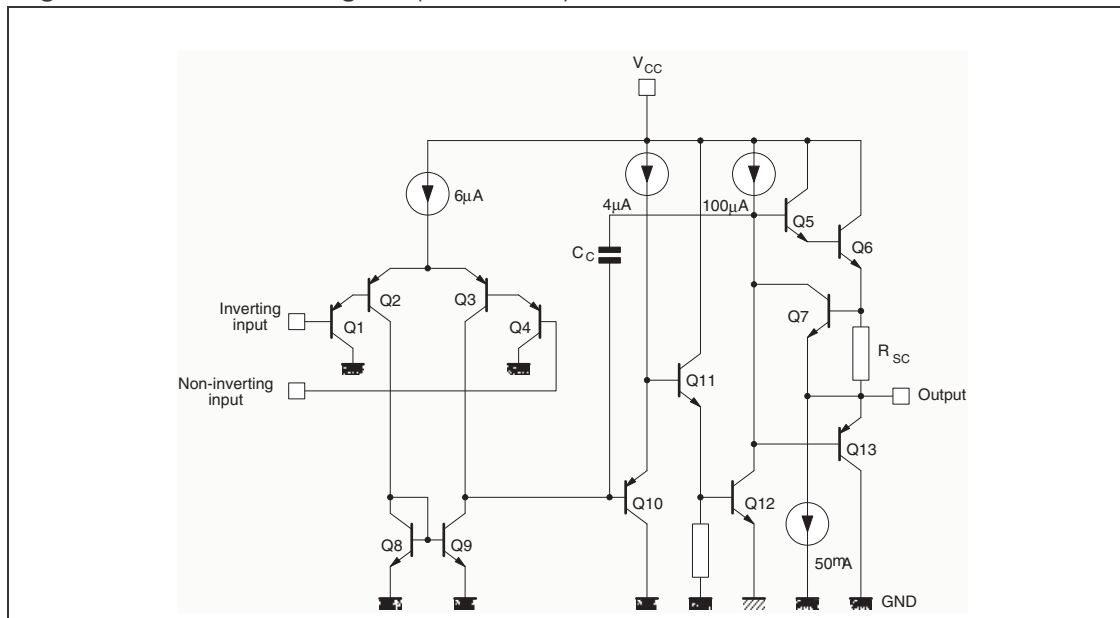
Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+32	V
V_{id}	Differential Input Voltage	+32	V
V_I	Input Voltage	-0.3 to +32	V
	Output Short-circuit to Ground ⁽¹⁾		
P_{tot}	Power Dissipation ⁽²⁾	500	mW
I_{in}	Input Current ⁽³⁾	50	mA
T_{oper}	Operating Free-Air Temperature Range	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
R_{thja}	Thermal Resistance Junction to Ambient SO-8 TSSOP8 DIP8 MiniSO-8	125 120 85 190	°C/W
ESD	HBM: Human Body Model ⁽⁴⁾	300	V
	MM: Machine Model ⁽⁵⁾	200	V
	CDM: Charged Device Model	1.5	kV

1. Short-circuits from the output to V_{CC} can cause excessive heating if $V_{CC} > 15V$. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC} . Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
2. Power dissipation must be considered to ensure maximum junction temperature (T_j) is not exceeded.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diodes clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative. This is not destructive and normal output will set up again for input voltage higher than -0.3V.
4. Human body model, 100pF discharged through a 1.5k Ω resistor into pin of device.
5. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5 Ω), into pin to pin of device.

2 Typical Application Schematic

Figure 1. Schematic Diagram (1/2 LM2904)



3 Electrical Characteristics

Table 2. $V_{CC}^+ = 5V$, $V_{CC}^- = \text{Ground}$, $V_O = 1.4V$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ⁽¹⁾ $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$.		2	7 9	mV
I_{io}	Input Offset Current $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$.		2	30 40	nA
I_{ib}	Input Bias Current ⁽²⁾ $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$.		20	150 200	nA
A_{vd}	Large Signal Voltage Gain $V_{CC}^+ = +15V, R_L = 2k\Omega$, $V_O = 1.4V$ to $11.4V$ $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$.	50 25	100		V/ mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$.	65 65	100		dB
I_{cc}	Supply Current, all Amp, no load $T_{amb} = 25^\circ C$, $V_{CC} = +5V$ $T_{min} \leq T_{amb} \leq T_{max}$, $V_{CC} = +30V$		0.7	1.2 2	mA
V_{icm}	Input Common Mode Voltage Range ($V_{CC} = +30V$) ⁽³⁾ $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$.	0 0		$V_{CC}^+ - 1.5$ $V_{CC}^+ - 2$	V
CMR	Common-mode Rejection Ratio ($R_S = 10k\Omega$) $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$.	70 60	85		dB
I_{source}	Output Short-circuit Current $V_{CC} = +15V$, $V_O = +2V$, $V_{id} = +1V$	20	40	60	mA
I_{sink}	Output Sink Current $V_O = 2V$, $V_{CC} = +5V$ $V_O = +0.2V$, $V_{CC} = +15V$	10 12	20 50		mA μA
V_{OPP}	Output Voltage Swing ($R_L = 2k\Omega$) $T_{amb} = 25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	0 0		$V_{CC}^+ - 1.5$ $V_{CC}^+ - 2$	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OH}	High Level Output Voltage ($V_{CC} + 30V$)				
	$T_{amb} = +25^{\circ}C$, $R_L = 2k\Omega$	26			
	$T_{min} \leq T_{amb} \leq T_{max}$.	26	27		V
	$T_{amb} = +25^{\circ}C$, $R_L = 10k\Omega$	27			
	$T_{min} \leq T_{amb} \leq T_{max}$.	27	28		
V_{OL}	Low Level Output Voltage ($R_L = 10k\Omega$)				
	$T_{amb} = +25^{\circ}C$		5	20	mV
	$T_{min} \leq T_{amb} \leq T_{max}$			20	
SR	Slew Rate $V_{CC} = 15V$, $V_i = 0.5$ to $3V$, $R_L = 2k\Omega$, $C_L = 100pF$, unity gain	0.3	0.6		V/ μs
GBP	Gain Bandwidth Product $f = 100kHz$ $V_{CC} = 30V$, $V_{in} = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$	0.7	1.1		MHz
THD	Total Harmonic Distortion $f = 1kHz$, $A_V = 20dB$, $R_L = 2k\Omega$, $V_o = 2V_{pp}$, $C_L = 100pF$, $V_{CC} = 30V$		0.02		%
DV_{io}	Input Offset Voltage Drift		7	30	$\mu V/^{\circ}C$
DI_{io}	Input Offset Current Drift		10	300	$pA/^{\circ}C$
V_{O1}/V_{O2}	Channel Separation ⁽⁴⁾ $1kHz \leq f \leq 20kHz$		120		dB

- $V_O = 1.4V$, $R_S = 0\Omega$, $5V < V_{CC}^+ < 30V$, $0V < V_{ic} < V_{CC}^+ - 1.5V$
- The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output, so no loading charge change exists on the input lines
- The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than $0.3V$. The upper end of the common-mode voltage range is $V_{CC}^+ - 1.5V$, but either or both inputs can go to $+32V$ without damage.
- Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Figure 2. Open loop frequency response

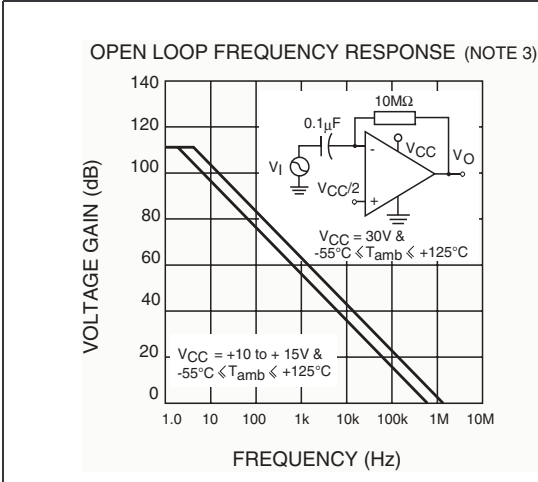


Figure 3. Large signal frequency response

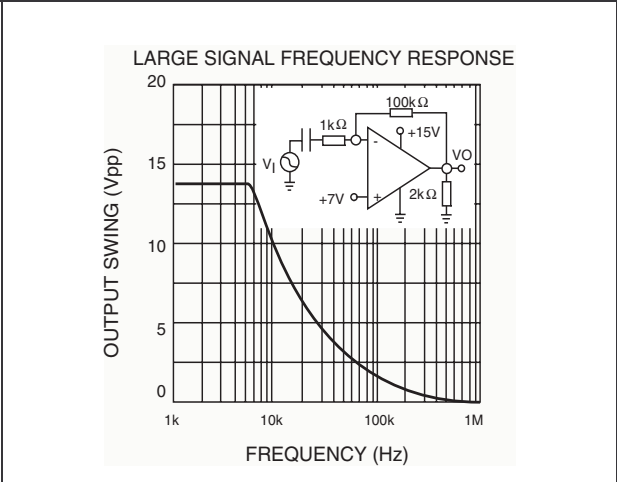


Figure 4. Voltage follower pulse response

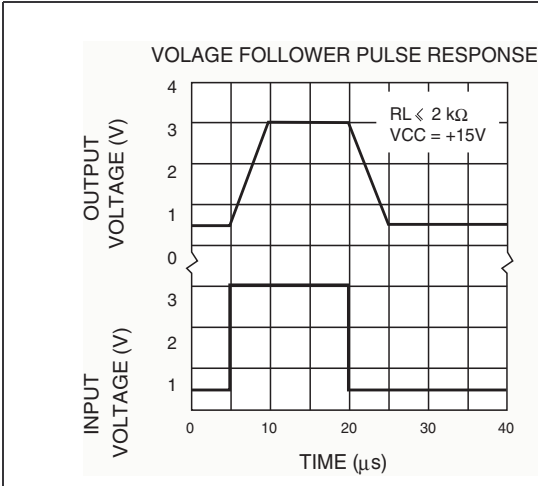


Figure 5. Output characteristics

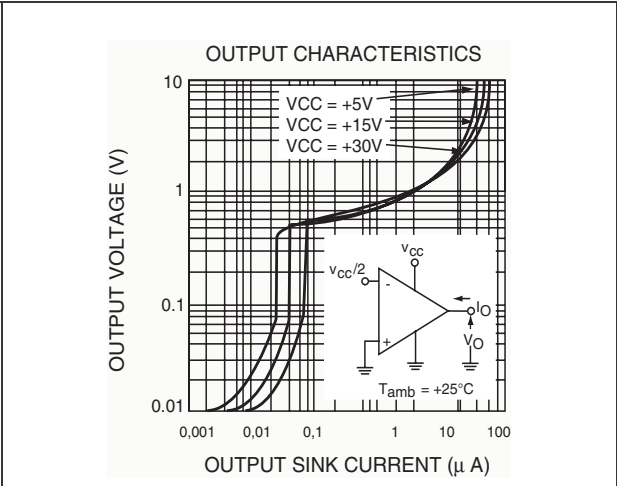


Figure 6. Voltage follower pulse response

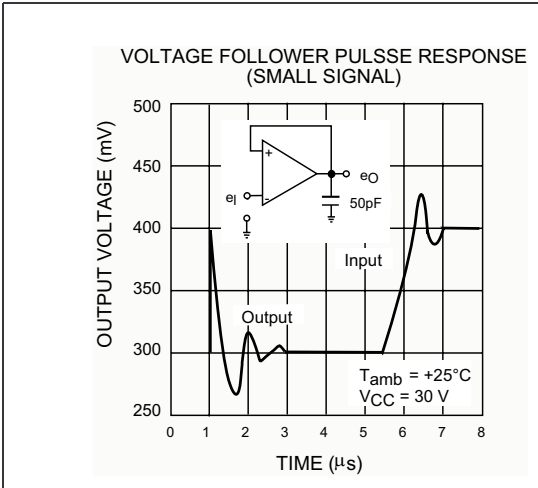


Figure 7. Output characteristics

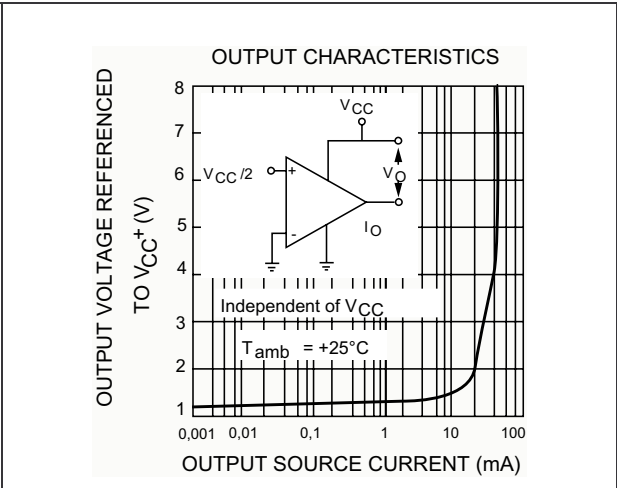


Figure 8. Input current

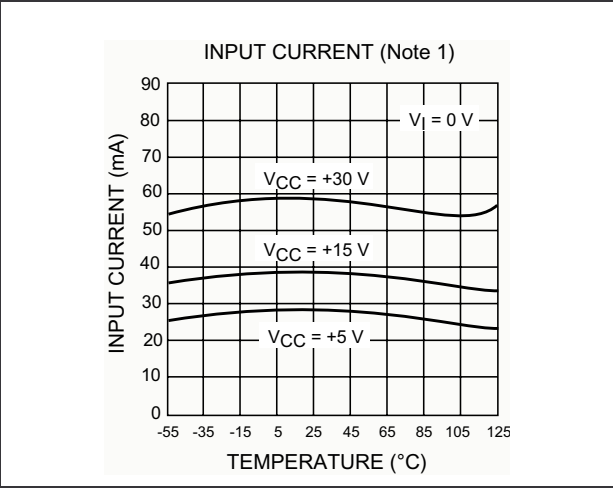


Figure 9. Current limiting

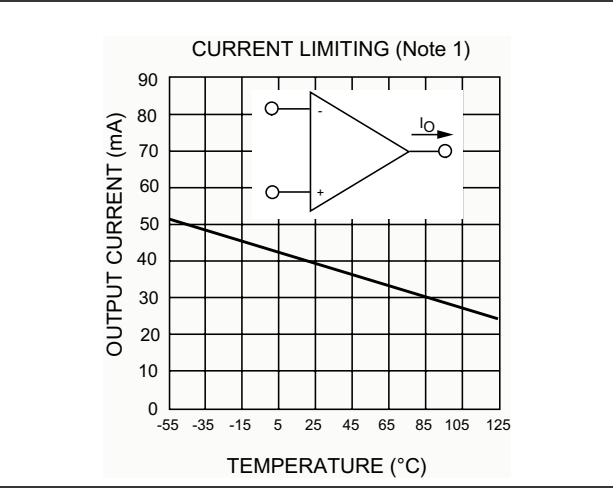


Figure 10. Input voltage range

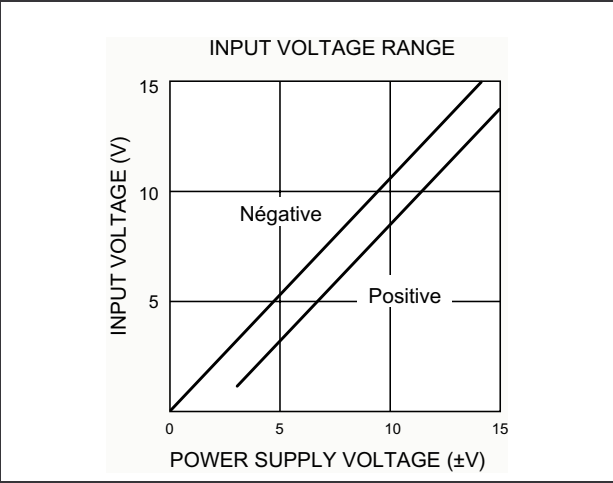


Figure 11. Supply current

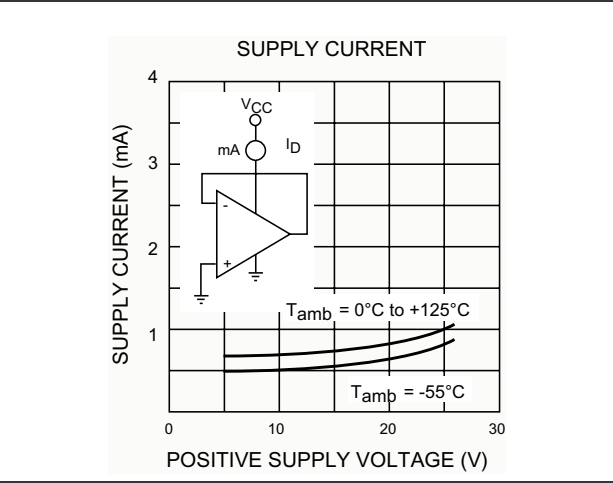


Figure 12. Positive supply voltage

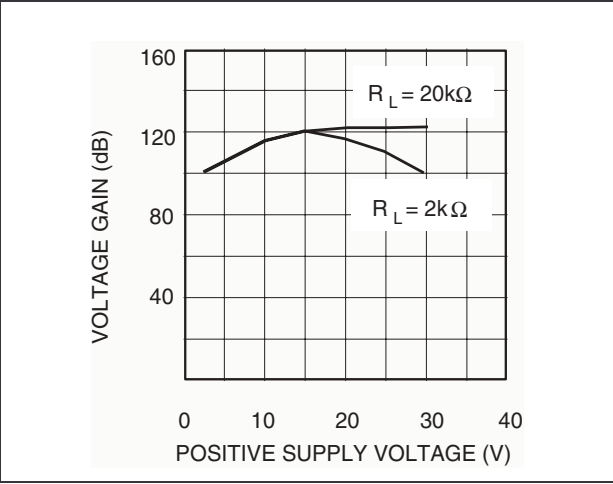


Figure 13. Positive supply voltage

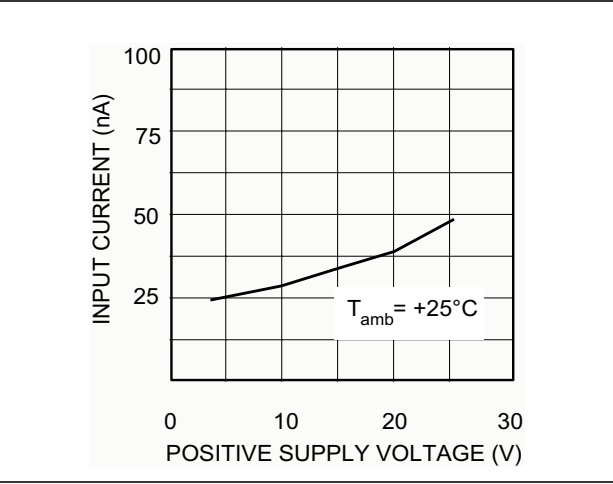


Figure 14. Positive supply voltage

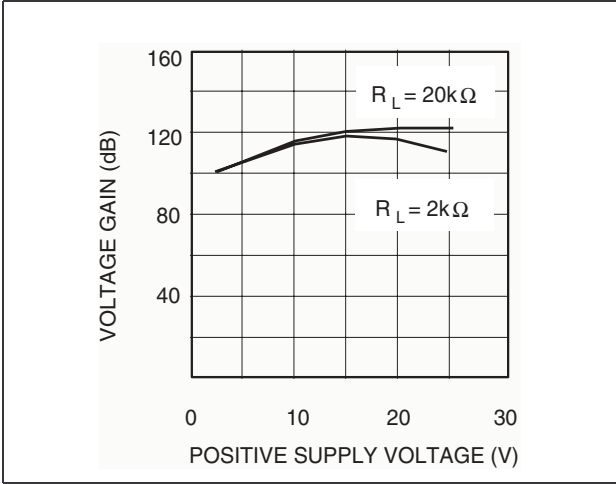


Figure 15. Gain bandwidth product

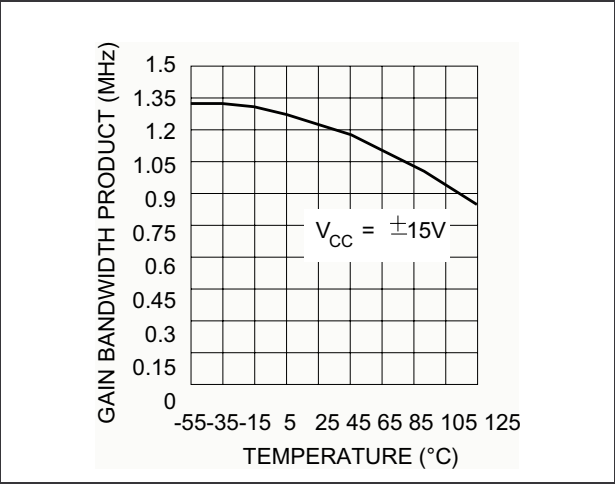


Figure 16. Power supply rejection ratio

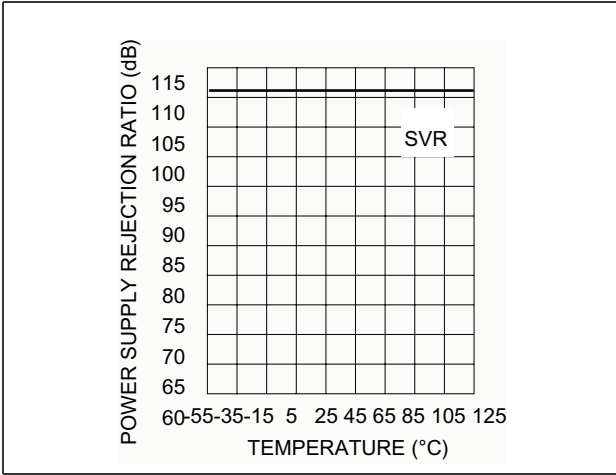
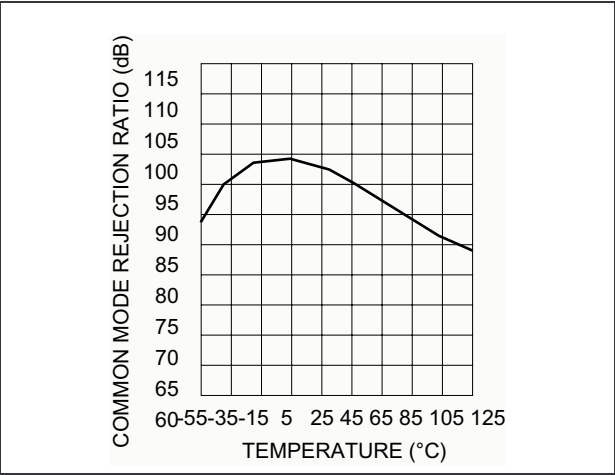


Figure 17. Common mode rejection ratio



Typical single - supply applications

Figure 18. AC coupled inverting amplifier

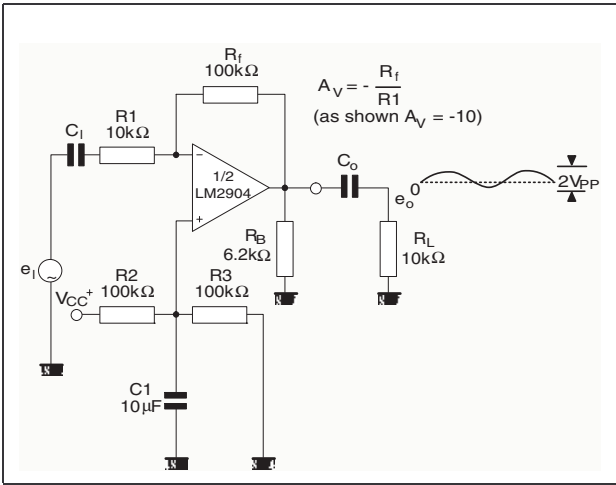


Figure 19. AC coupled non-inverting amplifier

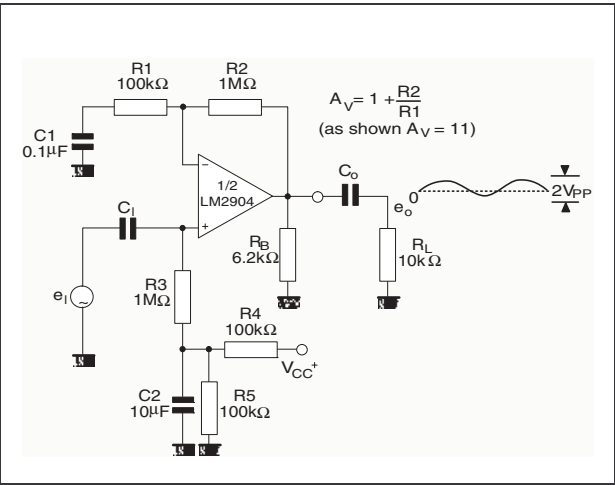


Figure 20. Non-inverting DC gain

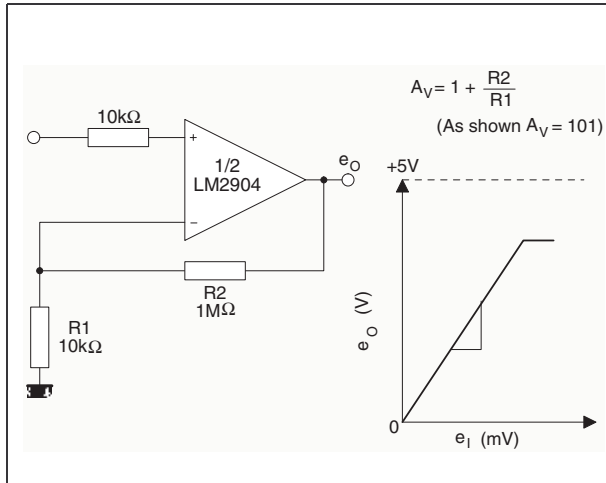


Figure 21. DC summing amplifier

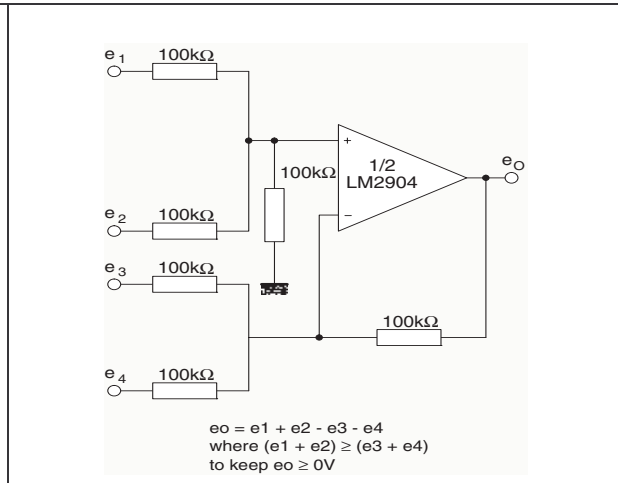


Figure 22. High input Z, DC differential amplifier

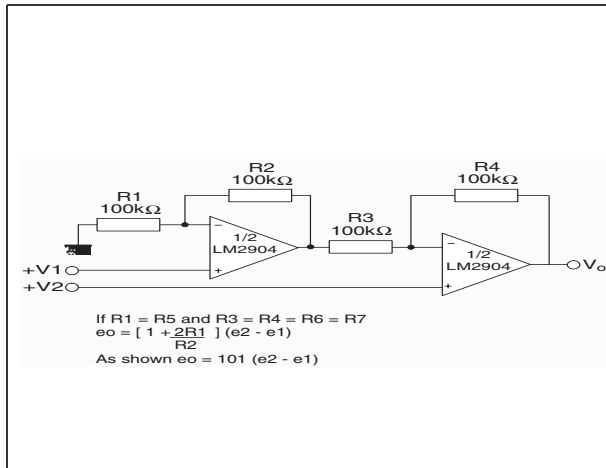


Figure 23. Using symmetrical amplifiers to reduce input current

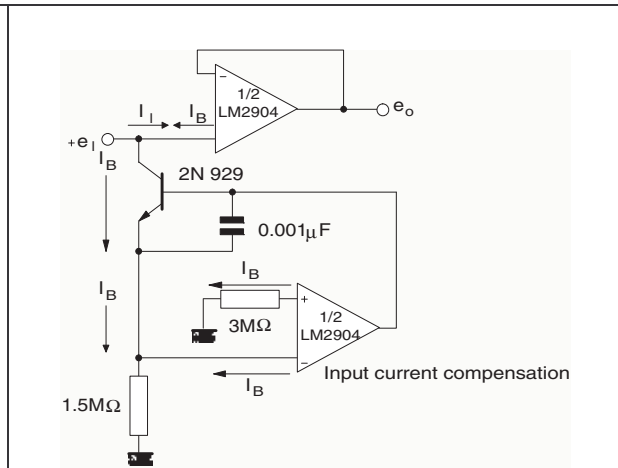


Figure 24. Low drift peak detector

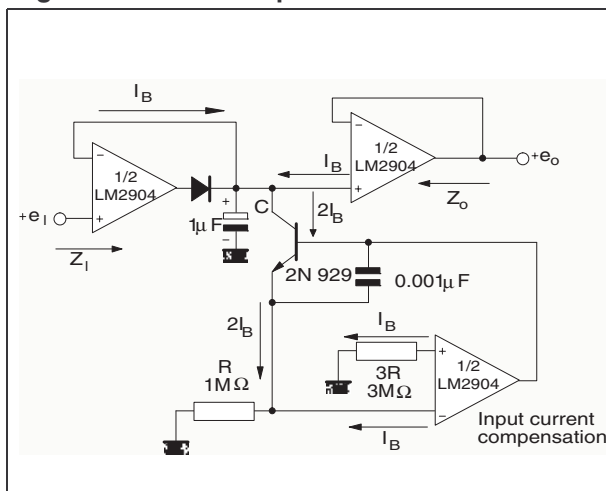
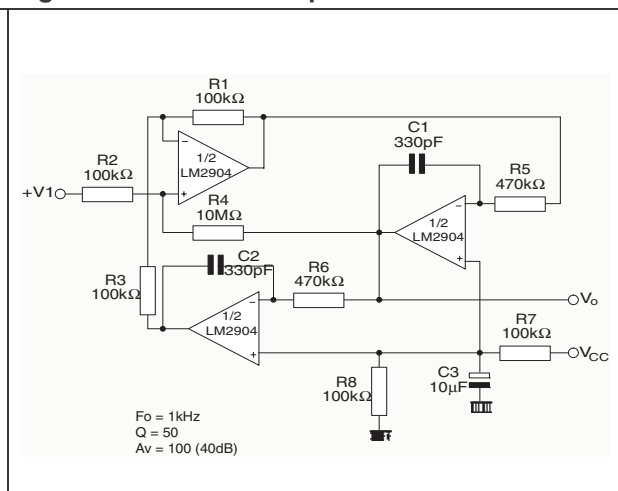


Figure 25. Active bandpass filter



4 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4.1 DIP8 Package

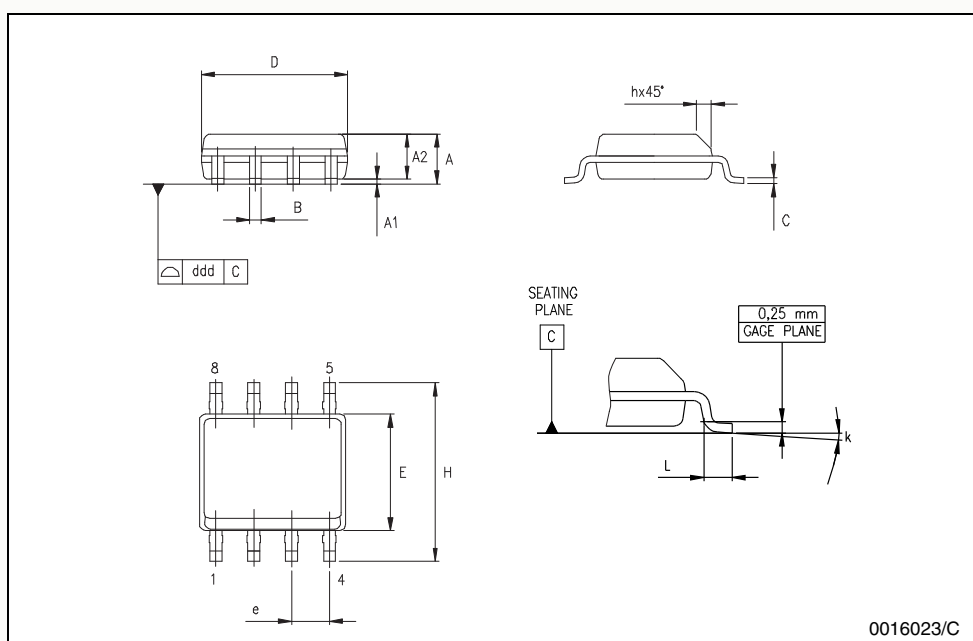
Plastic DIP-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

The diagram illustrates the mechanical dimensions of the DIP8 package. It includes three views: a top view showing the pin layout and dimensions A, a1, B, B1, b, b1, D, E, e, e3, e4, F, I, L, and Z; a side view showing the package height and dimensions A, a1, B, B1, b, b1, D, E, e, e3, e4, F, I, L, and Z; and a bottom view showing the pin layout and dimensions A, a1, B, B1, b, b1, D, E, e, e3, e4, F, I, L, and Z. The package is labeled with '8' and '5' on the top and '1' and '4' on the bottom.

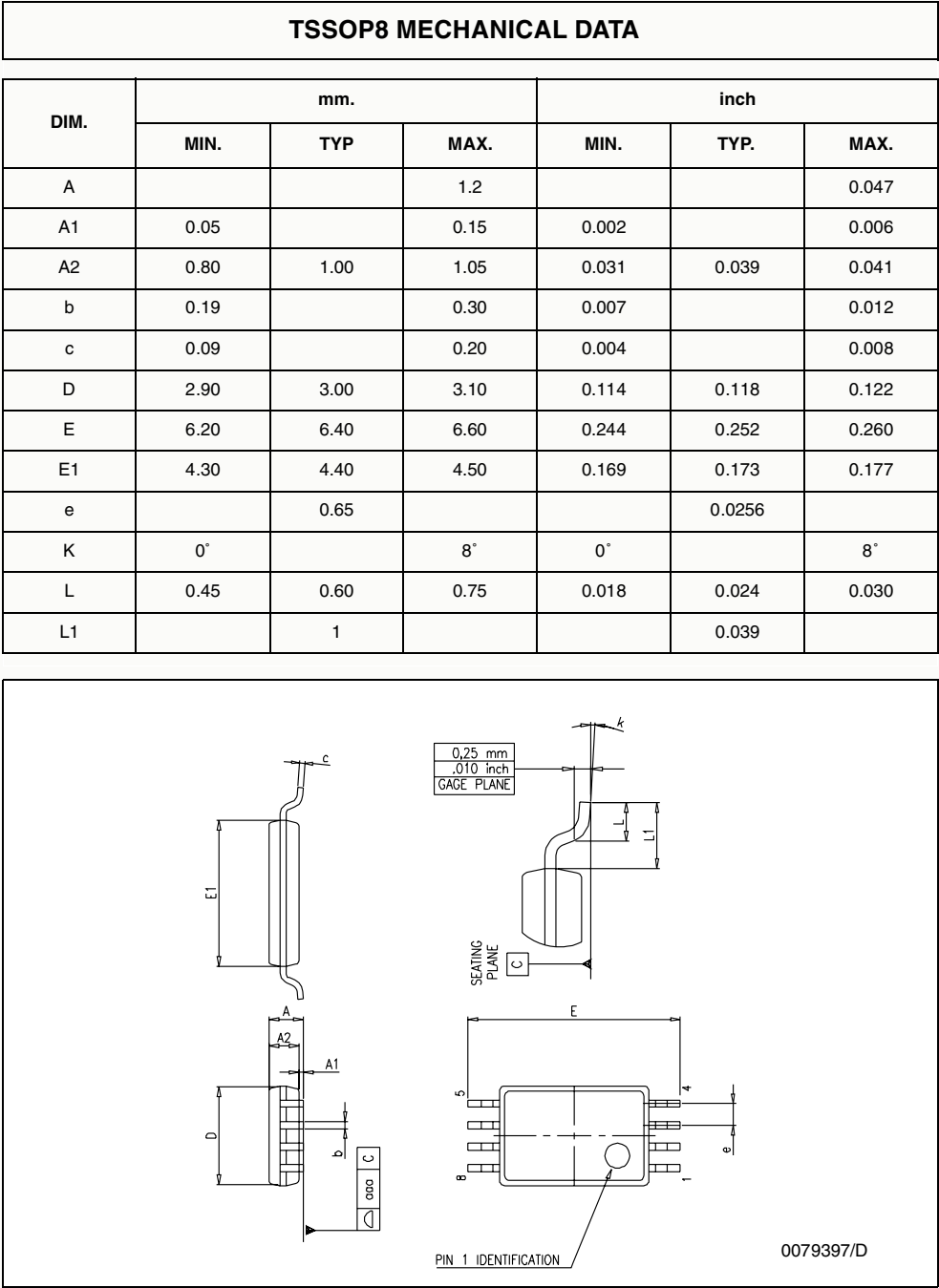
4.2 SO-8 Package

SO-8 MECHANICAL DATA

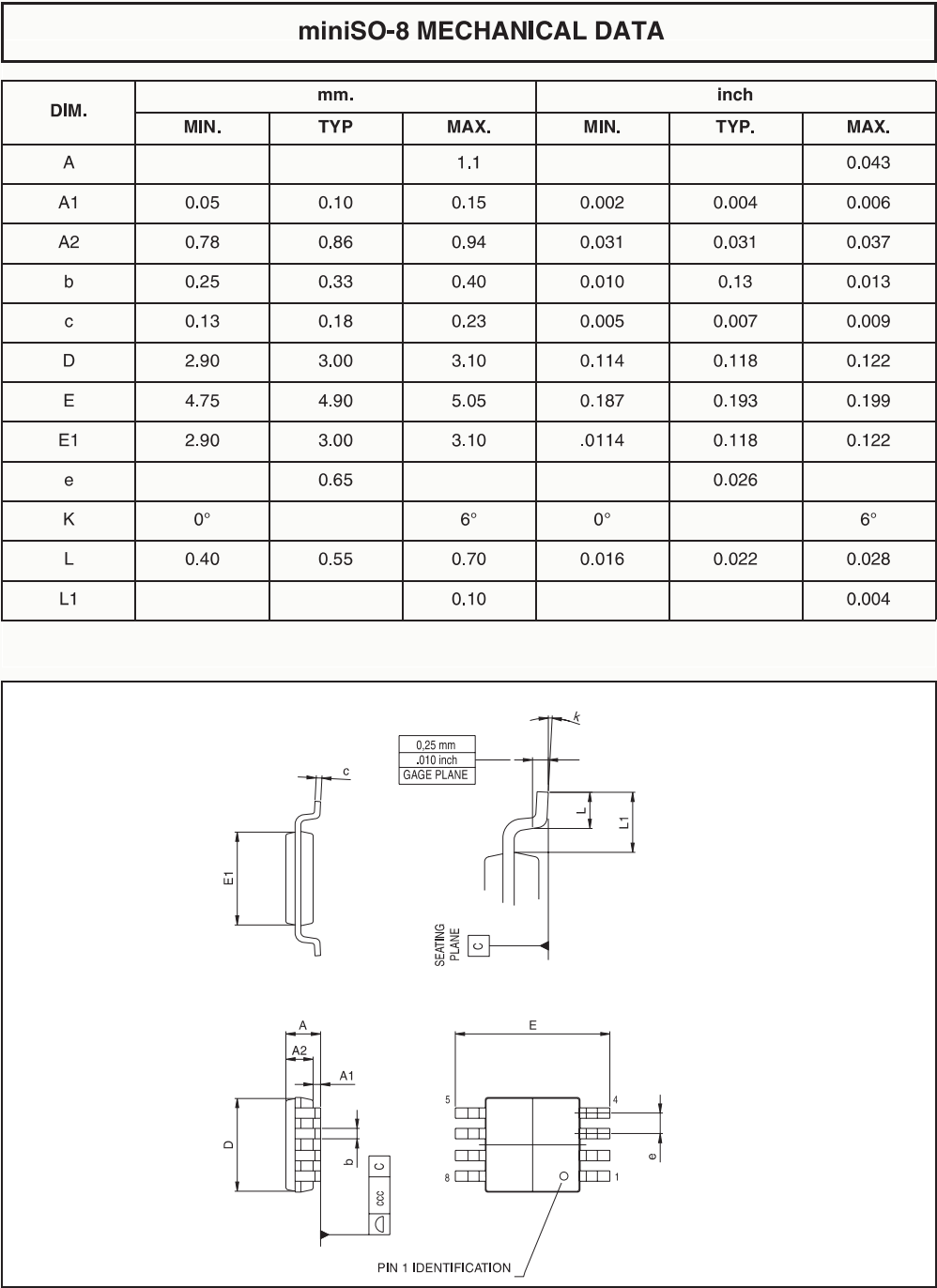
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



4.3 TSSOP8 Package



4.4 Mini SO-8 Package



5 Revision History

Date	Revision	Changes
Jan. 2002	1	Initial release.
June 2005	2	1 - PPAP references inserted in the datasheet see table <i>Order Codes on page 2</i> 2 - ESD protection inserted in <i>Table 1.: Key parameters and their absolute maximum ratings on page 4.</i>
Oct. 2005	3	PPAP part numbers added in table <i>Order Codes on page 2.</i>

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