



VNQ5050K-E

QUAD CHANNEL HIGH SIDE DRIVER FOR AUTOMOTIVE APPLICATIONS

ADVANCE DATA

Table 1. General Features

TYPE	V _{CC}	R _{DS(on)}	I _{out}
VNQ5050K-E	41V	50mΩ (*)	12A

(*) Per channel

- OUTPUT CURRENT: 12A
- 3.0 V CMOS COMPATIBLE INPUT
- STATUS DISABLE
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- OUTPUT STUCK TO V_{CC} DETECTION
- OPEN DRAIN STATUS OUTPUT
- UNDERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CURRENT AND POWER LIMITATION
- VERY LOW STAND-BY CURRENT
- PROTECTION AGAINST LOSS OF GROUND AND LOSS OF V_{CC}
- VERY LOW ELECTROMAGNETIC SUSCEPTIBILITY
- OPTIMIZED ELECTROMAGNETIC EMISSION
- REVERSE BATTERY PROTECTION (**)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

DESCRIPTION

The VNQ5050K-E is a monolithic device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSSO-24	VNQ5050K-E	VNQ5050KTR-E

Note: (**) See application schematic at page 9.

Figure 1. Package



The device detects open load condition both in on and off state, when STAT_DIS is left open or driven low. Output shorted to V_{CC} is detected in the off state.

When STAT_DIS is driven high, the STATUS pin is in a high impedance condition.

Output current limitation protects the device in overload condition. In case of long duration overload, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

Figure 2. Block Diagram

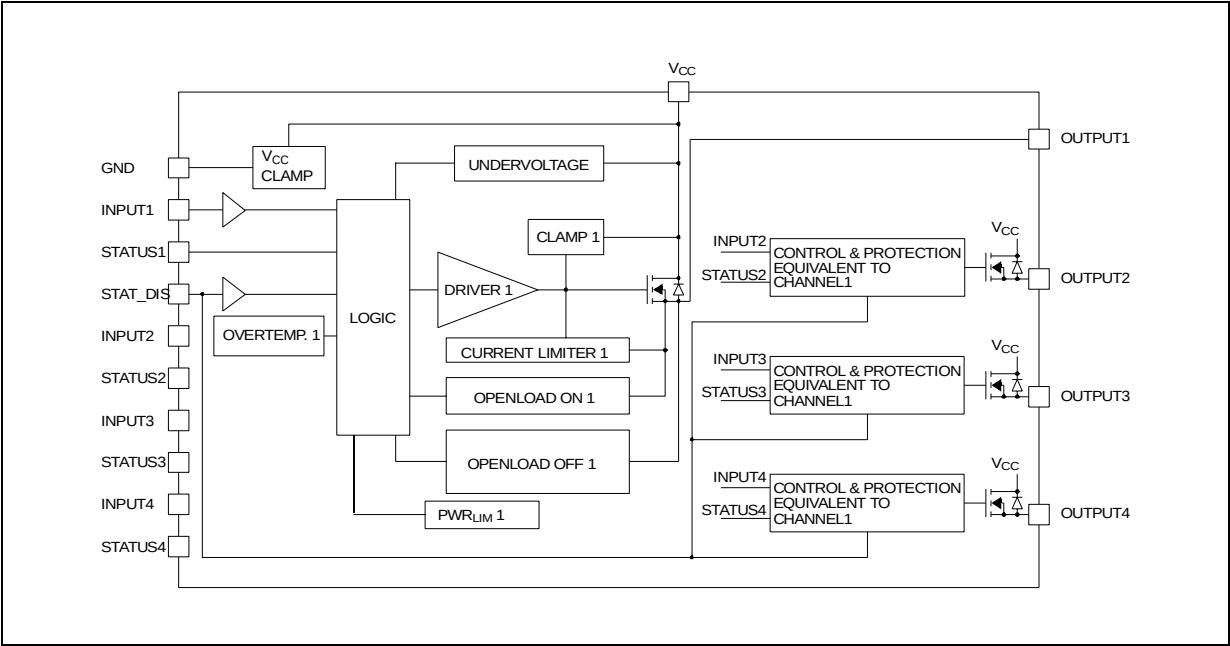


Table 3. Pin Function

Name	Function
V _{CC}	Battery connection
OUTPUT _n	Power output
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network
INPUT _n	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
STATUS _n	Open drain digital diagnostic pin
STAT_DIS	Active high CMOS compatible pin, to disable the STATUS pin

Figure 3. Current and Voltage Conventions

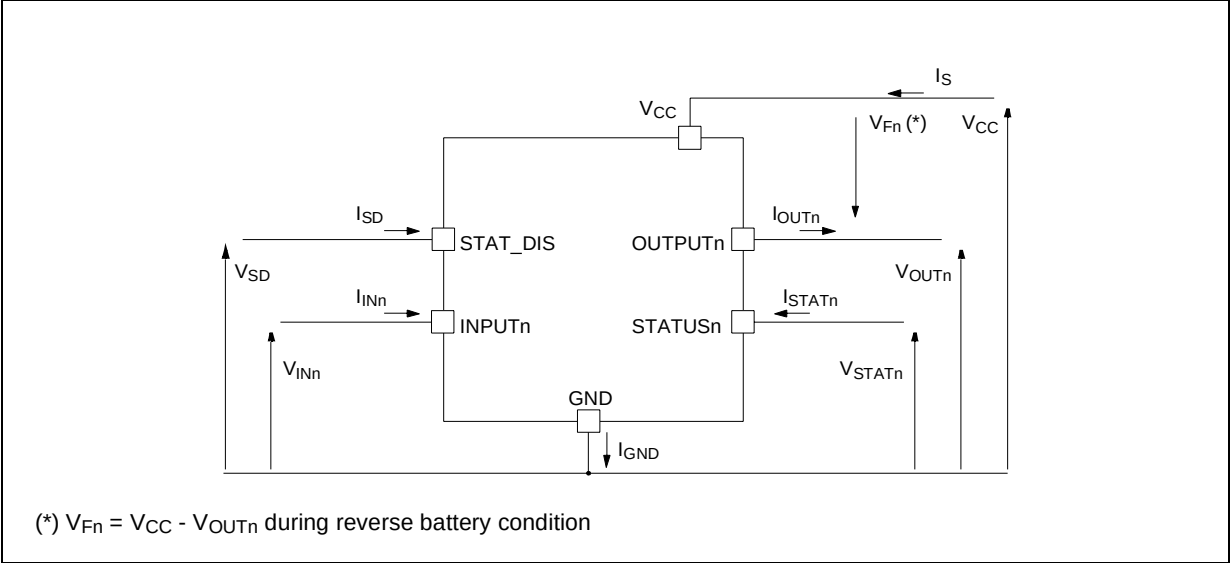
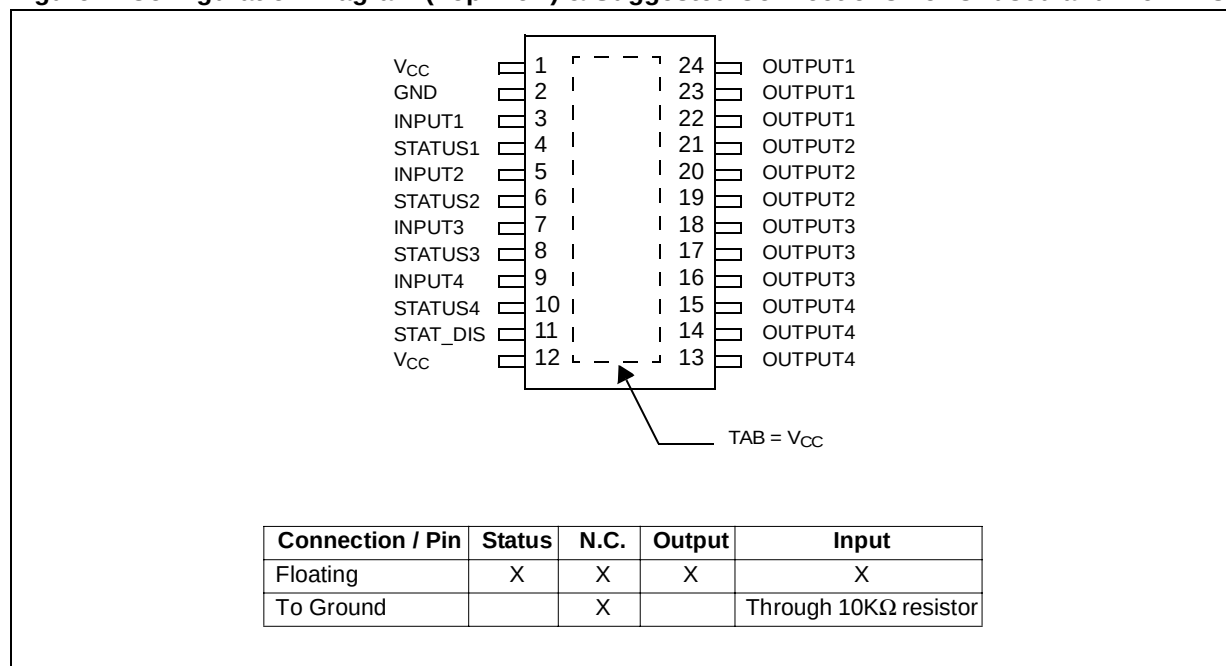


Figure 4. Configuration Diagram (Top View) & Suggested Connections For Unused and n.c. Pins**Table 4. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	41	V
- V _{CC}	Reverse DC Supply Voltage	- 0.3	V
- I _{GND}	DC Reverse Ground Pin Current	- 200	mA
I _{OUT}	DC Output Current	Internally Limited	A
- I _{OUT}	Reverse DC Output Current	- 15	A
I _{IN}	DC Input Current	+10/-1	mA
I _{STAT}	DC Status Current	+10/-1	mA
V _{ESD}	Electrostatic discharge (R=1.5kΩ; C=100pF)	2000	V
T _j	Junction Operating Temperature	-40 to 150	°C
T _{stg}	Storage Temperature	- 55 to 150	°C

Table 5. Thermal Data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal Resistance Junction-case	1.7	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	52 ⁽¹⁾	°C/W

Note: 1. When mounted on a standard single-sided FR-4 board with 1 cm² of Cu (at least 35μm thick) connected to TAB.

ELECTRICAL CHARACTERISTICS ($8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise specified)**Table 6. Power Section**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shut-down			3	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
$R_{ON}^{(**)}$	On state resistance	$I_{OUT}=2A$; $T_j=25^{\circ}C$ $I_{OUT}=2A$; $T_j=150^{\circ}C$ $I_{OUT}=2A$; $V_{CC}=5V$; $T_j=25^{\circ}C$			50 100 65	$m\Omega$ $m\Omega$ $m\Omega$
V_{clamp}	Clamp Voltage	$I_S=20\text{ mA}$	41	46	52	V
I_S	Supply current	Off State; $V_{CC}=13V$; $V_{IN}=V_{OUT}=0V$; $T_j=25^{\circ}C$ On State; $V_{IN}=5V$; $V_{CC}=13V$; $I_{OUT}=0A$		2 ⁽²⁾ 8	5 ⁽²⁾ 14	μA mA
$I_{L(off1)}^{(**)}$	Off state output current	$V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=25^{\circ}C$ $V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=125^{\circ}C$	0 0		3 5	μA μA
$I_{L(off2)}^{(**)}$	Off state output current	$V_{IN}=0V$; $V_{OUT}=4V$	-75		0	μA

Note: (**) Per each channel.

Note: 2. PowerMOS leakage included.

Table 7. Switching ($V_{CC}=13V$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$R_L=6.5\Omega$		15		μs
$t_{d(off)}$	Turn-off Delay Time	$R_L=6.5\Omega$		40		μs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	$R_L=6.5\Omega$		0.3		V/ μs
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	$R_L=6.5\Omega$		0.35		V/ μs
W_{ON}	Switching energy losses at turn-on	$R_L=6.5\Omega$		TBD		mJ
W_{OFF}	Switching energy losses at turn-off	$R_L=6.5\Omega$		TBD		mJ

ELECTRICAL CHARACTERISTICS (continued)**Table 8. Status Pin** ($V_{SD}=0$)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	$I_{STAT}=1.6\text{ mA}$, $V_{SD}=0\text{V}$			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation or $V_{SD}=5\text{V}$, $V_{STAT}=5\text{V}$			10	μA
C_{STAT}	Status Pin Input Capacitance	Normal Operation or $V_{SD}=5\text{V}$, $V_{STAT}=5\text{V}$			100	pF
V_{SCL}	Status Clamp Voltage	$I_{STAT}=1\text{mA}$ $I_{STAT}=-1\text{mA}$	5.5	-0.7	TBD	V V

Table 9. Protections (see note 3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC Short circuit current	$V_{CC}=13\text{V}$ $5\text{V}<V_{CC}<36\text{V}$	12	18	24 24	A A
I_{limL}	Short circuit current during thermal cycling	$V_{CC}=13\text{V}$ $T_R<T_J<T_{TSD}$		7		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset temperature		$T_{RS}+1$	$T_{RS}+5$		$^{\circ}\text{C}$
T_{RS}	Thermal reset of STATUS		135			$^{\circ}\text{C}$
T_{HYST}	Thermal hysteresis ($T_{TSD}-T_R$)			7		$^{\circ}\text{C}$
t_{SDL}	Status Delay in Overload Conditions	$T_J>T_{TSD}$			20	μs
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT}=2\text{A}$; $V_{IN}=0$; $L=6\text{mH}$	$V_{CC}-41$	$V_{CC}-46$	$V_{CC}-52$	V
V_{ON}	Output voltage drop limitation	$I_{OUT}=0.1\text{A}$ (see fig. 6) $T_J=-40^{\circ}\text{C}\dots+150^{\circ}\text{C}$		25		mV

Note: 3. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 10. Openload Detection

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	$V_{IN}=5\text{V}$, $8\text{V}<V_{CC}<18\text{V}$	10	40	70	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	$I_{OUT}=0\text{A}$, $V_{CC}=13\text{V}$			200	μs
t_{POL}	Delay between INPUT falling edge and STATUS rising edge in Openload condition	$I_{OUT}=0\text{A}$	200	500	1000	μs
V_{OL}	Openload OFF State Voltage Detection Threshold	$V_{IN}=0\text{V}$, $8\text{V}<V_{CC}<16\text{V}$	2	3	4	V
t_{DSTKON}	Output Short Circuit to V_{CC} Detection Delay at Turn Off		180		t_{POL}	μs

Figure 5.

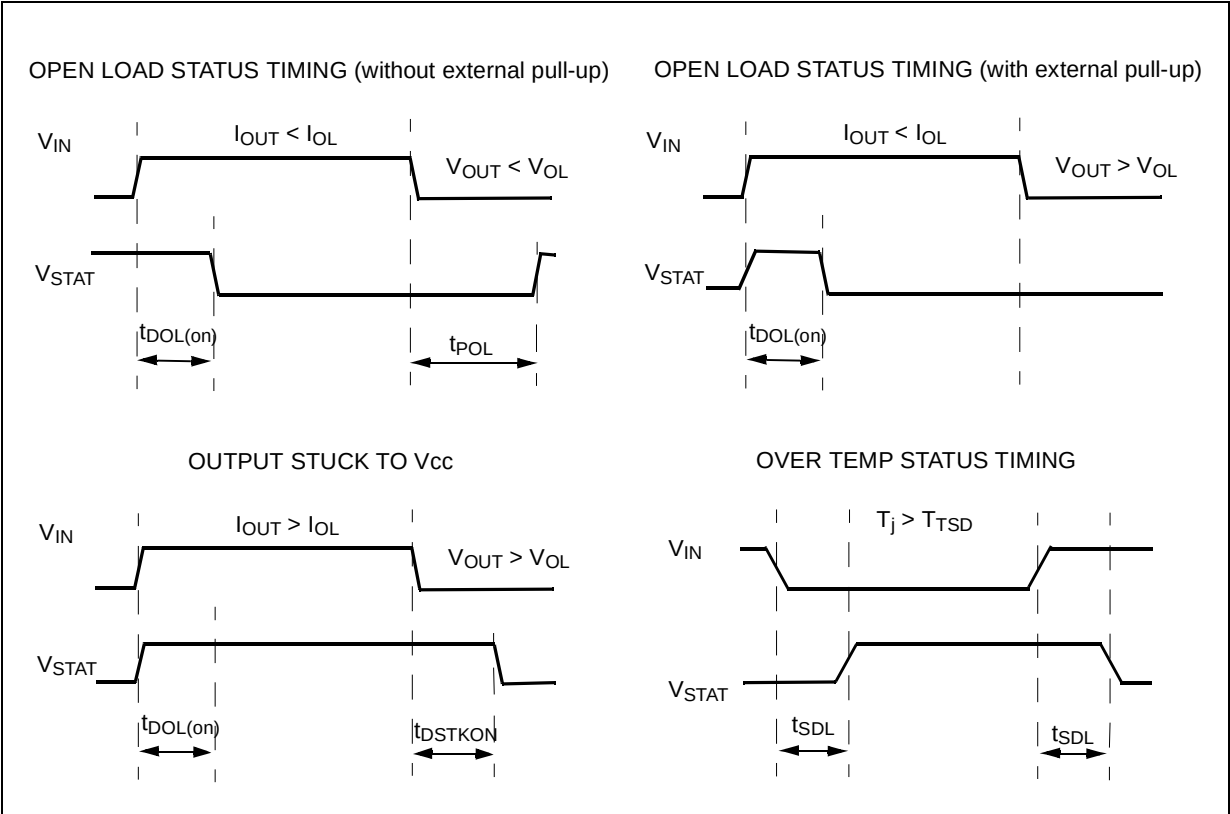
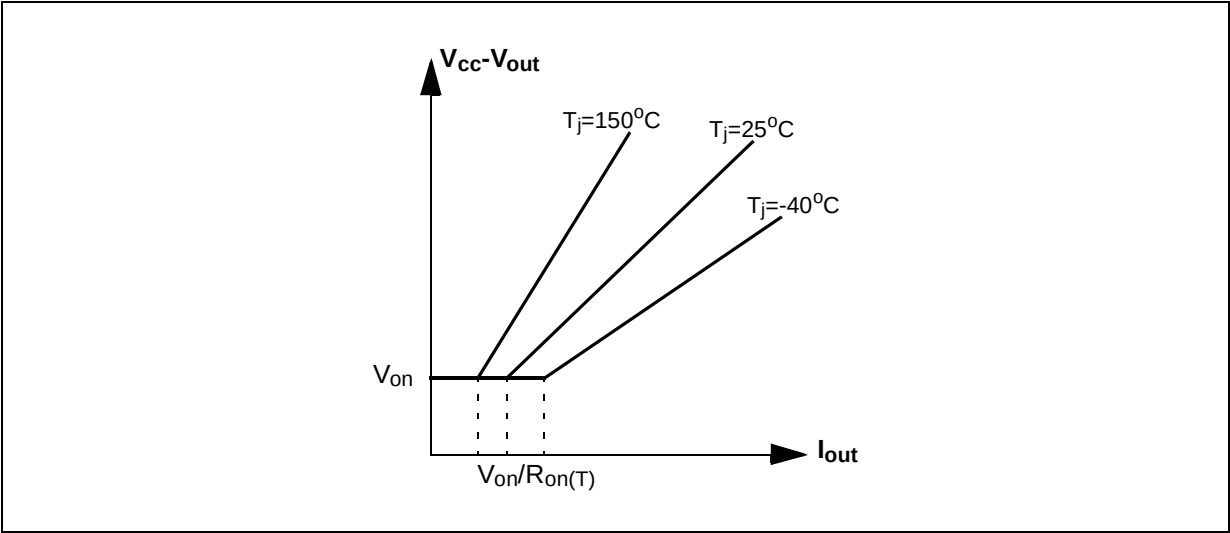


Figure 6.



ELECTRICAL CHARACTERISTICS (continued)**Table 11. Logic Input**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level				0.9	V
I_{IL}	Low Level Input Current	$V_{IN} = 0.9V$	1			μA
V_{IH}	Input High Level		2.1			V
I_{IH}	High Level Input Current	$V_{IN} = 2.1V$			10	μA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.25			V
V_{ICL}	Input Clamp Voltage	$I_{IN} = 1mA$	5.5		TBD	V
		$I_{IN} = -1mA$		-0.7		V
V_{SDL}	STAT_DIS low level voltage				0.9	V
I_{SDL}	Low level STAT_DIS current	$V_{SD}=0.9V$	1			μA
V_{SDH}	STAT_DIS high level voltage		2.1			V
I_{SDH}	High level STAT_DIS current	$V_{SD}=2.1V$			10	μA
$V_{SD(hyst)}$	STAT_DIS hysteresis voltage		0.25			V
V_{SDCL}	STAT_DIS clamp voltage	$I_{SD}=1mA$	5.5		TBD	V
		$I_{SD}=-1mA$		-0.7		V

Table 12. Truth Table

CONDITIONS	INPUTn	OUTPUTn	STATUSn ($V_{SD}=0V$) ⁽¹⁾
Normal Operation	L	L	H
	H	H	H
Current Limitation	L	L	H
	H	X	H
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Output Voltage > V_{OL}	L	H	L ⁽²⁾
	H	H	H
Output Current < I_{OL}	L	L	H ⁽³⁾
	H	H	L

Note: 1. If the V_{SD} is high, the STATUS pin is in a high impedance.

2. The STATUS pin is low with a delay equal to t_{DSTKON} after INPUT falling edge.

3. The STATUS pin becomes high with a delay equal to t_{POL} after INPUT falling edge.

Figure 7. Switching Characteristics

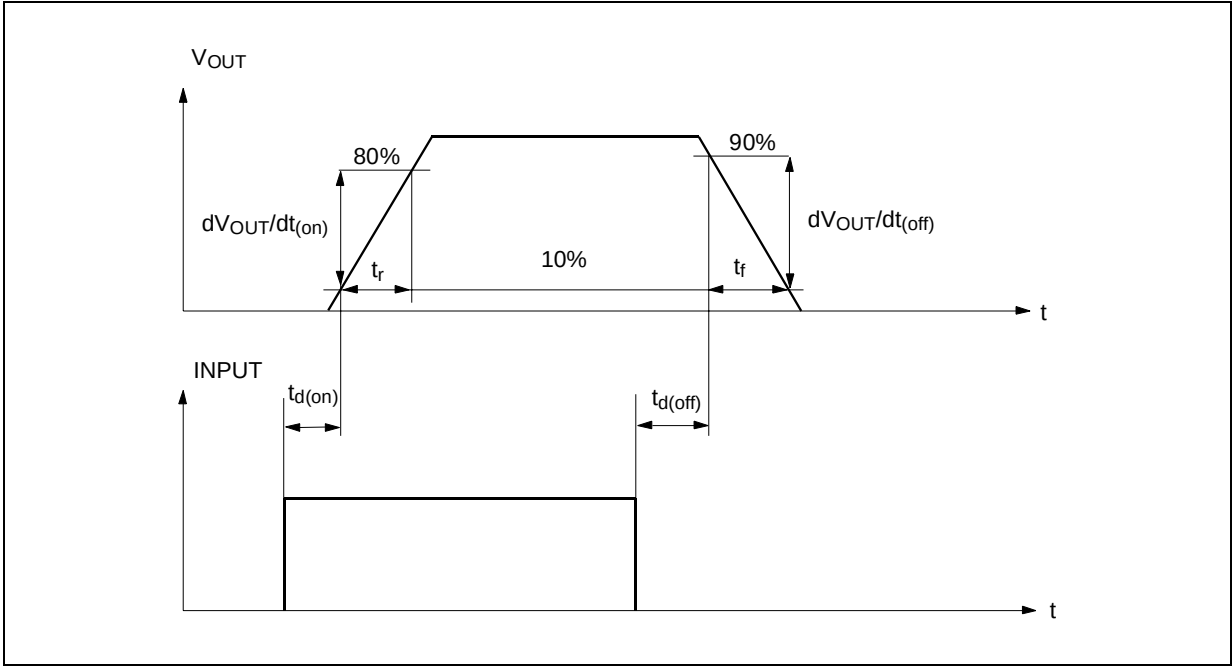


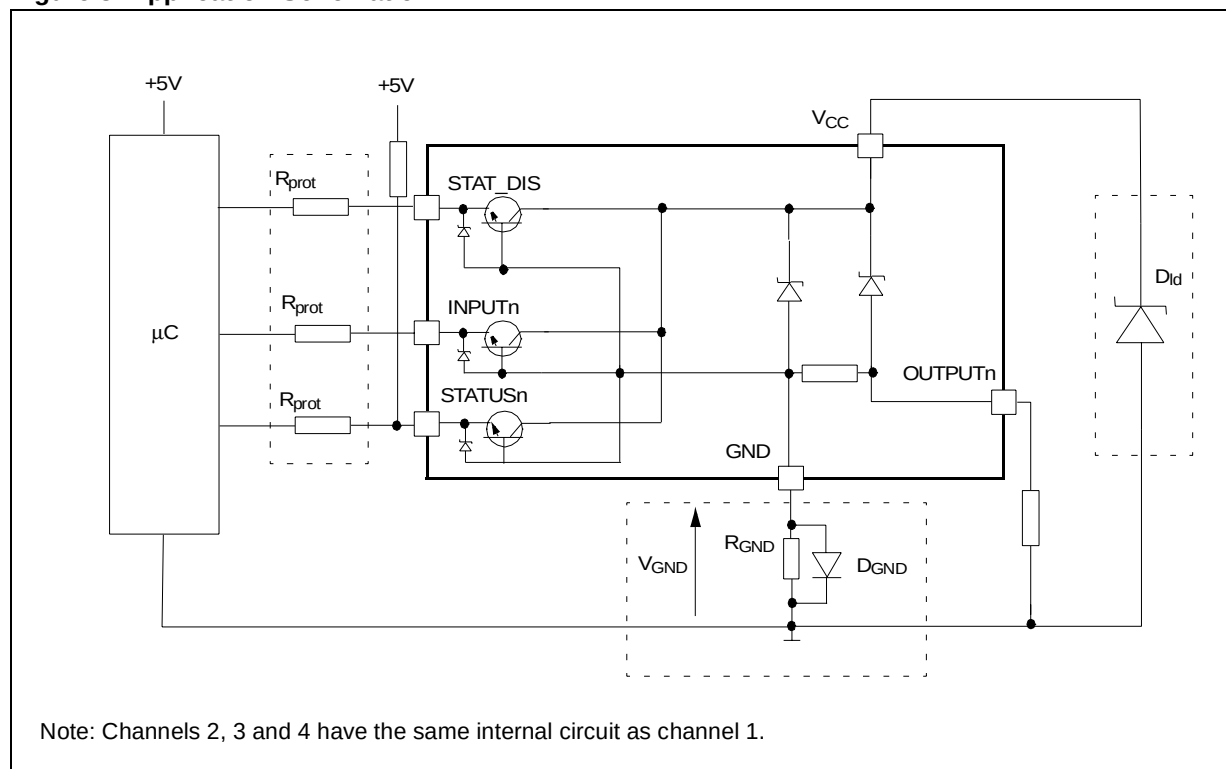
Table 13. Electrical Transient Requirements

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μ s 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μ s 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 8. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND} = 1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600\text{mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds to V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

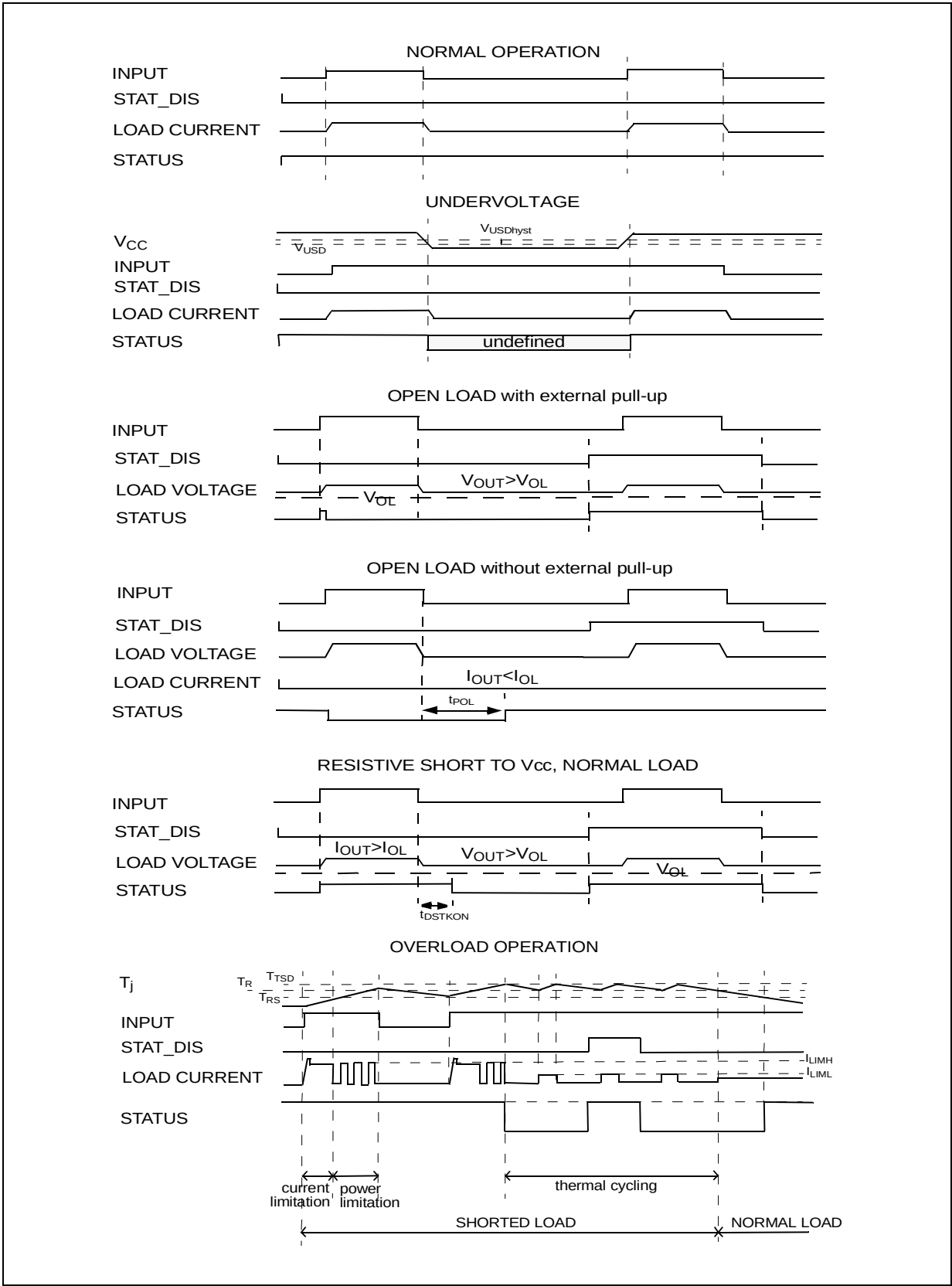
Calculation example:

For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$

$$5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega.$$

Recommended R_{prot} value is $10\text{k}\Omega$.

Figure 9. Waveforms

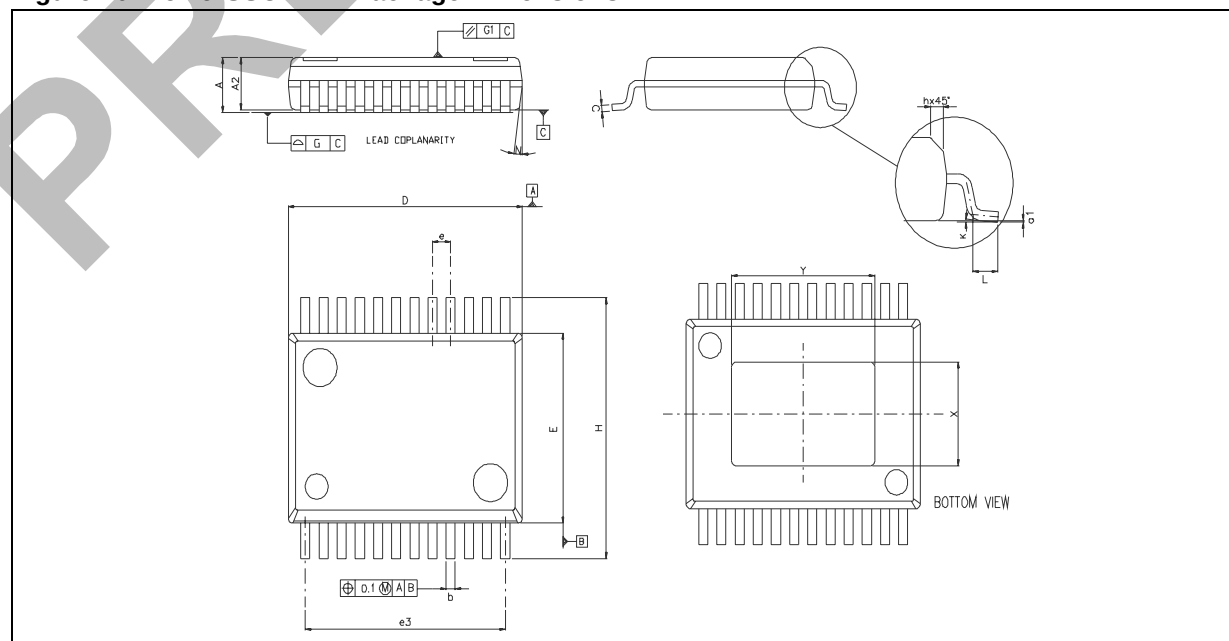


PACKAGE MECHANICAL

Table 14. PowerSSO-24™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	1.9		2.22
A2	1.9		2.15
a1	0		0.07
b	0.34	0.4	0.46
c	0.23		0.32
D	10.2		10.4
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10°
X	3.9		4.3
Y	6.1		6.5

Figure 10. PowerSSO-24™ Package Dimensions



REVISION HISTORY

Table 1. Revision History

Date	Revision	Description of Changes
Oct. 2004	1	- First issue.
Mar. 2005	2	- Minor changes

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