



4242-V_{PK} Small-Footprint and Low-Power Triple and Quad Channels Digital Isolators

 Check for Samples: [ISO7131CC](#), [ISO7140CC](#), [ISO7140FCC](#), [ISO7141CC](#), [ISO7141FCC](#)

FEATURES

- **Maximum Signaling Rate: 50 Mbps (with 5V Supplies)**
- **Robust Design With Integrated Noise Filter**
- **Default Output Low Option (Suffix F)**
- **Low Power Consumption, Typical I_{CC} per Channel (with 3.3 V Supplies):**
 - ISO7131: 1.5 mA at 1 Mbps, 2.6 mA at 25 Mbps
 - ISO7140: 1 mA at 1 Mbps, 2.3 mA at 25 Mbps
 - ISO7141: 1.3 mA at 1 Mbps, 2.6 mA at 25 Mbps
- **Low Propagation Delay: 23 ns Typical (3.3 V Supplies)**
- **Wide Temperature Range: –40°C to 125°C**
- **50 kV/μs Transient Immunity, Typical**
- **Long Life with SiO₂ Isolation Barrier**
- **Operates From 2.7 V, 3.3 V and 5 V Supply and Logic Levels**
- **Small QSOP-16 Package**

APPLICATIONS

- **General-Purpose Isolation**
 - Industrial Fieldbus
 - Profibus
 - Modbus™
 - DeviceNet Data Buses
 - RS-232, RS-485
 - Serial Peripheral Interface

SAFETY AND REGULATORY APPROVALS

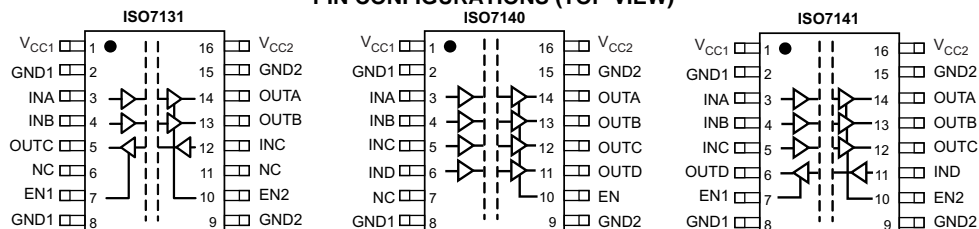
- **2500 V_{RMS} Isolation for 1 minute per UL 1577 (Approved)**
- **4242 V_{PK} Isolation per DIN EN 60747-5-2 (VDE 0884 Teil 2), 566 V_{PK} Working Voltage (Approved)**
- **CSA Component Acceptance Notice 5A (Approval Pending)**
- **IEC 60950-1 and IEC 61010-1 End Equipment Standards (Approval Pending)**
- **GB 4943.1-2011 and GB 8898:2011 CQC Certification (Approval Pending)**

DESCRIPTION

ISO7131, ISO7140, and ISO7141 provide galvanic isolation up to 2500 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. ISO7131 has three channels with two forward and one reverse-direction channels. ISO7140 and ISO7141 are quad-channel isolators; ISO7140 has four forward, ISO7141 has three forward and one reverse-direction channels. These devices are capable of 50 Mbps maximum data rate with 5V supplies and 40Mbps maximum data rate with 3.3V or 2.7V supplies, with integrated filters on the inputs for noise-prone applications. The suffix F indicates that default output state is low; otherwise, the default output state is high (see [Table 1](#)).

Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO₂) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The devices have TTL input thresholds and can operate from 2.7 V, 3.3 V, and 5 V supplies. All inputs are 5V tolerant when supplied from a 2.7V or 3.3V supply.

PIN CONFIGURATIONS (TOP VIEW)



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. FUNCTION TABLE⁽¹⁾

INPUT V _{CC}	OUTPUT V _{CC}	INPUT (IN _x)	OUTPUT ENABLE (EN _x)	OUTPUT (OUT _x)	
				ISO71xxCC	ISO71xxFCC
PU	PU	H	H or open	H	H
		L	H or open	L	L
		X	L	Z	Z
		Open	H or open	H	L
PD	PU	X	H or open	H	L
PD	PU	X	L	Z	Z
PU	PD	X	X	Undetermined	Undetermined

(1) PU = Powered Up (V_{CC} ≥ 2.7 V); PD = Powered Down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance

AVAILABLE OPTIONS

PRODUCT	RATED ISOLATION	INPUT THRESHOLD	DEFAULT OUTPUT	MAX DATA RATE and INPUT FILTER	CHANNEL DIRECTION	ORDERING NUMBER	
ISO7131CC	4242 V _{PK} ⁽¹⁾	1.5-V TTL (CMOS compatible)	High	50 Mbps, with noise filter integrated	2 forward, 1 reverse	ISO7131CCDBQ (tube)	
						ISO7131CCDBQR (reel)	
ISO7140CC			4		0	reverse	ISO7140CCDBQ (tube)
							ISO7140CCDBQR (reel)
ISO7140FCC			3		1	reverse	ISO7140FCCDBQ (tube)
							ISO7140FCCDBQR (reel)
ISO7141CC	3	1	reverse	ISO7141CCDBQ (tube)			
				ISO7141CCDBQR (reel)			
ISO7141FCC	3	1	reverse	ISO7141FCCDBQ (tube)			
				ISO7141FCCDBQR (reel)			

(1) See the [REGULATORY INFORMATION](#) section for detailed Isolation Ratings.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

PARAMETER		VALUE
Supply voltage ⁽²⁾	V_{CC1}, V_{CC2}	–0.5 V to 6 V
Input voltage	INx, ENx	–0.5 V to 6 V
Output voltage	OUTx	–0.5 V to $V_{CC} + 0.5$ V
Output current	I_O	±15 mA
Electrostatic discharge	Human-body model	ESDA / JEDEC JS-001-2012
	Field-induced charged device model	JEDEC JESD22-C101E
	All pins	±4 kV
		±1.5 kV
Maximum junction temperature	T_J	150°C
Storage temperature	T_{STG}	–65°C to 150°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	2.7		5.5	V
I_{OH}	High-level output current ($V_{CC} \geq 3.0$ V)	–4			mA
	High-level output current ($V_{CC} < 3.0$ V)	–2			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration ($V_{CC} \geq 4.5$ V)	20			ns
t_{ui}	Input pulse duration ($V_{CC} < 4.5$ V)	25			ns
$1 / t_{ui}$	Signaling rate ($V_{CC} \geq 4.5$ V)	0		50	Mbps
$1 / t_{ui}$	Signaling rate ($V_{CC} < 4.5$ V)	0		40	Mbps
T_J	Junction temperature	–40		136	°C
T_A	Ambient temperature	–40	25	125	°C

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		ISO7131, ISO714x	UNIT	
		DBQ (16 Pins)		
θ_{JA}	Junction-to-ambient thermal resistance	104.5	°C/W	
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	57.8	°C/W	
θ_{JB}	Junction-to-board thermal resistance	46.8	°C/W	
ψ_{JT}	Junction-to-top characterization parameter	18.3	°C/W	
ψ_{JB}	Junction-to-board characterization parameter	46.4	°C/W	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	°C/W	
P_D	Device power dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$ °C, $C_L = 15$ pF Input a 25-MHz, 50% duty cycle square wave	150	mW

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V \pm 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA; see Figure 1	$V_{CCx}^{(1)} - 0.5$	4.8		V
		$I_{OH} = -20$ μ A; see Figure 1	$V_{CCx}^{(1)} - 0.1$	5		
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA; see Figure 1		0.2	0.4	V
		$I_{OL} = 20$ μ A; see Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			450		mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$ at INx or ENx			10	μ A
I_{IL}	Low-level input current	$V_{IL} = 0$ V at INx or ENx	-10			
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V; see Figure 4	25	75		kV/ μ s

(1) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2} , for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V \pm 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay time	See Figure 1	12	19	35	ns
PWD ⁽¹⁾	Pulse width distortion $ t_{PHL} - t_{PLH} $				3	
$t_{sk(o)}$ ⁽²⁾	Channel-to-channel output skew time	Same-direction channels			2	
		Opposite-direction channels			4	
$t_{sk(pp)}$ ⁽³⁾	Part-to-part skew time			12		
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ} , t_{PLZ}	Disable propagation delay, high/low-to-high impedance output	See Figure 2		6	10	ns
t_{PZH} , t_{PZL}	Enable propagation delay, high impedance-to-high/low output			5	10	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.5		μ s
t_{GR}	Input glitch rejection time			11		ns

(1) Also known as pulse skew

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals, and loads.

SUPPLY CURRENT

 V_{CC1} and V_{CC2} at 5 V \pm 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
ISO7131							
I_{CC1}	Disable	EN1 = EN2 = 0V		2.2	3.7	mA	
I_{CC2}				3.7	5		
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V AC signal: All channels switching with square-wave clock input; $C_L = 15$ pF		2.2	3.7		
I_{CC2}				3.7	5		
I_{CC1}	10 Mbps			3.4	4.8		
I_{CC2}				4.9	6.6		
I_{CC1}	25 Mbps			4.9	6.6		
I_{CC2}				6.8	9		
I_{CC1}	50 Mbps			7.1	10		
I_{CC2}				10.5	13		
ISO7140							
I_{CC1}	Disable		EN = 0 V		0.6	1.2	mA
I_{CC2}				4.6	7		
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; $C_L = 15$ pF		0.6	1.3		
I_{CC2}				4.8	7		
I_{CC1}	10 Mbps			1.4	2.2		
I_{CC2}				6.9	9.2		
I_{CC1}	25 Mbps			2.7	3.9		
I_{CC2}				10.3	13.5		
I_{CC1}	50 Mbps			4.7	6.5		
I_{CC2}				15.6	21		
ISO7141							
I_{CC1}	Disable		EN1 = EN2 = 0V		2.5	4.2	mA
I_{CC2}				4.2	7		
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V, AC signal: All channels switching with square wave clock input; $C_L = 15$ pF		2.5	4.2		
I_{CC2}				4.2	7		
I_{CC1}	10 Mbps			3.8	5.3		
I_{CC2}				6.2	9.6		
I_{CC1}	25 Mbps			5.6	7.5		
I_{CC2}				9.2	13		
I_{CC1}	50 Mbps			8.4	11.2		
I_{CC2}				14	18.5		

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V \pm 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA; see Figure 1	$V_{CCx}^{(1)} - 0.5$	3		V
		$I_{OH} = -20$ μ A; see Figure 1	$V_{CCx}^{(1)} - 0.1$	3.3		
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA; see Figure 1		0.2	0.4	V
		$I_{OL} = 20$ μ A; see Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			425		mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$ at INx or ENx			10	μ A
I_{IL}	Low-level input current	$V_{IL} = 0$ V at INx or ENx	-10			
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V; see Figure 4	25	50		kV/ μ s

(1) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2} , for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V \pm 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay time	See Figure 1	15	23	45	ns
PWD ⁽¹⁾	Pulse width distortion $ t_{PHL} - t_{PLH} $				3	
$t_{sk(o)}$ ⁽²⁾	Channel-to-channel output skew time	Same-direction Channels			2	ns
		Opposite-direction Channels			4	
$t_{sk(pp)}$ ⁽³⁾	Part-to-part skew time				19	
t_r	Output signal rise time	See Figure 1		2.5		ns
t_f	Output signal fall time			2.5		
t_{PHZ} , t_{PLZ}	Disable propagation delay, from high/low to high-impedance output	See Figure 2		6.5	15	ns
t_{PZH} , t_{PZL}	Enable propagation delay, from high-impedance to high/low output			6.5	15	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		8		μ s
t_{GR}	Input glitch rejection time			12.5		ns

(1) Also known as pulse skew

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

SUPPLY CURRENT

 V_{CC1} and V_{CC2} at 3.3 V \pm 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
ISO7131							
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.9	2.7	mA	
I_{CC2}				2.6	3.8		
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V AC signal: All channels switching with square-wave clock input; $C_L = 15$ pF		1.9	2.7		
I_{CC2}				2.6	3.8		
I_{CC1}	10 Mbps			2.4	3.5		
I_{CC2}				3.5	4.7		
I_{CC1}	25 Mbps			3.2	4.6		
I_{CC2}				4.7	6.2		
I_{CC1}	40 Mbps			5	7		
I_{CC2}				7	9		
ISO7140							
I_{CC1}	Disable		EN = 0 V		0.3	0.7	mA
I_{CC2}				3.6	5.2		
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V, AC signal: All channels switching with square-wave clock input; $C_L = 15$ pF		0.4	0.8		
I_{CC2}				3.7	5.3		
I_{CC1}	10 Mbps			0.9	1.4		
I_{CC2}				5.1	6.8		
I_{CC1}	25 Mbps			1.7	2.4		
I_{CC2}				7.3	10		
I_{CC1}	40 Mbps			2.4	3.7		
I_{CC2}				9.4	13		
ISO7141							
I_{CC1}	Disable		EN1 = EN2 = 0 V		2	3.1	mA
I_{CC2}				3.2	4.9		
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V, AC signal: All channels switching with square-wave clock input; $C_L = 15$ pF		2	3.1		
I_{CC2}				3.2	4.9		
I_{CC1}	10 Mbps			2.8	3.8		
I_{CC2}				4.5	6.1		
I_{CC1}	25 Mbps			4	5.2		
I_{CC2}				6.4	8.3		
I_{CC1}	40 Mbps			5	8		
I_{CC2}				8.2	11.6		

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA; see Figure 1	$V_{CC}^{(1)} - 0.3$	2.5		V
		$I_{OH} = -20$ μ A; see Figure 1	$V_{CC}^{(1)} - 0.1$	2.7		
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA; see Figure 1		0.2	0.4	V
		$I_{OL} = 20$ μ A; see Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			350		mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$ at INx or ENx			10	μ A
I_{IL}	Low-level input current	$V_{IL} = 0$ V at INx or ENx	-10			
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V; see Figure 4	25	50		kV/ μ s

(1) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2} , for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay time	See Figure 1	15	27	50	ns
PWD ⁽¹⁾	Pulse width distortion $ t_{PHL} - t_{PLH} $		3			
$t_{sk(o)}$ ⁽²⁾	Channel-to-channel output skew time	Same-direction Channels			2	
		Opposite-direction Channels			4	
$t_{sk(pp)}$ ⁽³⁾	Part-to-part skew time				22	
t_r	Output signal rise time	See Figure 1		3		ns
t_f	Output signal fall time			3		
t_{PHZ} , t_{PLZ}	Disable propagation delay, from high/low to high-impedance output	See Figure 2		9	15	ns
t_{PZH} , t_{PZL}	Enable propagation delay, from high-impedance to high/low output			9	15	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		8.5		μ s
t_{GR}	Input glitch rejection time			14		ns

(1) Also known as pulse skew

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

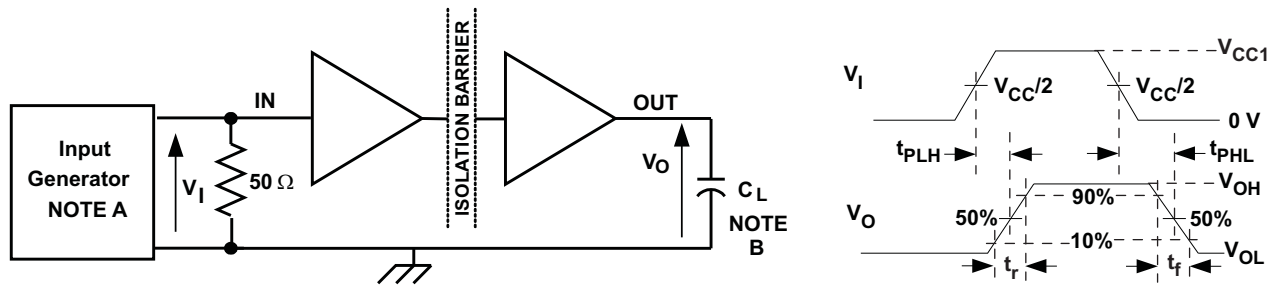
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals, and loads.

SUPPLY CURRENT

 V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted.)

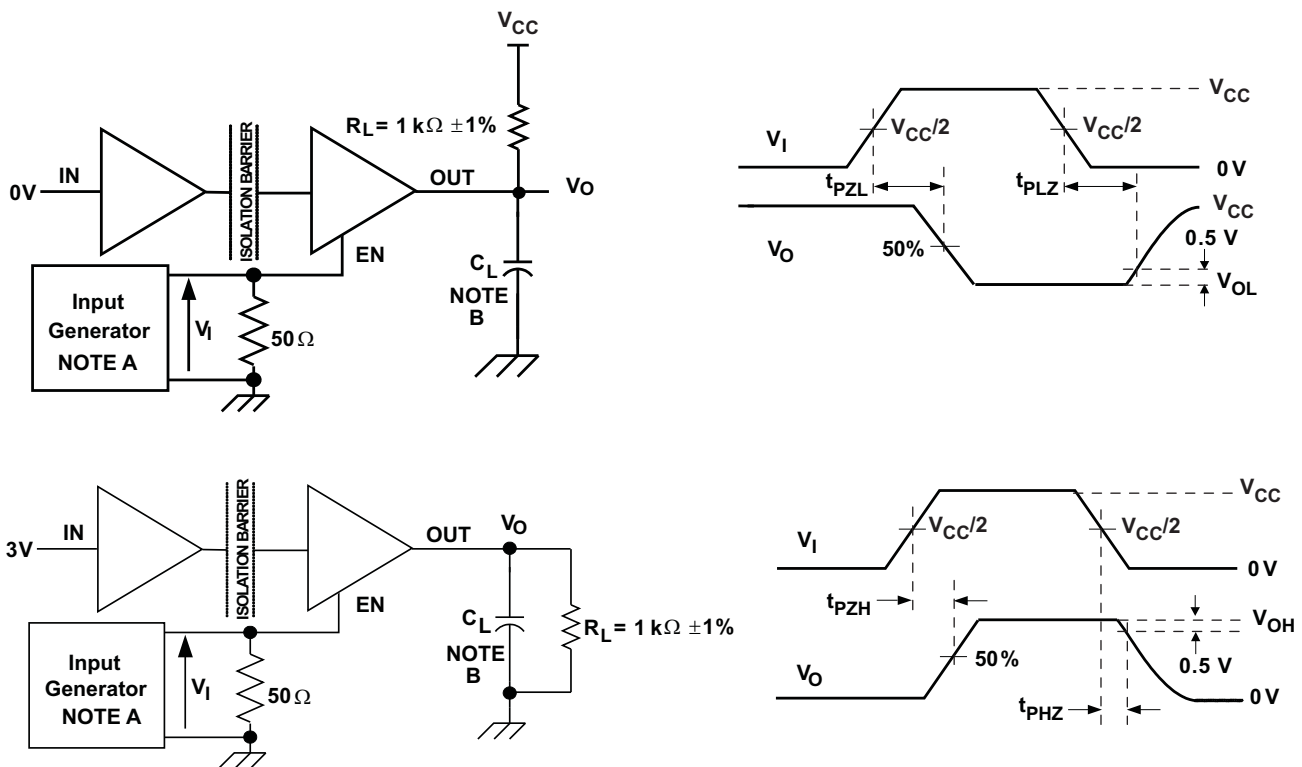
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
ISO7131							
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.2	2.4	mA	
I_{CC2}				2.3	3.3		
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V AC signal: All channels switching with square-wave clock input; $C_L = 15$ pF		1.2	2.4		
I_{CC2}				2.3	3.3		
I_{CC1}	10 Mbps			2.1	3		
I_{CC2}				2.9	4		
I_{CC1}	25 Mbps			3	3.8		
I_{CC2}				4	5.2		
I_{CC1}	40 Mbps			4.2	5.3		
I_{CC2}				5.8	7		
ISO7140							
I_{CC1}	Disable		EN = 0 V		0.2	0.4	mA
I_{CC2}				3.2	4.7		
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V, AC signal: All channels switching with square-wave clock input; $C_L = 15$ pF		0.2	0.5		
I_{CC2}				3.4	4.8		
I_{CC1}	10 Mbps			0.6	1		
I_{CC2}				4.5	6.3		
I_{CC1}	25 Mbps			1.2	1.8		
I_{CC2}				6.2	8		
I_{CC1}	40 Mbps			1.8	2.6		
I_{CC2}				8	11		
ISO7141							
I_{CC1}	Disable		EN1 = EN2 = 0 V		1.6	2.6	mA
I_{CC2}				2.8	4.1		
I_{CC1}	DC to 1 Mbps	DC signal: $V_I = V_{CC}$ or 0 V, AC signal: All channels switching with square-wave clock input; $C_L = 15$ pF		1.6	2.6		
I_{CC2}				2.8	4.1		
I_{CC1}	10 Mbps			2.3	3.2		
I_{CC2}				3.8	5		
I_{CC1}	25 Mbps			3.3	4.2		
I_{CC2}				5.4	6.8		
I_{CC1}	40 Mbps			4.3	5.8		
I_{CC2}				6.9	9.2		

PARAMETER MEASUREMENT INFORMATION



- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$. At the input, a 50- Ω resistor is required to terminate the input-generator signal. It is not needed in an actual application.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

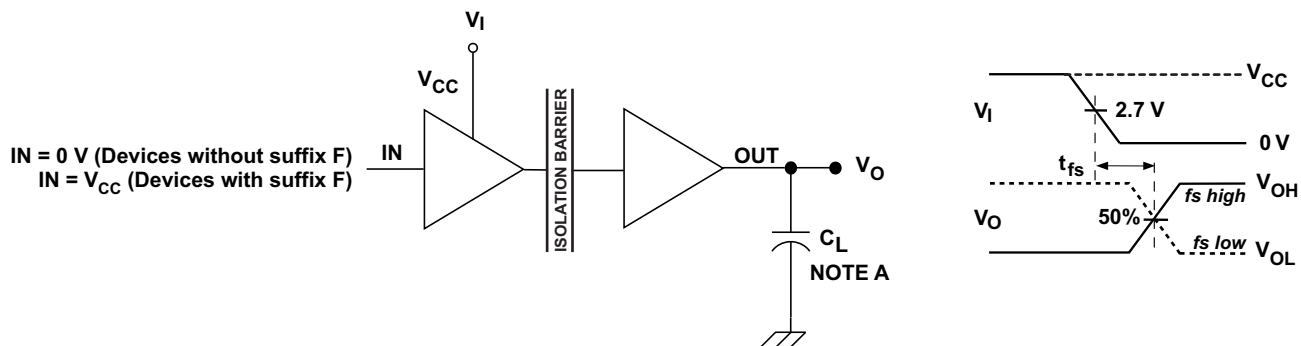
Figure 1. Switching-Characteristics Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

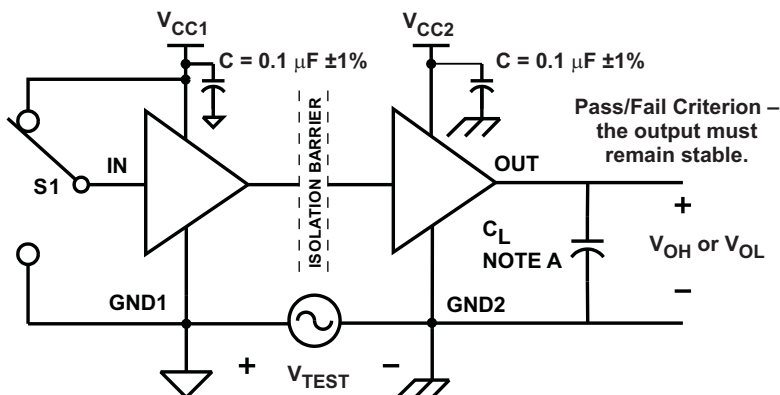
Figure 2. Enable/Disable Propagation Delay-Time Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Failsafe Delay-Time Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 4. Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

INSULATION AND SAFETY-RELATED SPECIFICATIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IOTM}	Maximum transient overvoltage per DIN EN 60747-5-2 (VDE 0884 Teil 2)				4242	V_{PK}
V_{IORM}	Maximum working voltage per DIN EN 60747-5-2 (VDE 0884 Teil 2)				566	V_{PK}
V_{ISO}	Isolation Voltage per UL 1577	$V_{TEST} = V_{ISO}$, $t = 60$ sec (qualification)			2500	V_{RMS}
		$V_{TEST} = 1.2 * V_{ISO}$, $t = 1$ sec (100% production)			3000	V_{RMS}
V_{PR}	Input-to-output test voltage	After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM} * 1.2$, $t = 10$ s, Partial discharge < 5 pC			679	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} * 1.6$, $t = 10$ s, Partial discharge < 5 pC			906	
		Method b1, 100% production test, $V_{PR} = V_{IORM} * 1.875$, $t = 1$ s, Partial discharge < 5 pC			1061	
L(I01)	Minimum air gap (clearance)	Shortest terminal to terminal distance through air	3.7			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal to terminal distance across the package surface	3.7			mm
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
	Pollution degree			2		
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
$R_{IO}^{(1)}$	Isolation Resistance, Input to Output	$V_{IO} = 500$ V, $T_A < 100^\circ\text{C}$			>10 ¹²	Ω
		$V_{IO} = 500$ V, $100^\circ\text{C} \leq T_A \leq \text{max}$			>10 ¹¹	
$C_{IO}^{(1)}$	Barrier capacitance, input to output	$V_I = 0.4 \sin(2\pi ft)$, $f = 1$ MHz			2.3	pF
$C_I^{(2)}$	Input capacitance	$V_I = V_{CC}/2 + 0.4 \sin(2\pi ft)$, $f = 1$ MHz, $V_{CC} = 5$ V			2.8	pF

- (1) All pins on each side of the barrier tied together creating a two-terminal device.
 (2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

Table 2. IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–III
	Rated mains voltage ≤ 400 V_{RMS}	I–II

REGULATORY INFORMATION

VDE	UL	CSA	CQC
Certified according to DIN EN 60747-5-2	Recognized under 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice	Certified according to GB 4943.1-2011 and GB 8898:2011
Basic Insulation Maximum Transient Overvoltage, 4242 V _{PK} Maximum Working Voltage, 566 V _{PK}	Single protection, 2500 V _{RMS} ⁽¹⁾	Reinforced Insulation per CSA 60950-1-03 and IEC 60950-1 (2nd Ed.), 150 V _{RMS} maximum working voltage Basic Insulation per CSA 60950-1-03 and IEC 60950-1 (2nd Ed.), 380 V _{RMS} maximum working voltage Reinforced Insulation per CSA 61010-1-04 and IEC 61010-1 (2nd Edition), 150 V _{RMS} maximum working voltage	Basic Insulation, Altitude ≤ 5000m, Tropical Climate, 250 VRMS maximum working voltage
File number: 40016131	File number: E181974	File number: 220991 (approval pending)	Report Number: Pending

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT	
I _S	Safety input, output, or supply current	DBQ-16	θ _{JA} = 104.5°C/W, V _I = 5.5V, T _J = 150°C, T _A = 25°C					217	mA
			θ _{JA} = 104.5°C/W, V _I = 3.6V, T _J = 150°C, T _A = 25°C					332	
			θ _{JA} = 104.5°C/W, V _I = 2.7V, T _J = 150°C, T _A = 25°C					443	
T _S	Maximum case temperature						150	°C	

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

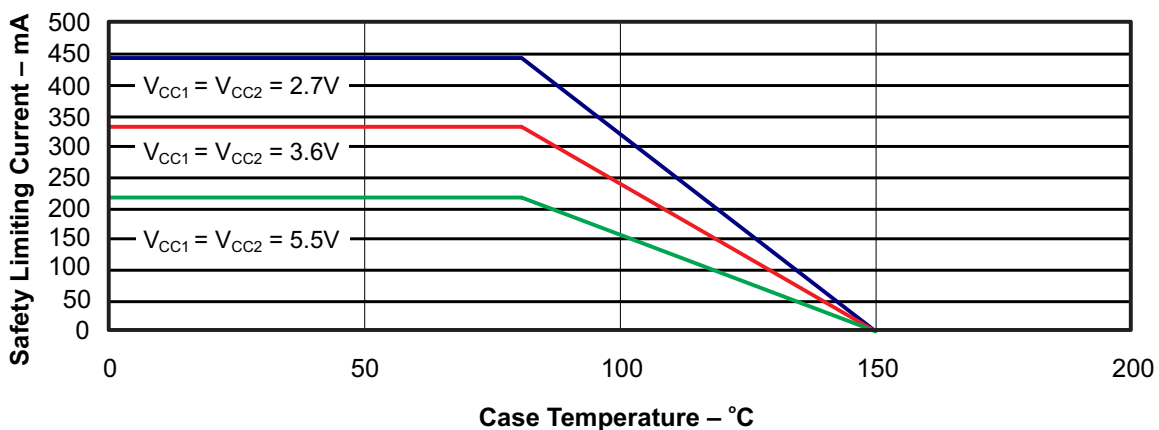


Figure 5. DBQ-16 θ_{Jc} Thermal Derating Curve

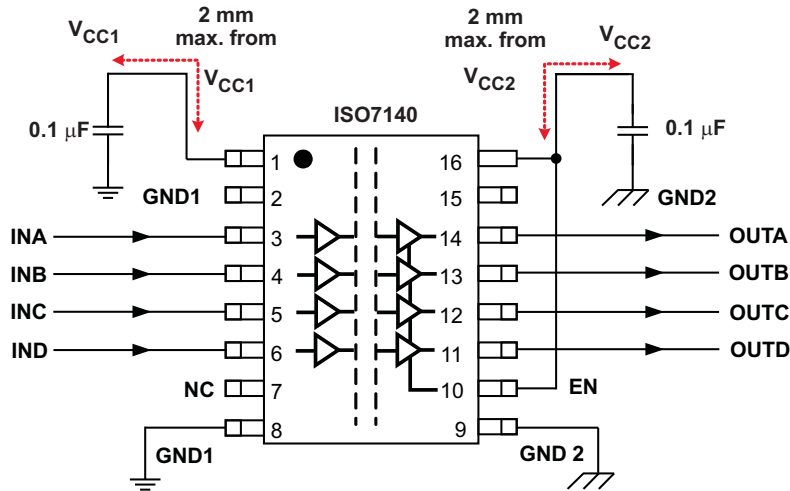
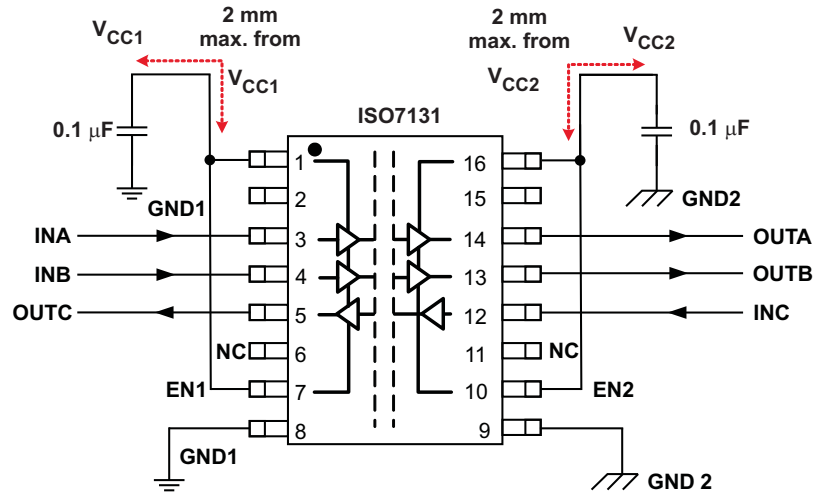


Figure 6. Typical Application Circuits for ISO7131 and ISO7140

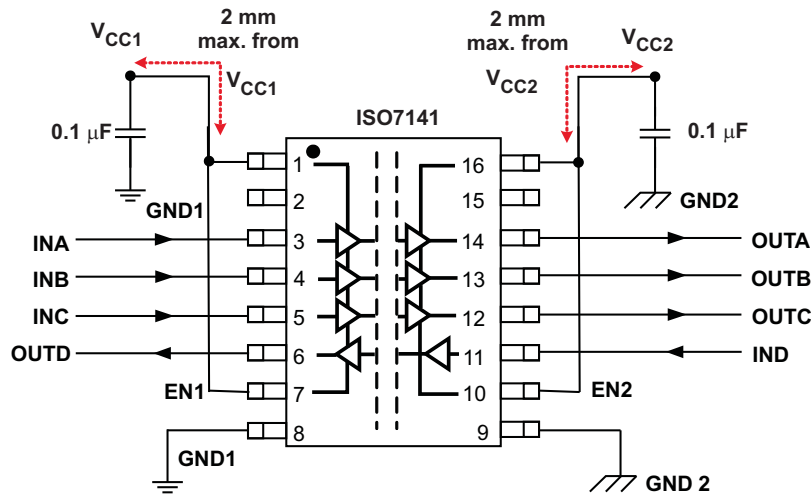


Figure 7. Typical Application Circuit for ISO7141

Note: For detailed layout recommendations, see Application Note [SLLA284](#), *Digital Isolator Design Guide*.

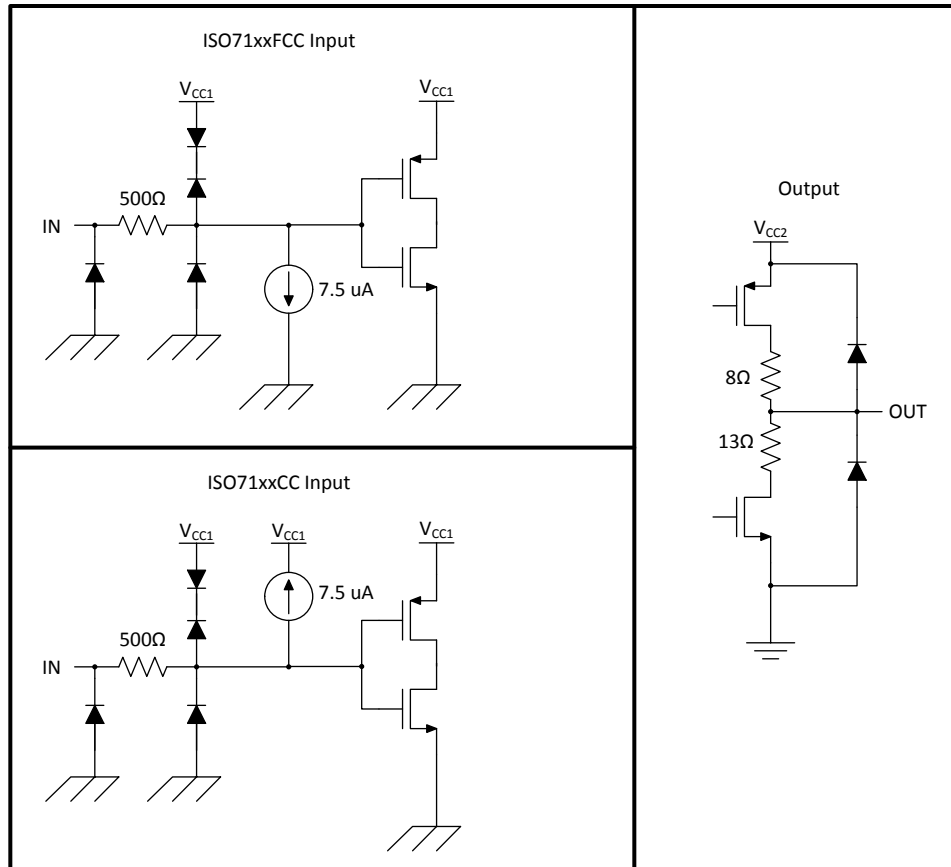


Figure 8. Device I/O Schematics

TYPICAL CHARACTERISTICS

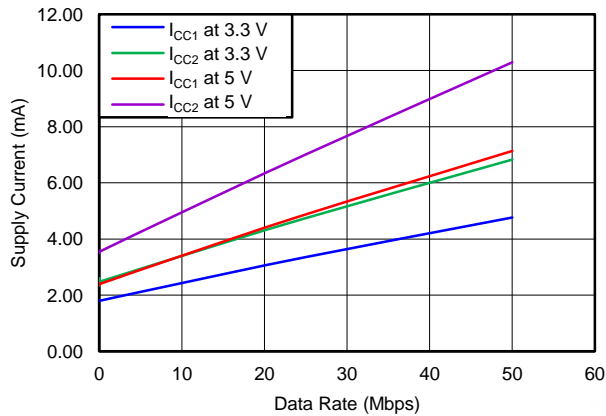


Figure 9. ISO7131 SUPPLY CURRENT FOR ALL CHANNELS vs DATA RATE

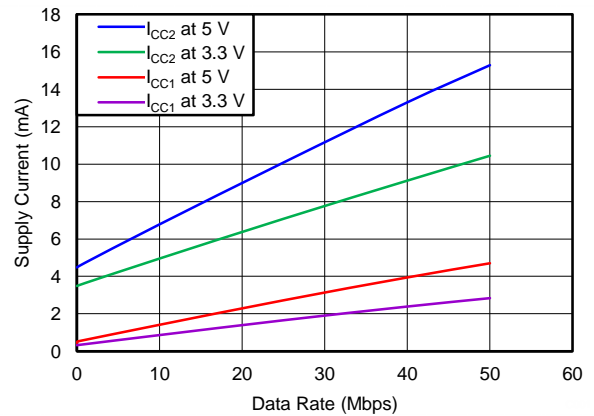


Figure 10. ISO7140 SUPPLY CURRENT FOR ALL CHANNELS vs DATA RATE

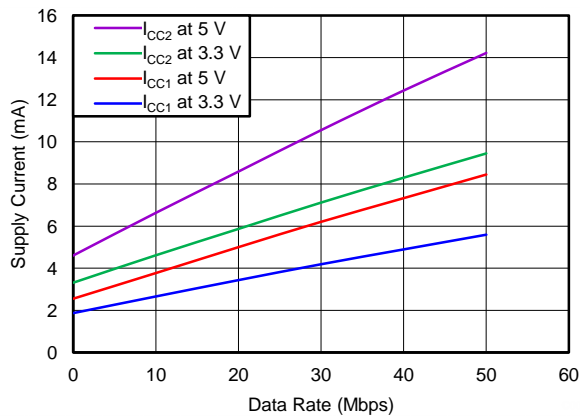


Figure 11. ISO7141 SUPPLY CURRENT FOR ALL CHANNELS vs DATA RATE

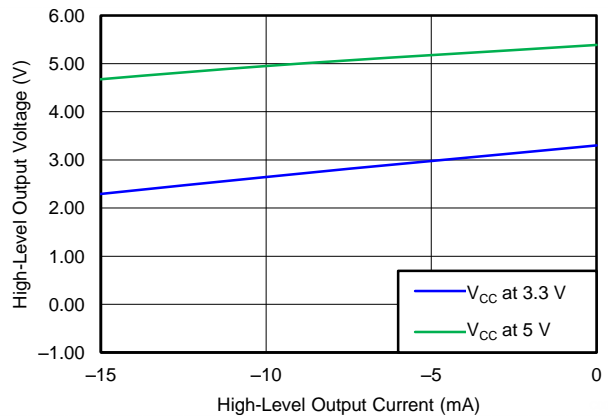


Figure 12. HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

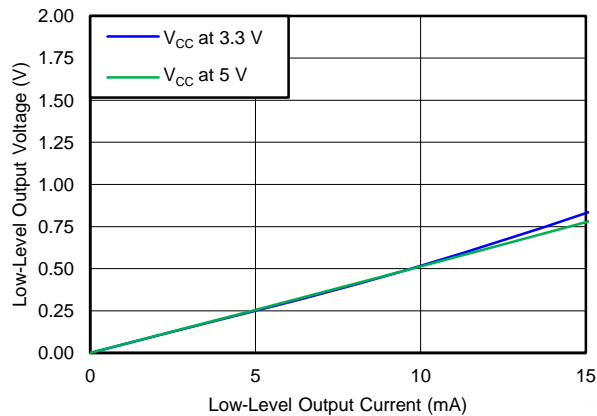


Figure 13. LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

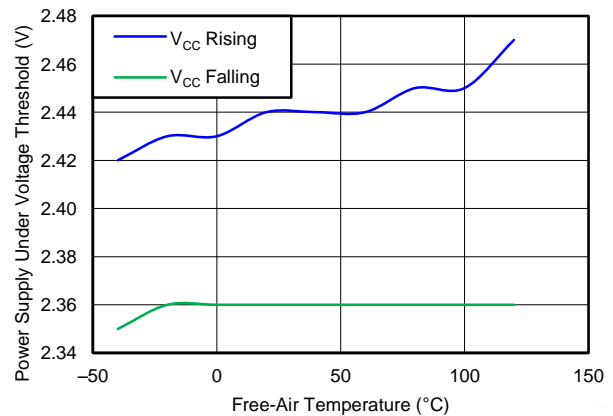


Figure 14. V_{CC} UNDERVOLTAGE THRESHOLD vs FREE-AIR TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

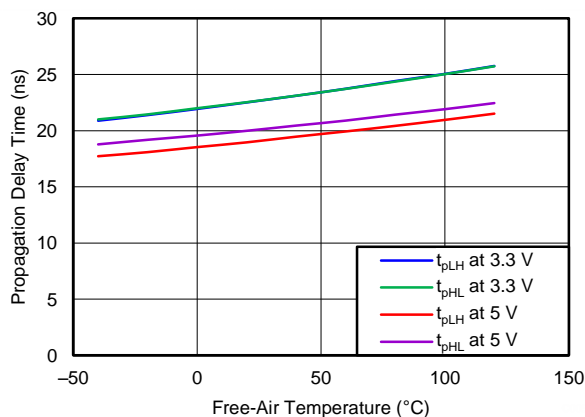


Figure 15. PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

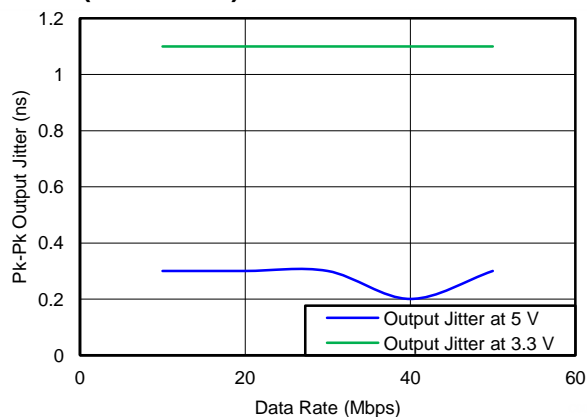


Figure 16. OUTPUT JITTER vs DATA RATE

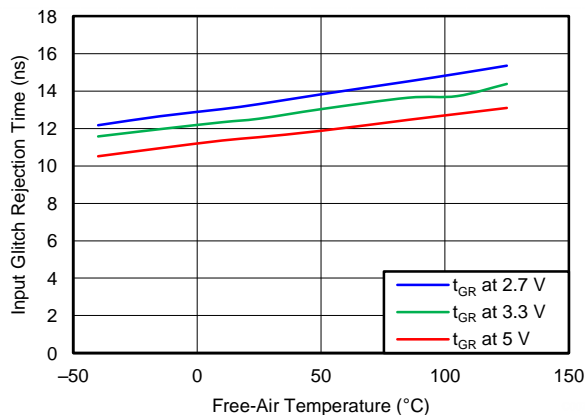


Figure 17. INPUT GLITCH REJECTION vs FREE-AIR TEMPERATURE

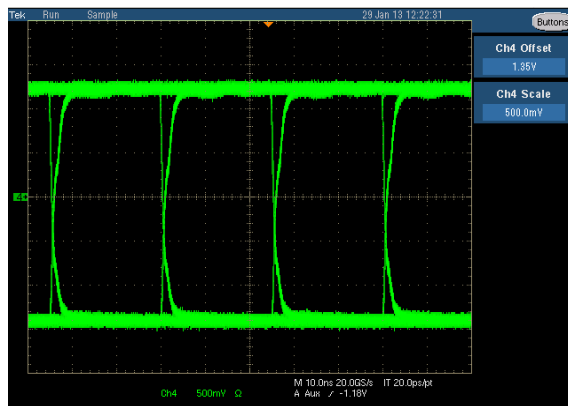


Figure 18. TYPICAL EYE DIAGRAM AT 40 MBPS, PRBS 2¹⁶ - 1, 2.7-V OPERATION

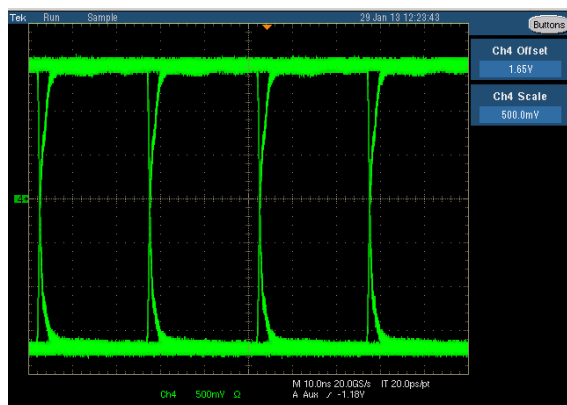


Figure 19. TYPICAL EYE DIAGRAM AT 40 MBPS, PRBS 2¹⁶ - 1, 3.3-V OPERATION

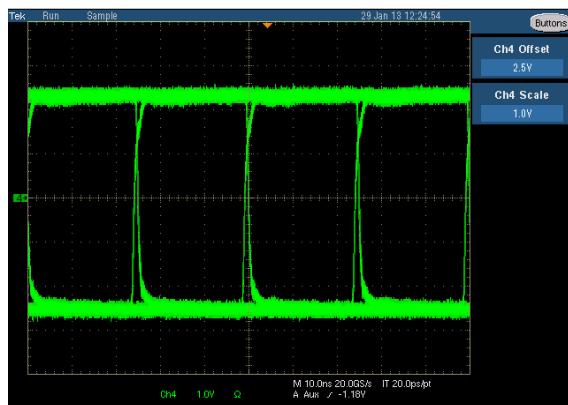


Figure 20. TYPICAL EYE DIAGRAM AT 50 MBPS, PRBS 2¹⁶ - 1, 5-V OPERATION

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time. Values by device.	4
• Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time. Values by device.	6
• Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time. Values by device.	8
• Added Figure 11	16

Changes from Revision A (June 2013) to Revision B	Page
• Changed device ISO7141CC From: Product Preview To: Released in the Product Status table	1

Changes from Revision B (June 2013) to Revision C	Page
• Changed Feature From: ISO7140: TBD at 1 Mbps, TBD at 25 Mbps To: ISO7140: 1 mA at 1 Mbps, 2.3 mA at 25 Mbps	1
• Changed the SAFETY and REGULATORY APPROVALS	1
• Added text to the Description: "All inputs are 5V tolerant when supplied from a 2.7V or 3.3V supply."	1
• Deleted the Product Status table	1
• Changed the AVAILABLE OPTIONS table	2
• Changed the ABSOLUTE MAXIMUM RATINGS table	3
• Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time.	4
• Changed ISO7140 in the SUPPLY CURRENT table From: TBD To: values	5
• Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time.	6
• Changed ISO7140 in the SUPPLY CURRENT table From: TBD To: values	7
• Changed the SWITCHING CHARACTERISTICS table, Input glitch rejection time.	8
• Changed ISO7140 in the SUPPLY CURRENT table From: TBD To: values	9
• Changed Figure 9 X-axis scale	16

Changes from Revision C (July 2013) to Revision D	Page
• Added Safety List item "GB 4943.1-2011 and GB 8898:2011 CQC Certification (Approval Pending)"	1
• Deleted "Product Preview" From the AVAILABLE OPTIONS table	2
• Changed the REGULATORY INFORMATION, added column for CQC	13
• Added Figure 10	16

Changes from Revision D (August 2013) to Revision E	Page
• Changed From: 2500 V _{RMS} Isolation for 1 minute per UL 1577 (Approval Pending) To: (Approved)	1
• Added note1 to the AVAILABLE OPTIONS table	2
• Changed From: Basic Insulation To: Basic Insulation, Altitude ≤ 5000m, Tropical Climate, 250 VRMS maximum working voltage in the Regulatory Information table	13
• Changed File number: E181974 (approval pending) To: File number: E181974 in the Regulatory Information table	13
• Changed Figure 5	13
• Changed the title of Figure 18 , Figure 19 , and Figure 19 to include "PRBS 2 ¹⁶ - 1"	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7131CCDBQ	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7131CC	Samples
ISO7131CCDBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7131CC	Samples
ISO7140CCDBQ	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7140CC	Samples
ISO7140CCDBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7140CC	Samples
ISO7140FCCDBQ	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7140FC	Samples
ISO7140FCCDBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7140FC	Samples
ISO7141CCDBQ	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7141CC	Samples
ISO7141CCDBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7141CC	Samples
ISO7141FCCDBQ	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7141FC	Samples
ISO7141FCCDBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7141FC	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

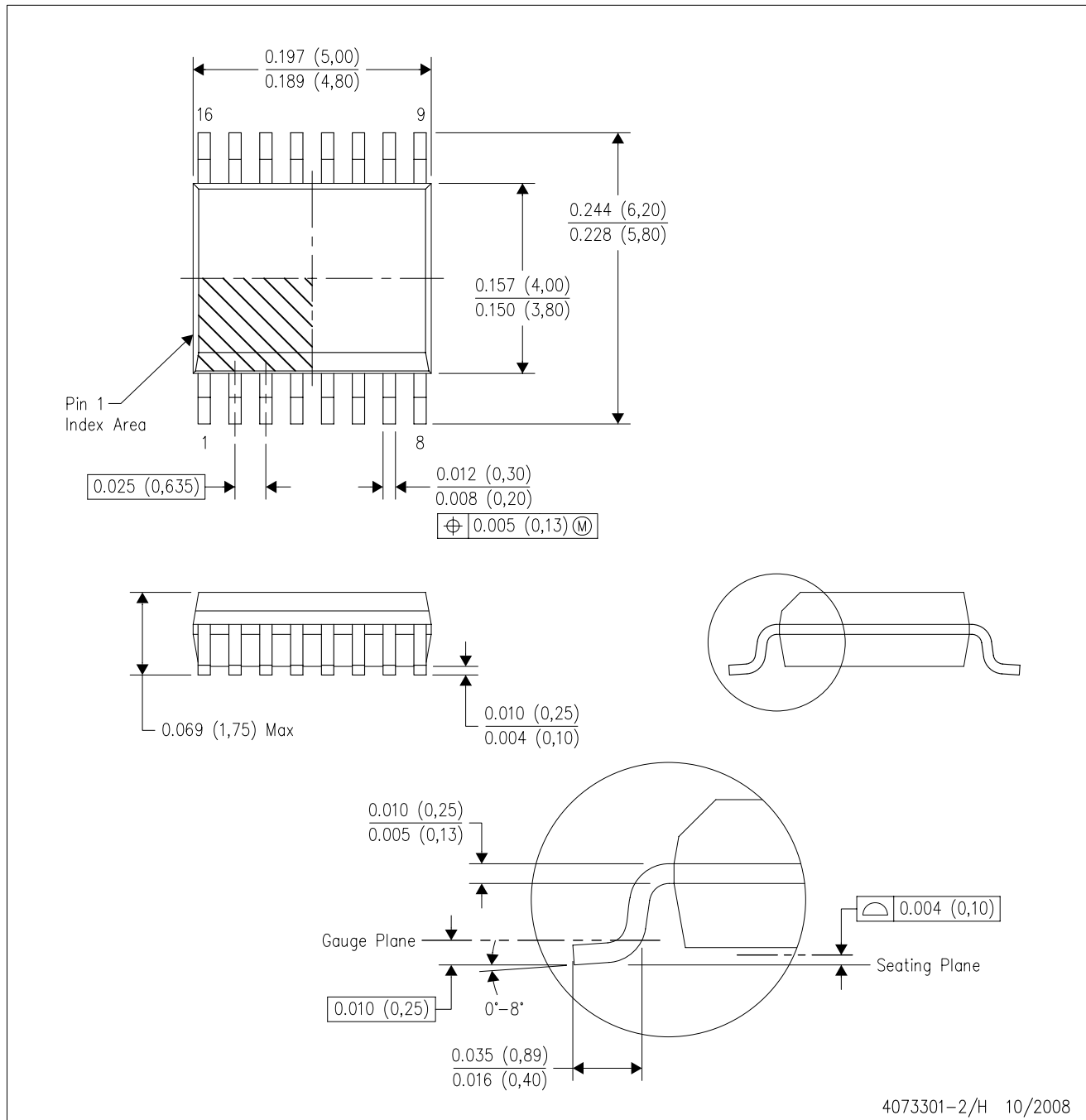
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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DBQ (R-PDSO-G16)

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 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AB.

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