



Precision, Gain of 0.2 Level Translation DIFFERENCE AMPLIFIER

FEATURES

- **GAIN OF 0.2 TO INTERFACE $\pm 10\text{V}$ SIGNALS TO SINGLE-SUPPLY ADCs**
- **GAIN ACCURACY: $\pm 0.024\%$ (max)**
- **WIDE BANDWIDTH: 1.5MHz**
- **HIGH SLEW RATE: $15\text{V}/\mu\text{s}$**
- **LOW OFFSET VOLTAGE: $\pm 100\mu\text{V}$**
- **LOW OFFSET DRIFT: $\pm 1.5\mu\text{V}/^\circ\text{C}$**
- **SINGLE-SUPPLY OPERATION DOWN TO 1.8V**

APPLICATIONS

- INDUSTRIAL PROCESS CONTROLS
- INSTRUMENTATION
- DIFFERENTIAL TO SINGLE-ENDED CONVERSION
- AUDIO LINE RECEIVERS

DESCRIPTION

The INA159 is a high slew rate, $G = 1/5$ difference amplifier consisting of a precision op amp with a precision resistor network. The gain of $1/5$ makes the INA159 useful to couple $\pm 10V$ signals to single-supply analog-to-digital converters (ADCs), particularly those operating on a single +5V supply. The on-chip resistors are laser-trimmed for accurate gain and high common-mode rejection. Excellent temperature coefficient of resistance (TCR) tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The input common-mode voltage range extends beyond the positive and negative supply rails. It operates on a total of +1.8V to +5.5V single or split supplies. The INA159 reference input uses two resistors for easy mid-supply or reference biasing.

The difference amplifier is the foundation of many commonly-used circuits. The INA159 provides this circuit function without using an expensive external precision resistor network. The INA159 is available in an MSOP-8 surface-mount package and is specified for operation over the extended industrial temperature range, -40°C to $+125^{\circ}\text{C}$.

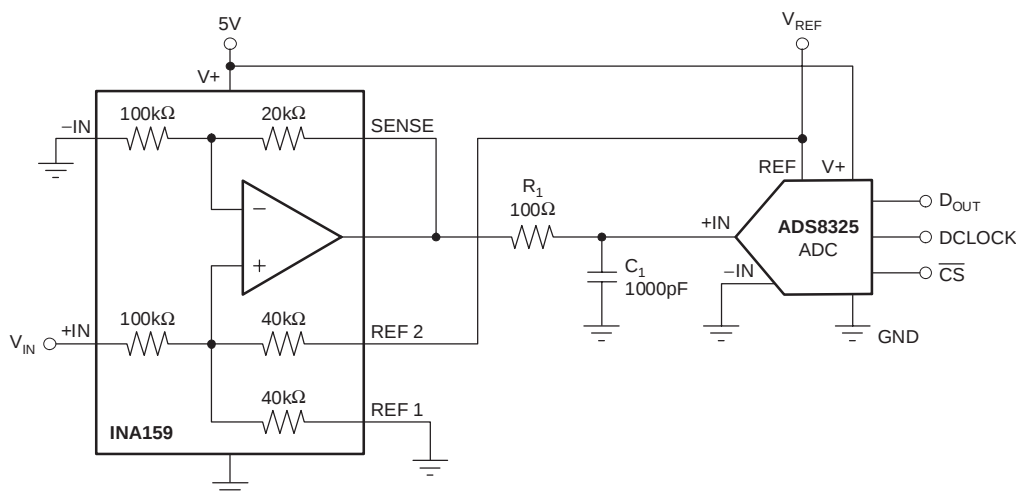


Figure 1. Typical Application



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	+5.5V
Signal Input Terminals (–IN and +IN), Voltage	±30V
Reference (REF 1 and REF2) and Sense Pins	
Current	±10mA
Voltage	(V–) – 0.5V to (V+) + 0.5V
Output Short Circuit	Continuous
Operating Temperature	–40°C to +150°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
ESD Rating	
Human Body Model	4000V
Charged Device Model	1000V

⁽¹⁾ Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

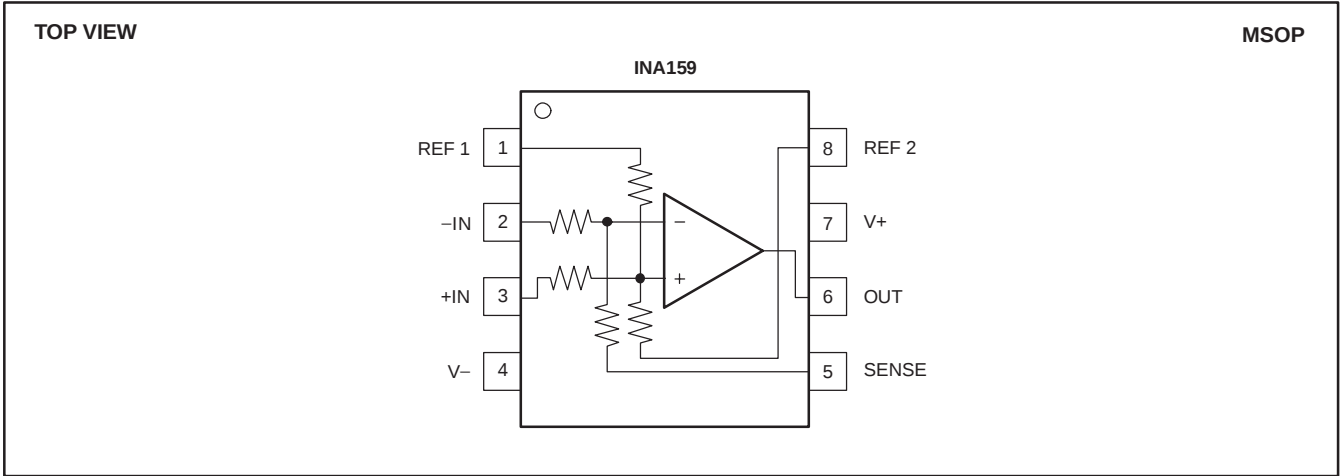
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA159	MSOP-8	DGK	CJB

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS



ELECTRICAL CHARACTERISTICS: $V_S = +5V$
Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

At $T_A = +25^{\circ}\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{REF} = 5V$, unless otherwise noted.

PARAMETER	CONDITIONS	INA159			UNIT
		MIN	TYP	MAX	
OFFSET VOLTAGE⁽¹⁾ Initial (1) V_{OS} vs Temperature vs Power Supply PSRR Reference Divider Accuracy ⁽²⁾ over Temperature	RTO $V_S = \pm 2.5V$, Reference and Input Pins Grounded $V_S = \pm 0.9V$ to $\pm 2.75V$		± 100 ± 1.5 ± 20 ± 0.002 ± 0.002	± 500 ± 100 ± 0.024	μV $\mu V/^{\circ}\text{C}$ $\mu V/V$ % %
INPUT IMPEDANCE⁽³⁾ Differential Common-Mode			240 60		$\text{k}\Omega$ $\text{k}\Omega$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Positive Negative Common-Mode Rejection Ratio over Temperature	RTI $V_{CM} = -10V$ to $+10V$, $R_S = 0\Omega$	80	17.5 -12.5 96 94		V V dB dB
OUTPUT VOLTAGE NOISE⁽⁴⁾ $f = 0.1\text{Hz}$ to 10Hz $f = 10\text{kHz}$	RTO		10 30		μV_{PP} $\text{nV}/\sqrt{\text{Hz}}$
GAIN Initial Error vs Temperature Nonlinearity	$V_{REF2} = 4.096V$, R_L Connected to GND, $(V_{IN+}) - (V_{IN-}) = -10V$ to $+10V$, $V_{CM} = 0V$ G		0.2 ± 0.005 ± 1 ± 0.0002	± 0.024	V/V % ppm/^{\circ}\text{C} % of FS
OUTPUT Voltage, Positive Voltage, Negative Current Limit, Continuous to Common Capacitive Load Open-Loop Output Impedance	$V_{REF2} = 4.096V$, R_L Connected to GND $V_{REF2} = 4.096V$, R_L Connected to GND $f = 1\text{MHz}$, $I_O = 0$	$(V+) - 0.1$ $(V-) + 0.048$ See Typical Characteristic	$(V+) - 0.02$ $(V-) + 0.01$ ± 60 110		V V mA pF Ω
FREQUENCY RESPONSE Small-Signal Bandwidth Slew Rate Settling Time, 0.01% Overload Recovery Time	-3dB SR t_S 4V Output Step, $C_L = 100\text{pF}$ 50% Overdrive		1.5 15 1 250		MHz V/ μs μs ns
POWER SUPPLY Specified Voltage Range Operating Voltage Range Quiescent Current	V_S $I_Q = 0\text{mA}$, $V_S = \pm 2.5V$, Reference and Input Pins Grounded I_Q	+1.8	+5 1.1	+5.5 1.5	V V mA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance MSOP-8	 θ_{JA} Surface-Mount	-40 -40 -65		+125 +150 +150	$^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C}/\text{W}$

(1) Includes effects of amplifier input bias and offset currents.

(2) Reference divider accuracy specifies the match between the reference divider resistors using the configuration in Figure 2.

(3) Internal resistors are ratio matched but have $\pm 20\%$ absolute value.

(4) Includes effects of amplifier input current noise and thermal noise contribution of resistor network.

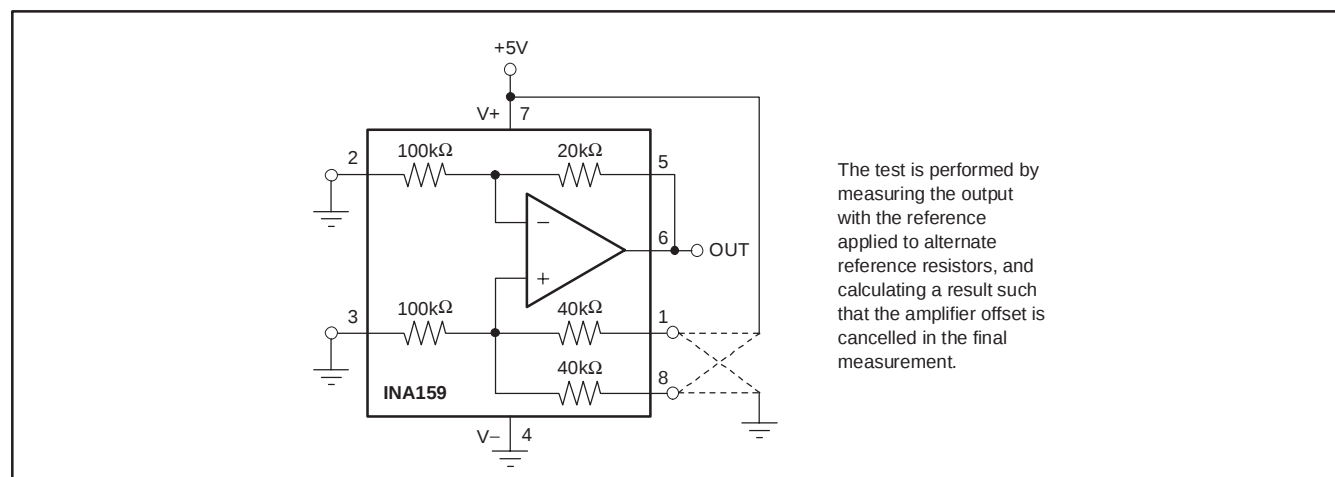
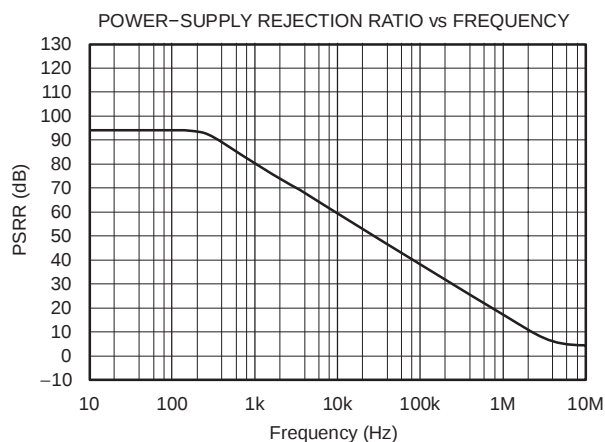
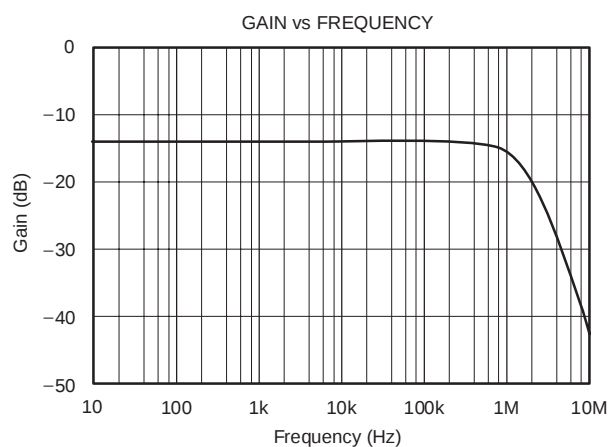
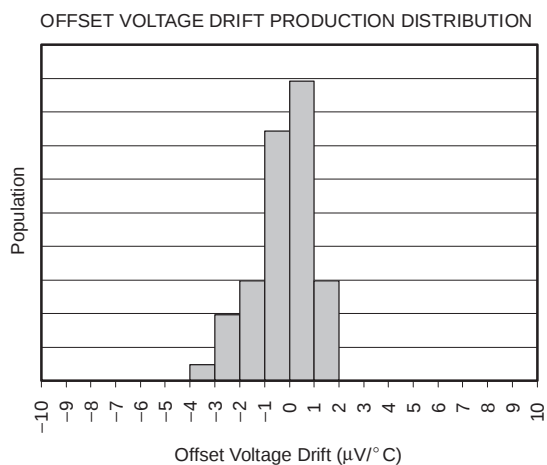
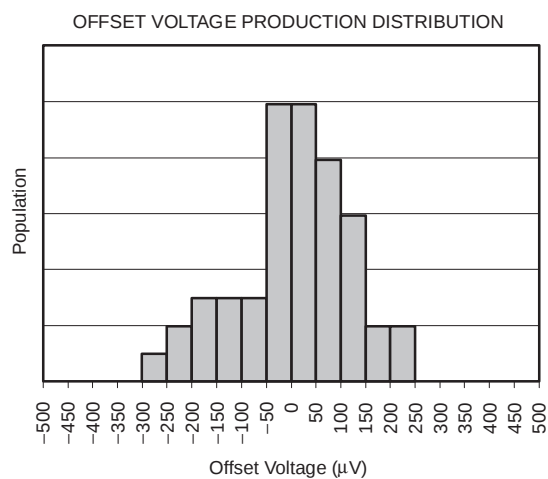


Figure 2. Test Circuit for Reference Divider Accuracy

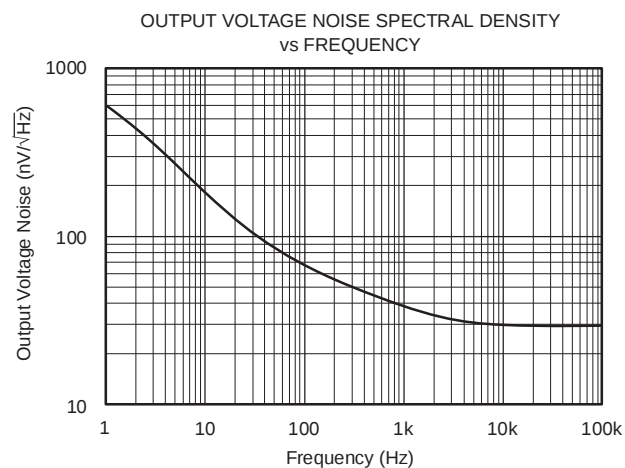
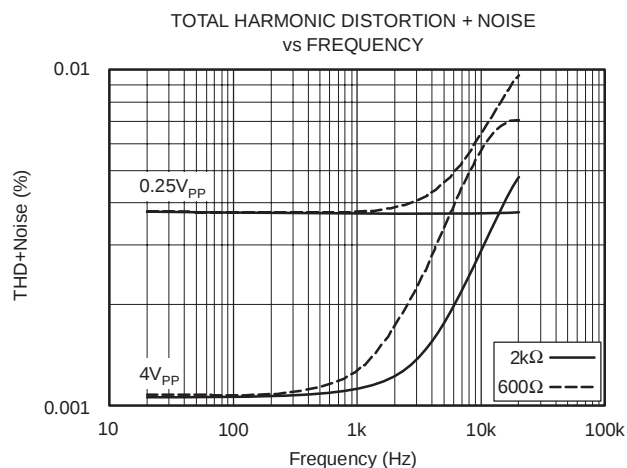
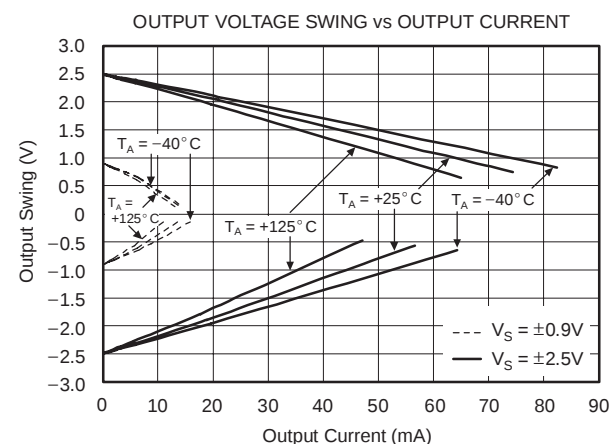
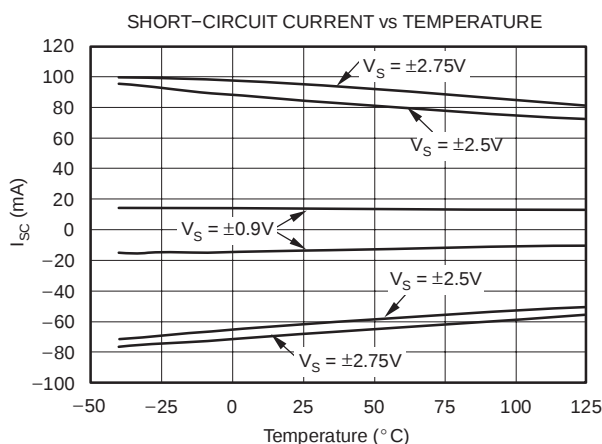
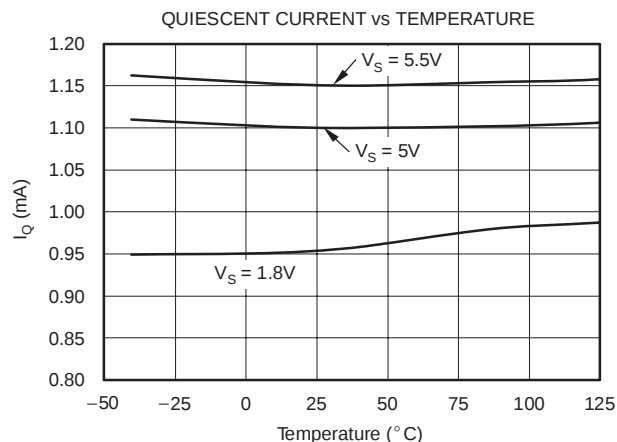
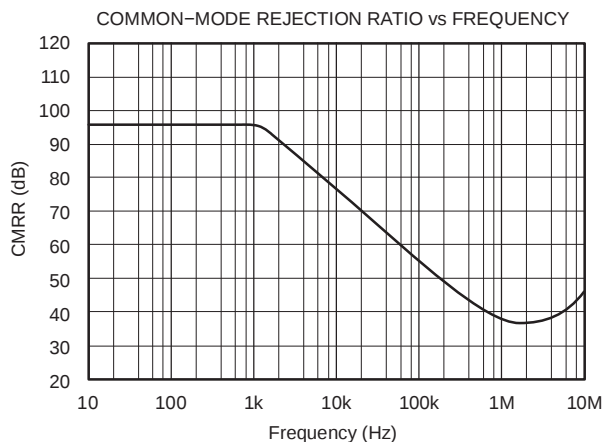
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{REF} = 5\text{V}$, unless otherwise noted.



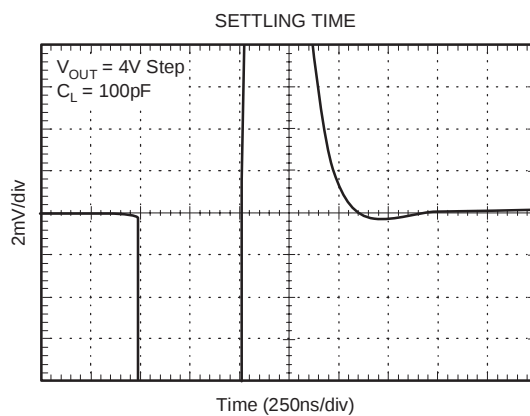
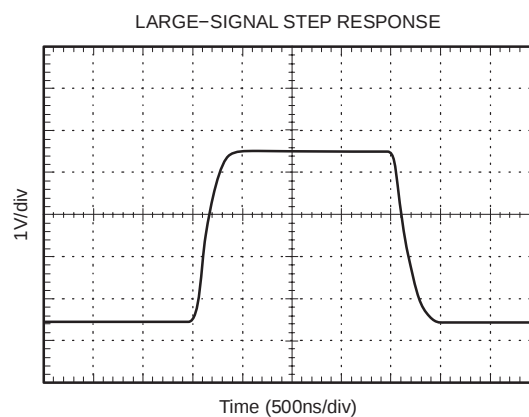
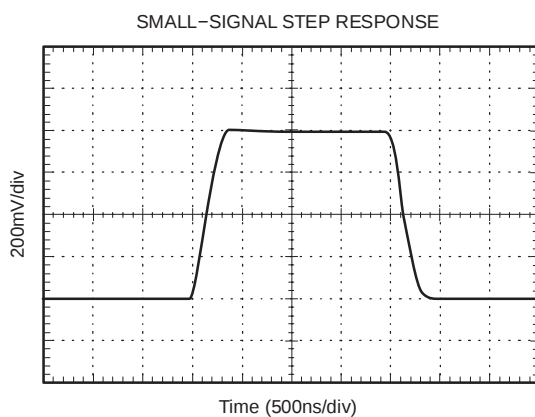
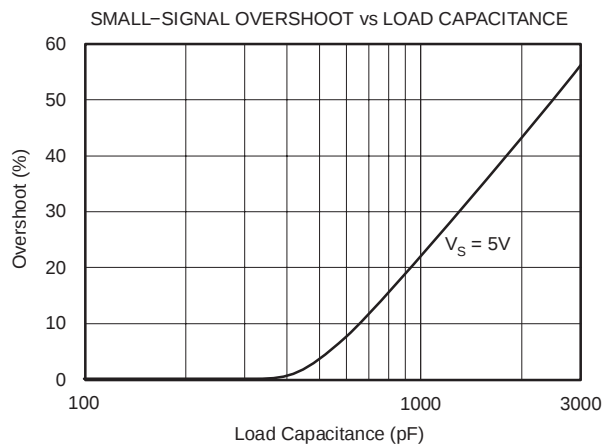
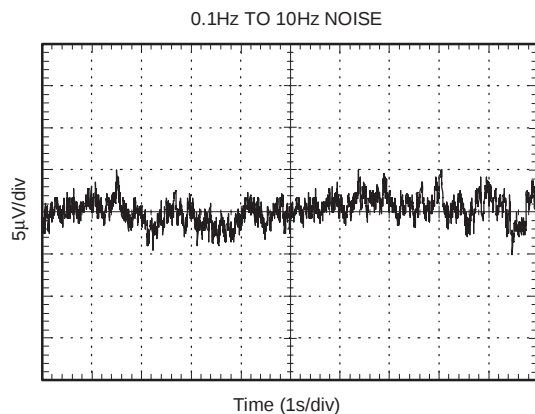
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{\text{REF}} = 5\text{V}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{REF} = 5\text{V}$, unless otherwise noted.



APPLICATION INFORMATION

The internal op amp of the INA159 has a rail-to-rail common-mode voltage capability at its inputs. A rail-to-rail op amp allows the use of $\pm 10\text{V}$ inputs into a circuit biased to 1/2 of a 5V reference (2.5V quiescent output). The inputs to the op amp will swing from approximately 400mV to 3.75V in this application.

The unique input topology of the INA159 eliminates the input offset transition region typical of most rail-to-rail complementary stage operational amplifiers. This allows the INA159 to provide superior glitch- and transition-free performance over the entire common-mode range.

Good layout practice includes the use of a 0.1 μF bypass capacitor placed closely across the supply pins.

COMMON-MODE RANGE

The common-mode range of the INA159 is a function of supply voltage and reference. Where both pins, REF1 and REF2, are connected together:

$$V_{\text{CM}+} = (V+) + 5[(V+) - V_{\text{REF}}] \quad (1)$$

$$V_{\text{CM}-} = (V-) - 5[V_{\text{REF}} - (V-)] \quad (2)$$

Where one REF pin is connected to the reference, and the other pin grounded (1/2 reference connection):

$$V_{\text{CM}+} = (V+) + 5[(V+) - (0.5V_{\text{REF}})] \quad (3)$$

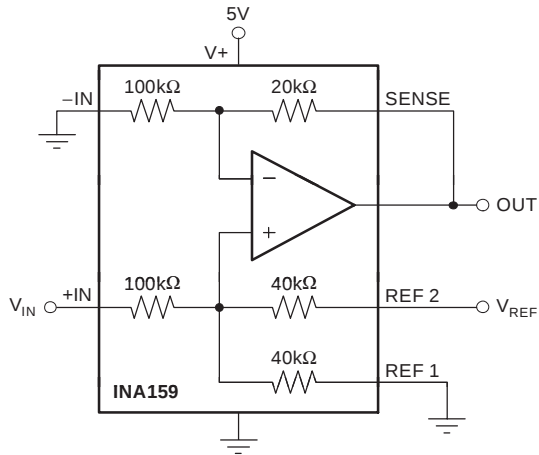
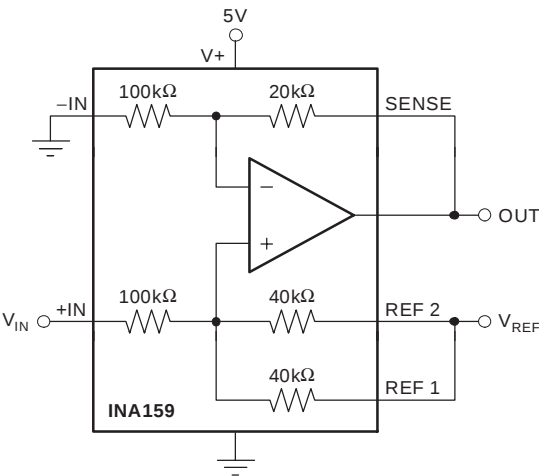
$$V_{\text{CM}-} = (V-) - 5[(0.5V_{\text{REF}}) - (V-)] \quad (4)$$

Some typical values are shown in Table 1.

Table 1. Common-Mode Range For Various Supply and Reference Voltages

REF 1 and REF 2 Connected Together				
V+	V-	V _{REF}	V _{CM+}	V _{CM-}
5	0	3	15	-15
5	0	2.5	17.5	-12.5
5	0	1.25	23.75	-6.25
1/2 Reference Connection				
V+	V-	V _{REF}	V _{CM+}	V _{CM-}
5	0	5	17.5	-12.5
5	0	4.096	19.76	-10.24
5	0	2.5	23.75	-6.25
3.3	0	3.3	11.55	-8.25
3.3	0	2.5	13.55	-6.25
3.3	0	1.25	16.675	-3.125

Table 2. Input and Output Relationships for Various Reference and Connection Combinations

V_{REF} (V)	REF CONNECTION	V_{OUT} for $V_{IN} = 0$ (V)	LINEAR V_{IN} RANGE (V)	USEFUL V_{OUT} SWING (V)
5		2.5	+10 0 -10	4.5 ($\pm 2V$ swing) 0.5
4.096		2.048	+10 0 -10	4.048 ($\pm 2V$ swing) 0.048
3.3		1.65	+10 0 -7.885	3.65 (-1.577V, +2V swing) 0.048
2.5		1.25	+10 (also +5) 0 -6 (also -5)	3.25 (-1.2V, +2V swing) 0.048
1.8		0.9	+10 0 -4.26	2.9 (-0.852V, +2V swing) 0.048
2.5		2.5	+10 0 -10	4.5 ($\pm 2V$ swing) 0.5
1.8		1.8	+10 0 -8.76	3.8 (-1.752V, +2V swing) 0.048
1.2		1.2	+10 0 -5.76	3.2 (-1.15V, +2V swing) 0.048

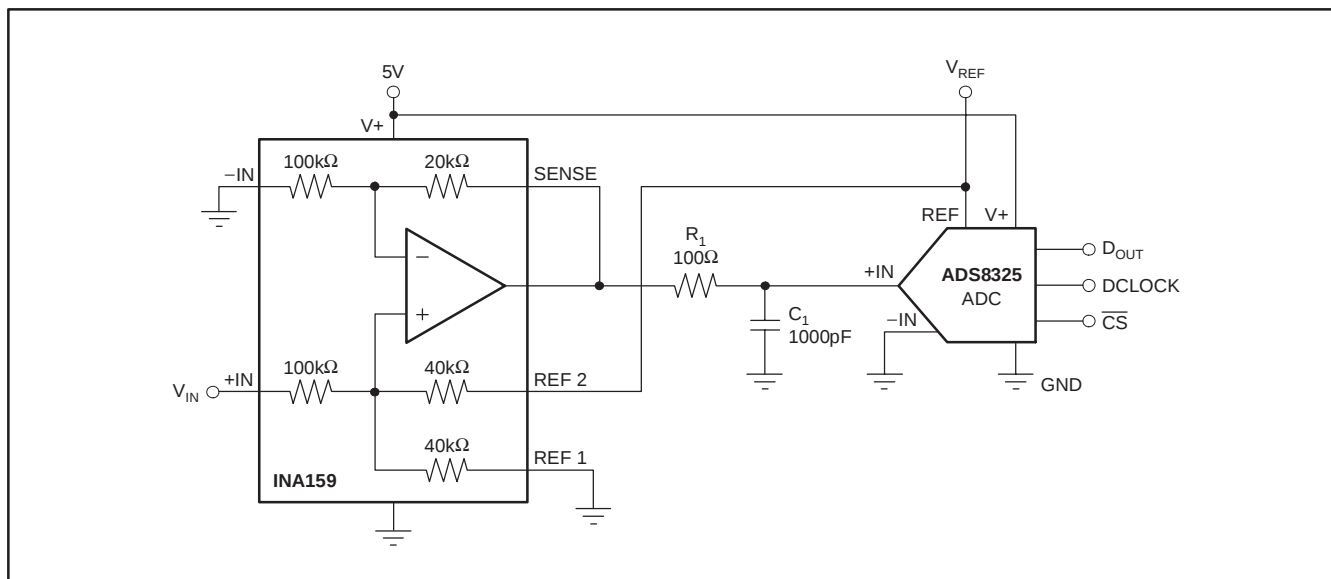


Figure 3. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs

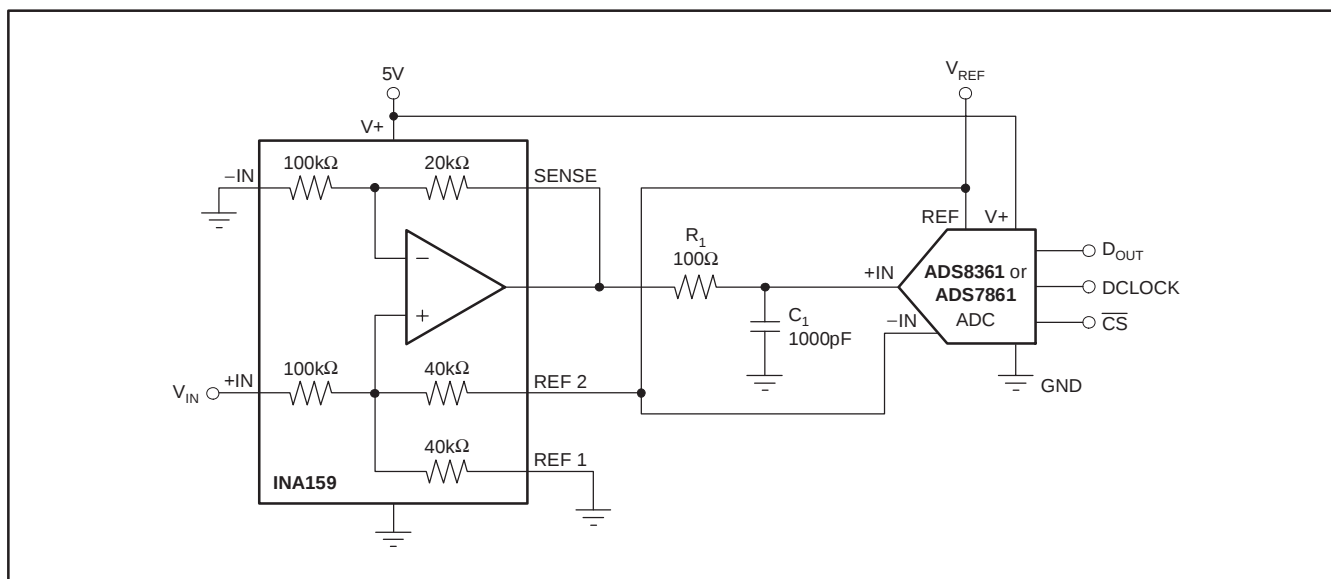
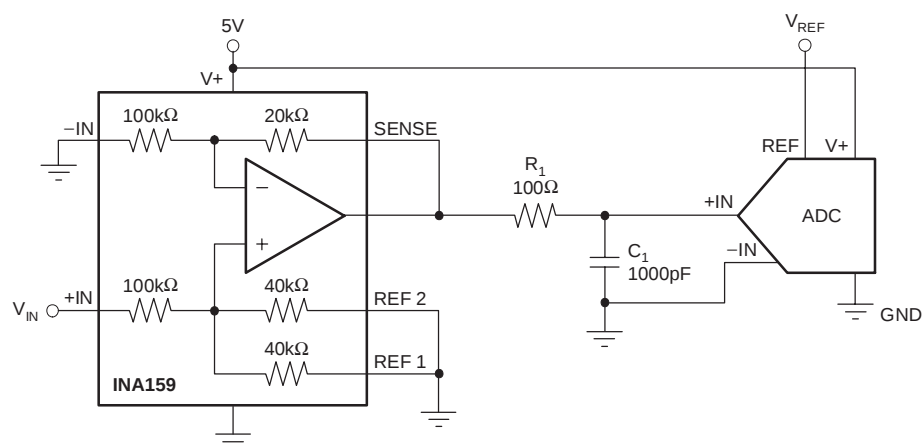
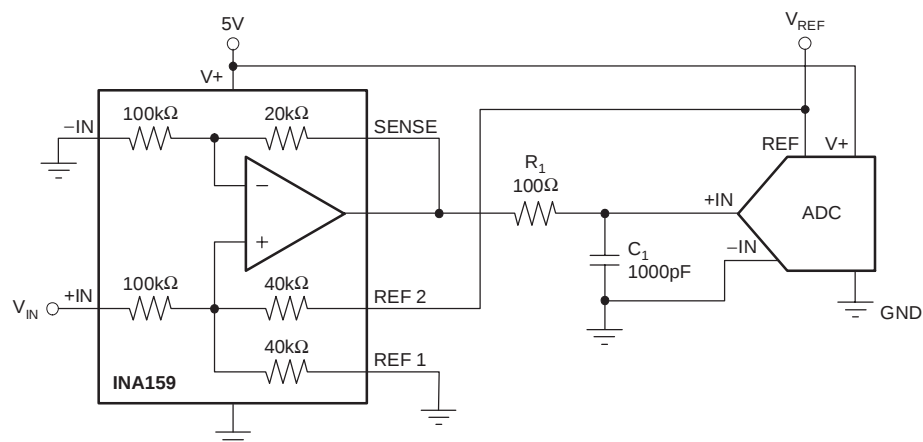


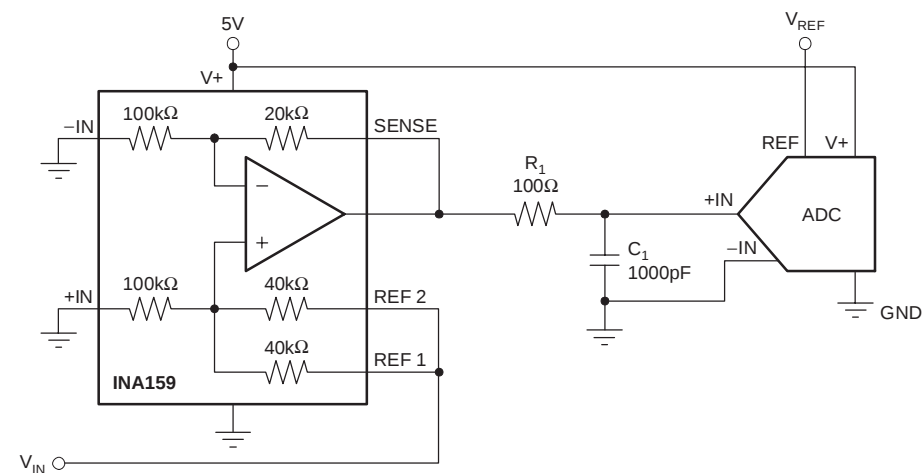
Figure 4. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs with Pseudo-Differential Inputs (such as the ADS7861 and ADS8361)



a) Unipolar, Noninverting, $G = 0.2$



b) Bipolar, Noninverting, $G = 0.2$



c) Unipolar, Unity Gain

Figure 5. Basic INA159 Configurations

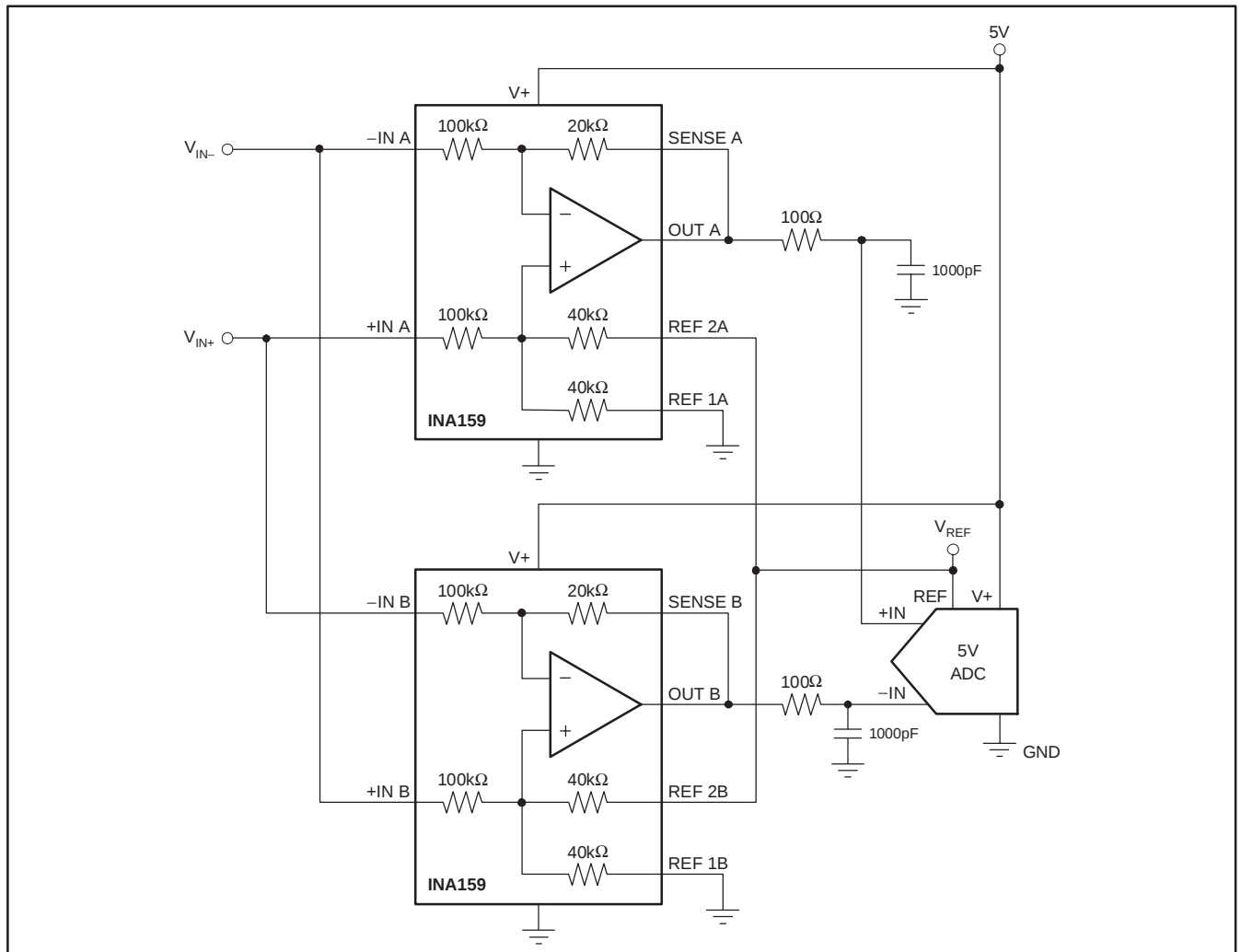


Figure 6. Differential ADC Drive

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
INA159AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA159AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA159AIDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

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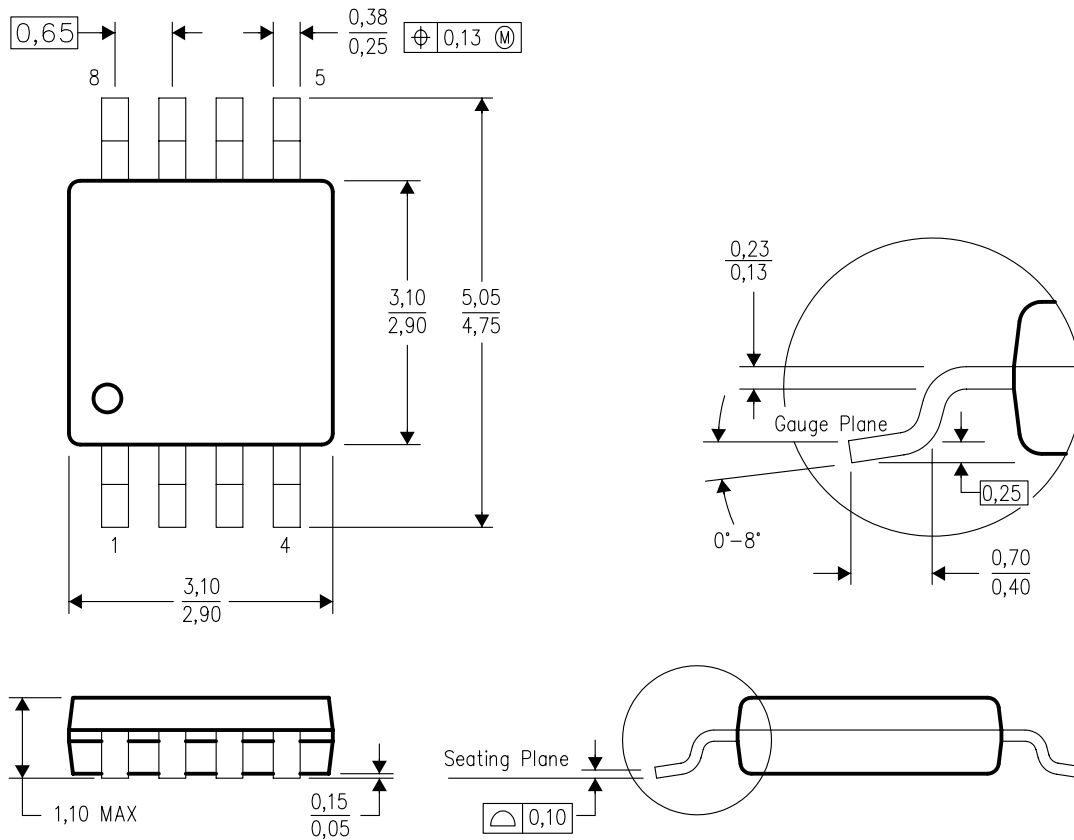
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/D 12/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation AA.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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