

## N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD16409Q3](#)

### FEATURES

- Ultra Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3mm x 3.3mm Plastic Package

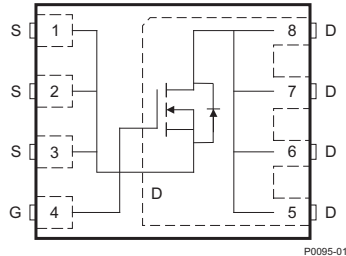
### APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



P0095-01

### PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	25	V
$Q_g$	Gate Charge Total (4.5V)	4	nC
$Q_{gd}$	Gate Charge Gate to Drain	1	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V$	9.5 mΩ
		$V_{GS} = 10V$	6.2 mΩ
$V_{th}$	Threshold Voltage	2	V

### ORDERING INFORMATION

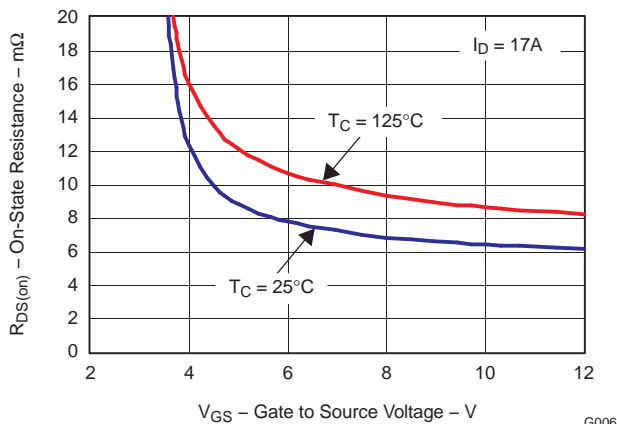
Device	Package	Media	Qty	Ship
CSD16409Q3	SON 3.3 × 3.3 Plastic Package	13-inch reel	2500	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	+16 / -12	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	60	A
	Continuous Drain Current <sup>(1)</sup>	15	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	90	A
$P_D$	Power Dissipation <sup>(1)</sup>	2.6	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 38A, L = 0.1mH, R_G = 25\Omega$	72	mJ

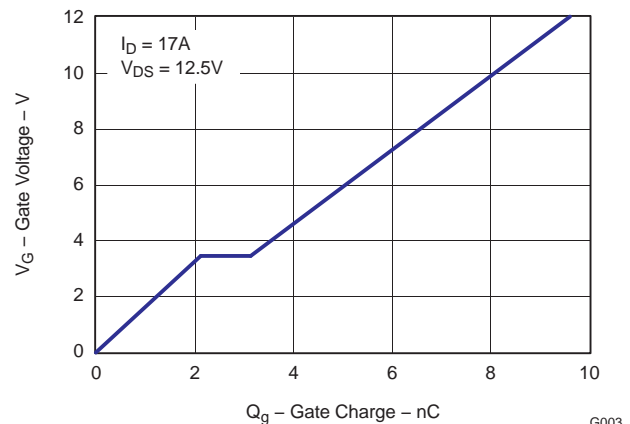
(1)  $R_{\theta JA} = 47^\circ\text{C/W}$  on  $1\text{in}^2$  Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$

 $R_{DS(on)}$  vs  $V_{GS}$ 


G006

Gate Charge



G003



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

(T<sub>A</sub> = 25°C unless otherwise stated)

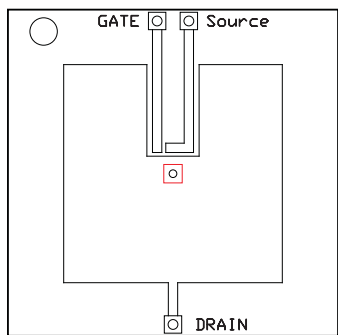
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV <sub>DSS</sub>	Drain to Source Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	25			V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 20V	1			μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = +16/-12V	100			nA
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.7	2	2.3	V
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 17A	9.5		12.4	mΩ
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 17A	6.2		8.2	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 15V, I <sub>D</sub> = 17A	38			S
Dynamic Characteristics						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 12.5V , f = 1MHz	600		800	pF
C <sub>OSS</sub>	Output Capacitance		480		635	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance		40		55	pF
R <sub>g</sub>	Series Gate Resistance	V <sub>DS</sub> = 12.5V, I <sub>D</sub> = 17A	0.9		1.8	Ω
Q <sub>g</sub>	Gate Charge Total (4.5V)		4		5.6	nC
Q <sub>gd</sub>	Gate Charge Gate to Drain		1			nC
Q <sub>gs</sub>	Gate Charge Gate to Source		2.1			nC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>		1.1			nC
Q <sub>OSS</sub>	Output Charge		9.1			nC
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = 12.5V, V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 17A, R <sub>G</sub> = 2Ω	6.5			ns
t <sub>r</sub>	Rise Time		10.6			ns
t <sub>d(off)</sub>	Turn Off Delay Time		6.3			ns
t <sub>f</sub>	Fall Time		3.4			ns
Diode Characteristics						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> = 17A, V <sub>GS</sub> = 0V	0.85		1	V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DD</sub> = 12.9V, I <sub>F</sub> = 17A, di/dt = 300A/μs	13.8			nC
t <sub>rr</sub>	Reverse Recovery Time	V <sub>DD</sub> = 12.9V, I <sub>F</sub> = 17A, di/dt = 300A/μs	17.5			ns

## THERMAL CHARACTERISTICS

(T<sub>A</sub> = 25°C unless otherwise stated)

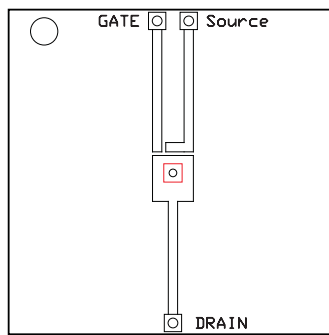
PARAMETER		MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Thermal Resistance Junction to Case <sup>(1)</sup>			3.5	°C/W
R <sub>θJA</sub>	Thermal Resistance Junction to Ambient <sup>(1) (2)</sup>			59	°C/W

- (1) R<sub>θJC</sub> is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 × 1.5 in 0.06 inch thick FR4 board. R<sub>θJC</sub> is specified by design while R<sub>θJA</sub> is determined by the user's board design.
- (2) Device mounted on FR4 Material with 1 inch<sup>2</sup> of 2 oz. Cu.



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Max  $R_{\theta JA} = 59^{\circ}\text{C/W}$   
when mounted on 1  
 $\text{inch}^2$  of 2 oz. Cu.

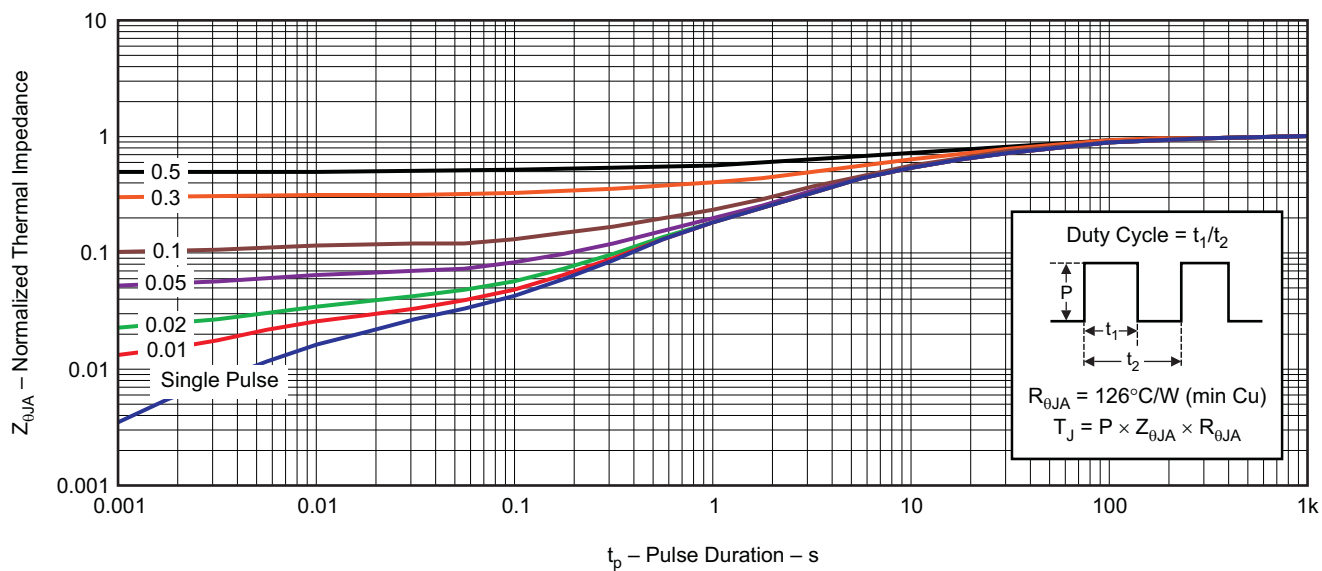


M0161-02

Max  $R_{\theta JA} = 157^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of 2  
oz. Cu.

## TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

## TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

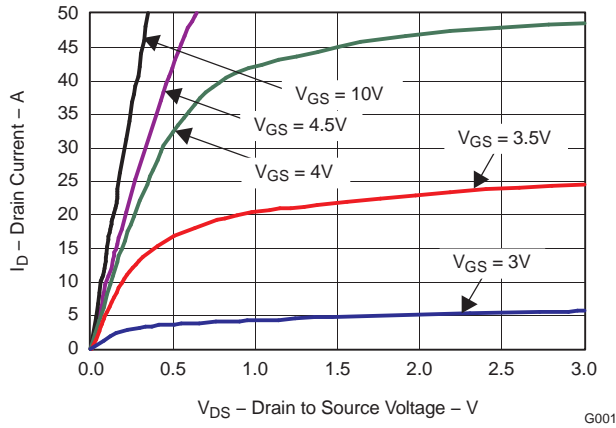


Figure 2. Saturation Characteristics

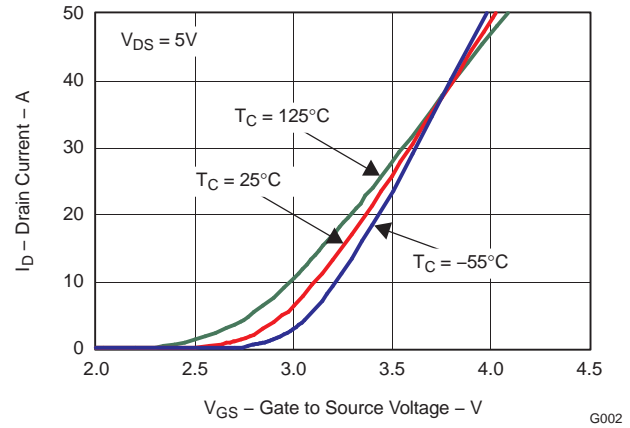


Figure 3. Transfer Characteristics

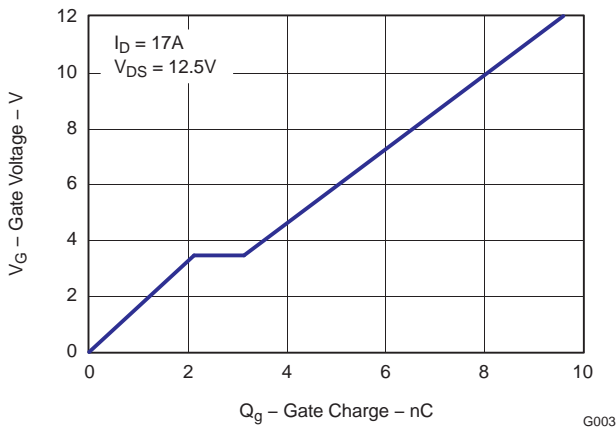


Figure 4. Gate Charge

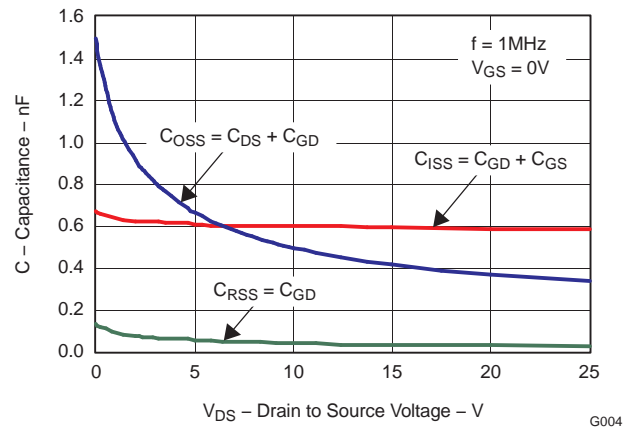


Figure 5. Capacitance

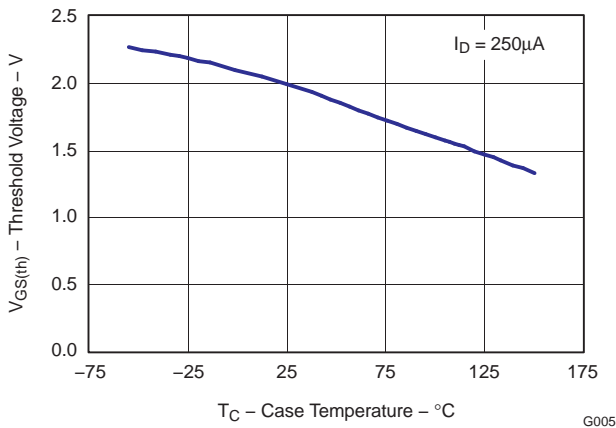


Figure 6. Threshold Voltage vs. Temperature

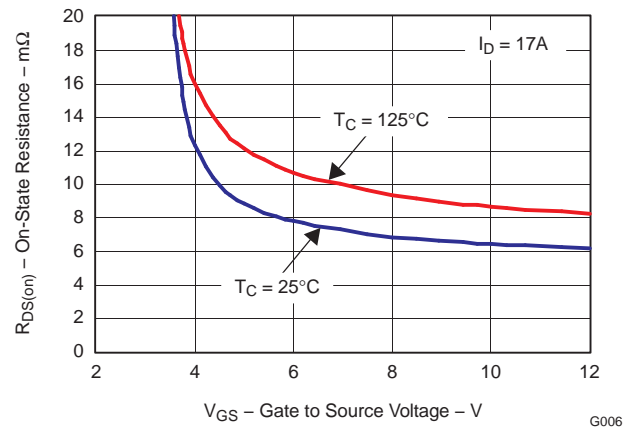
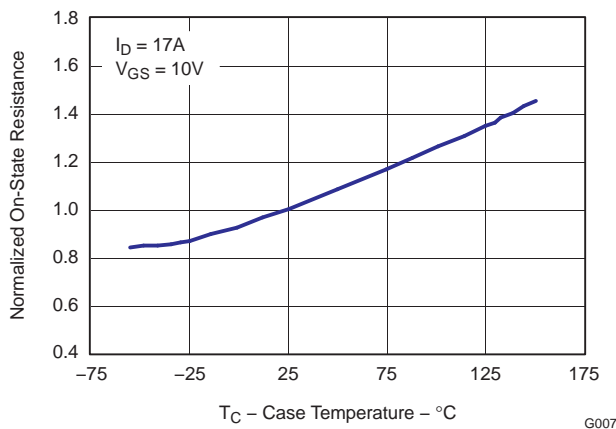


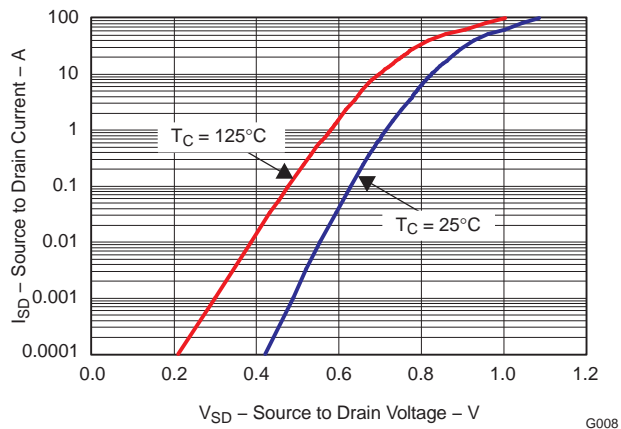
Figure 7. On Resistance vs. Gate Voltage

## TYPICAL MOSFET CHARACTERISTICS (continued)

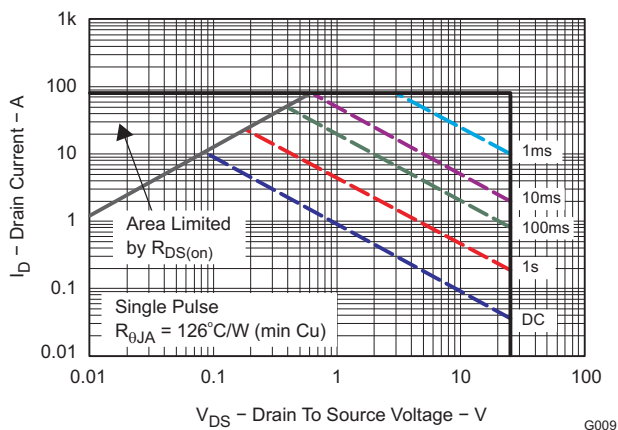
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



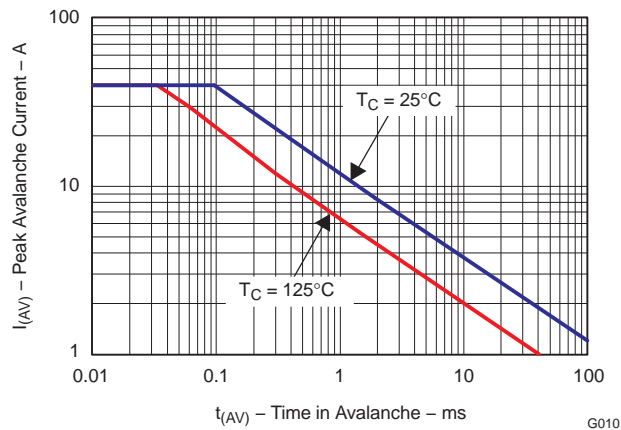
**Figure 8. Normalized On Resistance vs. Temperature**



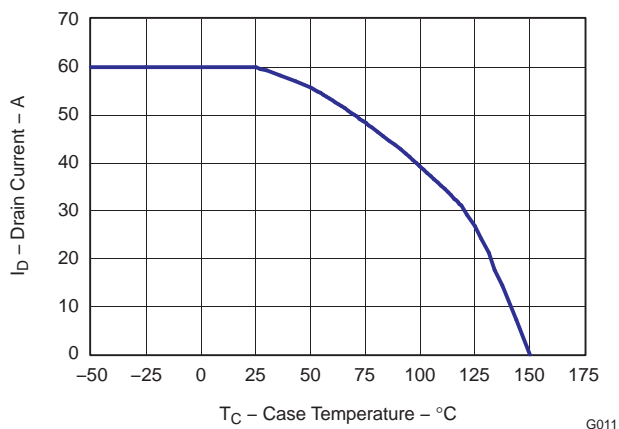
**Figure 9. Typical Diode Forward Voltage**



**Figure 10. Maximum Safe Operating Area**



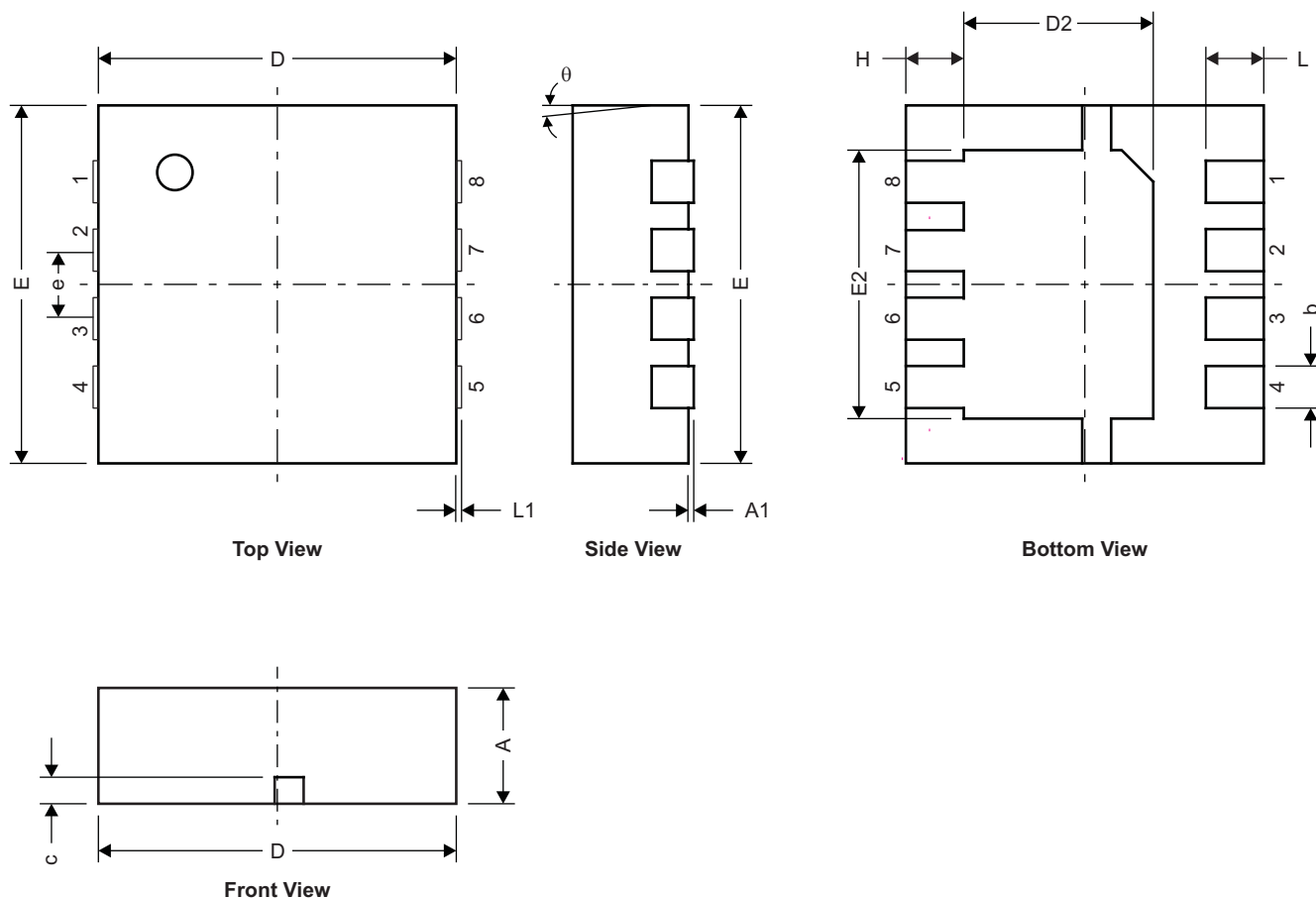
**Figure 11. Single Pulse Unclamped Inductive Switching**



**Figure 12. Maximum Drain Current vs. Temperature**

## MECHANICAL DATA

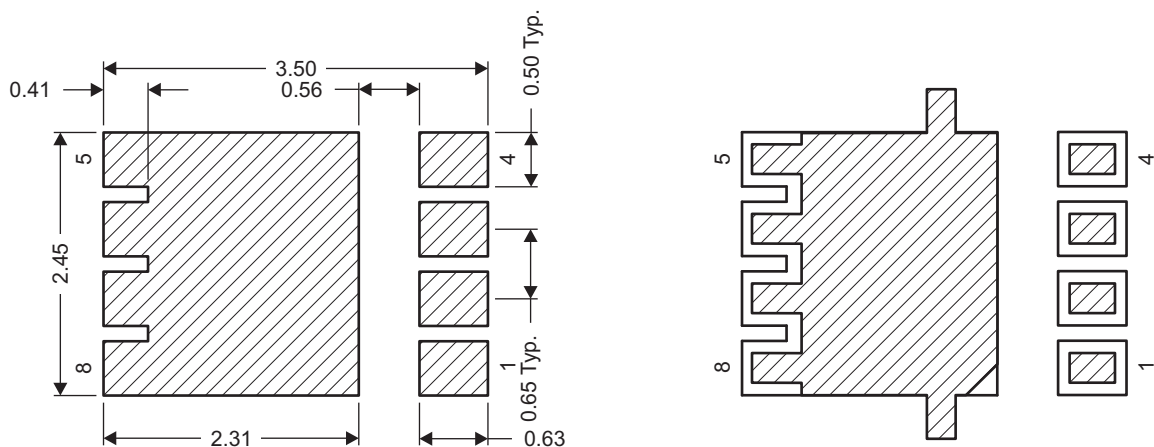
### Q3 Package Dimensions



M0142-01

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D1	–	–	–	–	–	–
D2	1.650	1.750	1.800	0.065	0.069	0.071
E	3.200	3.300	3.400	0.126	0.130	0.134
E1	–	–	–	–	–	–
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	–	–	–	–	–	–
$\theta$	–	–	–	–	–	–

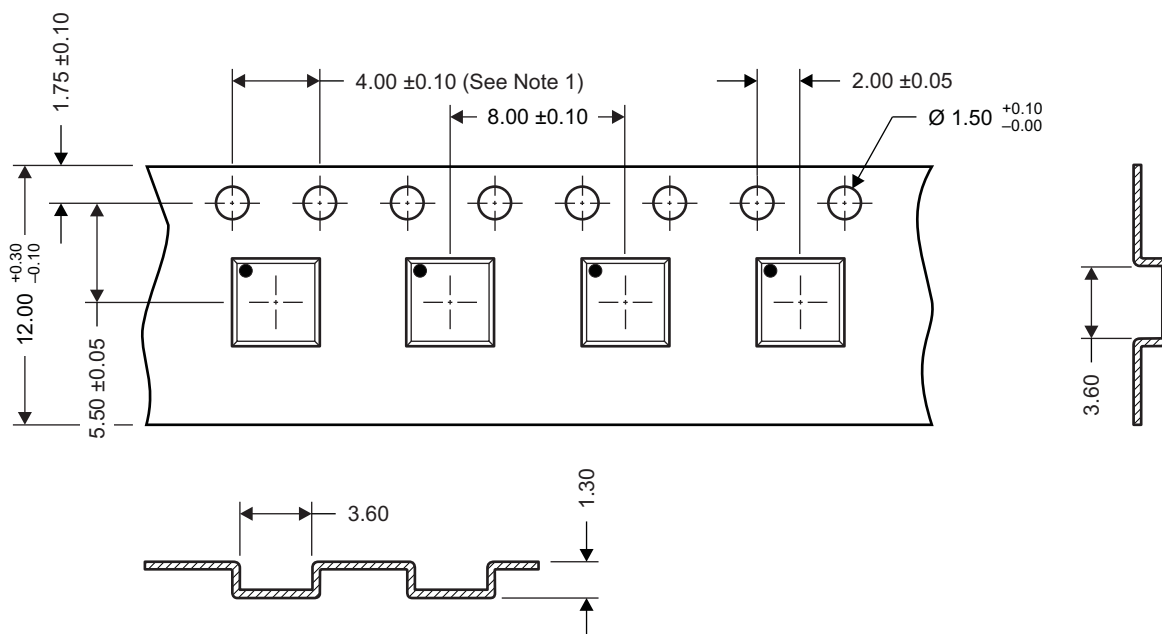
## Recommended PCB Land Pattern



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For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

## Q3 Tape and Reel Information



M0144-01

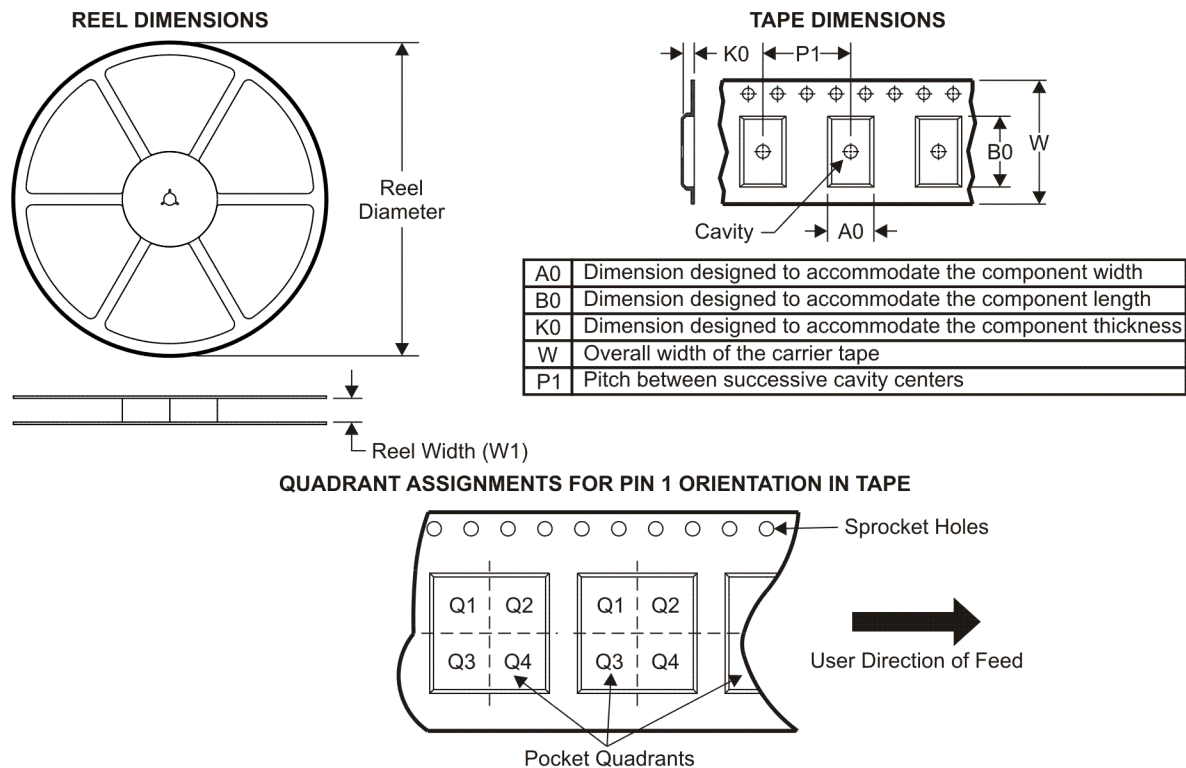
### Notes:

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness:  $0.30 \pm 0.05$  mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

**REVISION HISTORY**

<b>Changes from Original (August 2009) to Revision A</b>	<b>Page</b>
<ul style="list-style-type: none"><li>Deleted the Package Marking Information section .....</li></ul>	<a href="#">7</a>



**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16409Q3	SON	DQG	8	2500	330.0	12.8	3.6	3.6	1.2	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16409Q3	SON	DQG	8	2500	335.0	335.0	32.0

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### Applications

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