Ten-Output Low-Jitter Low-Power Clock Buffer

Check for Samples: CDCLVC1310

FEATURES

- **High-Performance Crystal Buffer With Ultralow Noise Floor of –169 dBc/Hz**
- **Additive Phase Noise/Jitter Performance Is 25 fs_{RMS} (Typ.)**
- **Operates with 3.3-V/2.5-V Core and 3.3-V/2.5-V/1.8-V/1.5-V Output Supply**
- **Device inputs consist of primary, secondary and crystal inputs and can be selected manually (through pins) using the input MUX. The primary and secondary inputs can accept LVPECL, LVDS, HCSL, SSTL or LVCMOS signals and crystal input.**
  - **Crystal Frequencies Supported Are From 8 MHz to 50 MHz**
  - **Differential and Single-Ended Input Frequencies Supported Are up to 200 MHz**
- **10 Single-Ended LVCMOS Outputs. The outputs can operate at 1.5-V, 1.8-V, 2.5-V or 3.3-V Power-Supply Voltage.**
  - **LVCMOS Outputs Operate up to 200 MHz**
  - **Output Skew Is 30 ps (typ)**
  - **Total Propagation Delay Is 2 ns (typ)**
  - **Synchronous and Glitch-Free Output Enable Is Available**
- **Offered in QFN-32 5-mm × 5-mm Package With Industrial Temperature Range of –40°C to 85°C**
- **Crystal Input Can Be Overdriven With LVCMOS Signal up to 50 MHz**

APPLICATIONS

- **Wireless and Wired Infrastructure**
- **Networking and Data Communications**
- **Medical Imaging**
- **Portable Test and Measurement**
- **High-End A/V**

DESCRIPTION

The CDCLVC1310 is a highly versatile, low-jitter, low-power clock fanout buffer which can distribute to ten low-jitter LVCMOS clock outputs from one of three inputs, whose primary and secondary inputs can feature differential or single-ended signals and crystal input. Such a buffer is intended for use in a variety of mobile and wired infrastructure, data communication, computing, low-power medical imaging, and portable test and measurement applications. When the input is an illegal level, the output is at a defined state. The core can be set to 2.5 V or 3.3 V, and output can be set to 1.5 V, 1.8 V, 2.5 V or 3.3 V. The CDCLVC1310 can be easily configured through pin programming. The overall additive jitter performance is 25 fs_{RMS} (typ). The CDCLVC1310 is packaged in a small 32-pin 5-mm × 5-mm QFN package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM

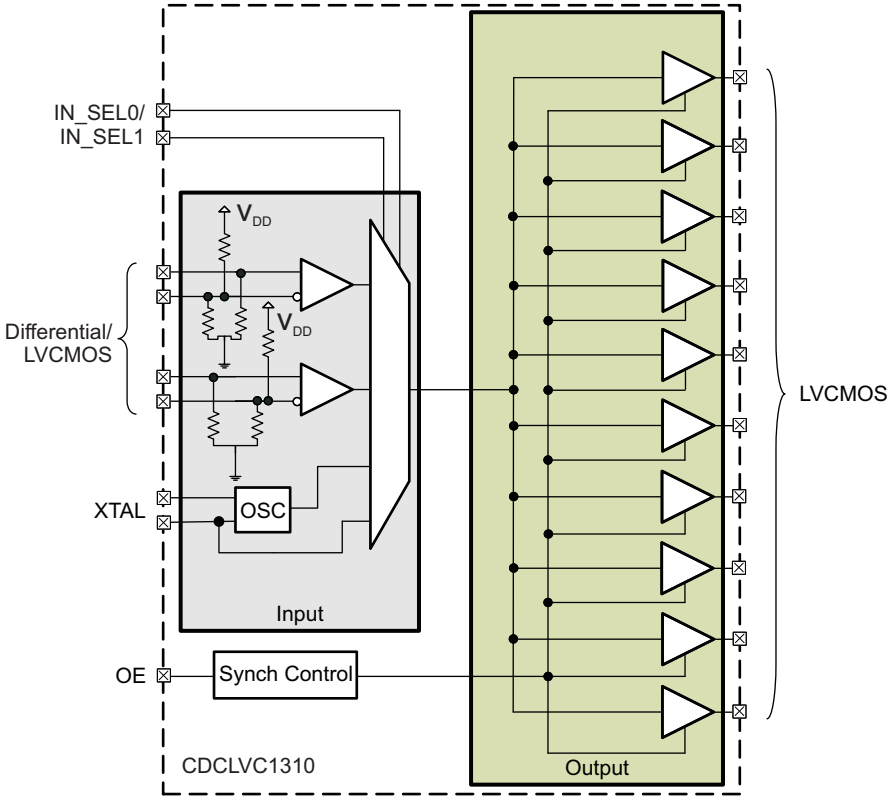
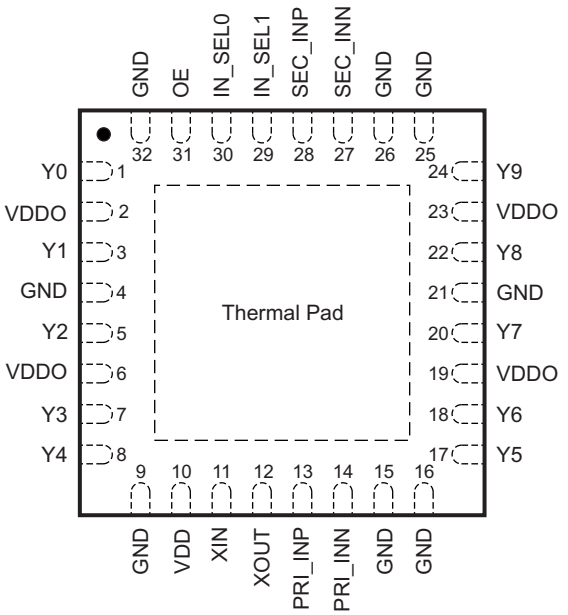


Figure 1. High-Level Block Diagram of CDCLVC1310

PINOUT DIAGRAM

CDCLVC1310
RHB Package
(Top View)



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PIN FUNCTIONS

PIN		I/O	TYPE	DESCRIPTION
NAME	NO(s)			
GND	4, 9, 15, 16, 21, 25, 26, 32	PWR	Analog	Power supply ground
IN_SEL0, IN_SEL1	30, 29	I	Digital	Input clock selection (pulldown of 150 kΩ)
OE	31	I	Digital	LVCMOS output enable (pulldown of 150 kΩ)
PRI_INN	14	I	Analog	Inverting differential primary reference input, internally biased to Vdd/2 (pullup/pulldown of 150 kΩ)
PRI_INP	13	I	Analog	Non-inverting differential/single-ended primary reference input (pulldown of 150 kΩ)
SEC_INN	27	I	Analog	Inverting differential secondary reference input, internally biased to Vdd/2 (pullup/pulldown of 150 kΩ)
SEC_INP	28	I	Analog	Non-inverting differential/single-ended secondary reference input (pulldown of 150 kΩ)
VDD	10	PWR	Analog	Power supply pins
VDDO	2, 6, 19, 23	PWR	Analog	I/O power supply pins
XIN	11	I	Analog	Crystal Oscillator Input or XTAL Bypass mode
XOUT	12	I	Analog	Crystal Oscillator Output
Y0	1	O	Analog	LVCMOS output 0
Y1	3	O	Analog	LVCMOS output 1
Y2	5	O	Analog	LVCMOS output 2
Y3	7	O	Analog	LVCMOS output 3
Y4	8	O	Analog	LVCMOS output 4
Y5	17	O	Analog	LVCMOS output 5
Y6	18	O	Analog	LVCMOS output 6
Y7	20	O	Analog	LVCMOS output 7
Y8	22	O	Analog	LVCMOS output 8
Y9	24	O	Analog	LVCMOS output 9

Table 1. Input Selection

IN_SEL1	IN_SEL0	INPUT CHOSEN
0	0	PRI_IN
0	1	SEC_IN
1	0	XTAL/overdrive (1)
1	1	XTAL bypass (2)

(1) This mode can be used to overdrive the XTAL oscillator with an LVCMOS input. For characteristics; see LVCMOS OUTPUT CHARACTERISTICS.

(2) This mode is only XTAL bypass. For characteristics, see LVCMOS OUTPUT CHARACTERISTICS.

Table 2. INPUT/OUTPUT OPERATION (1)

INPUT STATE	OUTPUT STATE
PRI_INx, SEC_INx open	Logic LOW
PRI_INP/SEC_INP = HIGH, PRI_INN/SEC_INN = LOW	Logic HIGH
PRI_INP/SEC_INP = LOW, PRI_INN/SEC_INN = HIGH	Logic LOW

(1) Device must have switching edge to obtain output states.

Table 3. OE Function

OE	Yx
0	High-impedance
1	Enabled

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
VDD, VDDO	Supply voltage range	–0.5 to 4.6	V
V_{IN}	Input voltage range	–0.5 to VDD + 0.5	V
V_{OUT}	Output voltage range	–0.5 to VDDO + 0.5	V
I_{IN}	Input current	±20	V
I_{OUT}	Output current	±50	V
T_{stg}	Storage temperature range	–65 to 150	°C
T_J	Junction temperature	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDO	Output supply voltage	3.135	3.3	3.465	V
		2.375	2.5	2.625	
		1.6	1.8	2	
		1.35	1.5	1.65	
VDD	Core supply voltage	3.135	3.3	3.465	V
		2.375	2.5	2.625	
I_{OH}	High-level output current, LVCMOS			–24	mA
I_{OL}	Low-level output current, LVCMOS			24	mA
T_A	Ambient temperature	–40		85	°C

THERMAL INFORMATION

THERMAL METRIC(1)		CDCLVC1310 RHB 32 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	41.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	34.1	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	14.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	14.4	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	6.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

INPUT CHARACTERISTICS

over recommended ranges of supply voltage (VDDO ≤ VDD), load and ambient temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Characteristic (OE, IN_SEL0, IN_SEL1, PRI_IN, SEC_IN)						
I_{IH}	Input high current	VDD = 3.465 V, V_{IH} = 3.465 V			40	µA
I_{IL}	Input low current	VDD = 3.465 V, V_{IL}=0V			–40	µA
ΔV/ΔT	Input edge rate	20%–80%		2		V/ns
$R_{Pullup/down}$	Pullup/down resistance			150		kΩ
C_{IN}	Input capacitance			2		pF
Single-Ended DC Characteristic (PRI_INP, SEC_INP)(1)						
V_{IH}	Input high voltage	VDD = 3.3 V ±5%	2		VDD + 0.3	V
		VDD = 2.5 V ±5%	1.6		VDD + 0.3	
V_{IL}	Input low voltage	VDD = 3.3 V ±5%	–0.3		1.3	V
		VDD = 2.5 V ±5%	–0.3		0.9	
Single-Ended DC Characteristic (OE, IN_SEL0, IN_SEL1)						
V_{IH}	Input high voltage		0.7 × VDD			V
V_{IL}	Input low voltage				0.3 × VDD	V
Differential DC Characteristic (PRI_IN, SEC_IN)						
$V_{I,DIFF}$	Differential input voltage swing(2)		0.15		1.3	V
V_{ICM}	Input common-mode voltage(3)		0.5		VDD – 0.85	V
AC Characteristic (PRI_IN, SEC_IN)						
f_{IN}	Input frequency		DC		200	MHz
idc	Input duty cycle		40%		60%	

(1) PRI/SEC_INN biased to VDD/2
(2) V_{IL} should not be less than –0.3 V
(3) Input common-mode voltage is defined as V_{IH} (see Figure 19).

CRYSTAL CHARACTERISTICS

over recommended ranges of supply voltage, load and ambient temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Equivalent series resistance (ESR)			50		Ω
Maximum shunt capacitance			7		pF
Drive level			100		µW

CRYSTAL OSCILLATOR CHARACTERISTICS

over recommended ranges of supply voltage, load and ambient temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Mode of oscillation			Fundamental		
Frequency		8		50	MHz
Frequency in overdrive mode(1)				50	MHz
Frequency in bypass mode(2)				50	MHz
On-chip load capacitance			12		pF

(1) Input signal swing (max) = 2 V; input signal t_r/t_f(max) = 10 ns; functional, but ac parameters may not be met.
(2) Input signal swing (max) = V_{DD}; input signal t_r/t_f(max) = 10 ns; functional, but ac parameters may not be met.

LVCMOS OUTPUT CHARACTERISTICS

over recommended ranges of supply voltage (VDDO ≤ VDD), load (50 Ω to VDDO/2), and ambient temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}					200	MHz
V_{OH}	Output high voltage	VDDO = 3.135 V	2.5			V
		VDDO = 2.375 V	1.8			
		VDDO = 1.6 V	1.15			
		VDDO = 1.35 V	0.95			
V_{OL}	Output low voltage	VDDO = 3.135 V			0.5	V
		VDDO = 2.375 V			0.4	
		VDDO = 1.6 V			0.4	
		VDDO = 1.35 V			0.4	
R_{OUT}	Output impedance	VDDO = 3.3 V		15		Ω
		VDDO = 2.5 V		20		
		VDDO = 1.8 V		25		
		VDDO = 1.5 V		30		
$t_{SLEW-RATE}$	Output rise/fall slew rate	20% to 80%		5		V/ns
t_{SK}	Output skew			30	50	ps
$t_{SK,PP}$	Part-to-part skew(1)				2	ns
t_{DELAY}	Propagation delay			2		ns
t_{RJIT}	System-level additive jitter(2)	Single-ended input, VDD = 3.3 V, VDDO = 3.3 V		25		f_S, RMS
		Single-ended input, VDD = 2.5 V/3.3 V, VDDO = 1.5 V/1.8 V/2.5 V, $f_{IN/OUT}$ = 125 MHz		30		
		Differential input, VDD = 3.3 V, VDDO = 3.3 V		30		
		Differential input, VDD = 2.5V/3.3V, VDDO = 1.5V/1.8V/2.5V, $f_{IN/OUT}$ = 125 MHz		30		
NF	Noise floor	10-kHz offset(3)		–145		dBc/Hz
		100-kHz offset(3)		–156		
		1-MHz offset(3)		–163		
		10-MHz offset(3)		–164		
		20-MHz offset(3)		–164		
		10-kHz offset(4)		–145		
		100-kHz offset(4)		–155		
		1-MHz offset(4)		–160		
		10-MHz offset(4)		–161		
		20-MHz offset(4)		–162		
odc	Output duty cycle	$f_{IN/OUT}$ = 125 MHz, idc = 50%(5)	45%		55%	
t_{EN}	Output enable/disable time				2	Cycle
$MUX_{ISOLATION}$	MUX isolation(6)	125 MHz	55			dB

(1) Part-to-part skew is calculated as the difference between the fastest and the slowest t_{pd} across multiple devices.
(2) Integration range: 12 kHz–20 MHz; input source see Application Information
(3) Single-ended input, $f_{IN/OUT}$ = 125 MHz, VDD = VDDO = 3.3 V
(4) Differential input, $f_{IN/OUT}$ = 125 MHz, VDD = VDDO = 3.3 V
(5) Stable V_{IH}, V_{IL}, and V_{CM}
(6) See Figure 18.

PHASE NOISE WITH XTAL[1] SELECTED

VDD = VDDO = 2.5 V/3.3V, f_{XTAL} = 25 MHz, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Jrms	RMS phase jitter	IB = 12 kHz to 5 MHz, VDD = VDDO = 3.3 V		80		ps rms
		IB = 12 kHz to 5 MHz, VDD = VDDO = 2.5 V		115		
PN	Phase noise (see Figure 15)	f_{offset} = 100 Hz, VDD = VDDO = 3.3 V		–92		dBc/Hz
		f_{offset} = 1 kHz, VDD = VDDO = 3.3 V		–137		
		f_{offset} = 10 kHz, VDD = VDDO = 3.3 V		–163		
		f_{offset} = 100 kHz, VDD = VDDO = 3.3 V		–168		
		f_{offset} = 1 MHz, VDD = VDDO = 3.3 V		–168		
		f_{offset} = 5 MHz, VDD = VDDO = 3.3 V		–169		
		f_{offset} = 100 Hz, VDD = VDDO = 2.5 V		–91		
		f_{offset} = 1 kHz, VDD = VDDO = 2.5 V		–136		
		f_{offset} = 10 kHz, VDD = VDDO = 2.5 V		–159		
		f_{offset} = 100 kHz, VDD = VDDO = 2.5 V		–164		
		f_{offset} = 1 MHz, VDD = VDDO = 2.5 V		–165		
		f_{offset} = 5 MHz, VDD = VDDO = 2.5 V		–165		

(1) Crystal specification: C_L = 18 pF; ESR = 35 Ω (max); C_0 = 7 pF; drive level = 100 µW (max)

DEVICE CURRENT CONSUMPTION

over recommended ranges of supply voltage, load and ambient temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL PARAMETERS FOR ALL VERSIONS						
I_{DD}	Static device current[1]	OE = 0 V or V_{DD}; Ref. input (PRI/SEC) = 0 V or V_{DD}; I_O = 0 mA; V_{DD}/V_{DDO} = 3.3 V		14		mA
		OE = 0 V or V_{DD}; Ref. input (PRI/SEC) = 0 V or V_{DD}; I_O = 0 mA; V_{DD}/V_{DDO} = 2.5 V		8		
$I_{DD,XTAL}$	Device current with XTAL input[1]			20		mA
C_{PD}	Power dissipation capacitance per output[2]	VDDO = 3.465 V; f = 100 MHz			8.8	pF
		VDDO = 2.625 V; f = 100 MHz			7.7	
		VDDO = 2 V; f = 100 MHz			7.3	
		VDDO = 1.65 V; f = 100 MHz			6.9	

(1) I_{DD} and $I_{DD,XTAL}$ is the current through V_{DD}; outputs on or in the high-impedance state; no load.
(2) This is the formula for the power dissipation calculation (see Power Consideration section)
$I_{DD,Total} = I_{DD} + I_{DD,Cload} + I_{DD,dyn}$ [mA]
$I_{DD,dyn} = C_{PD} \times V_{DDO} \times f \times n$ [mA]
$I_{DD,Cload} = C_{load} \times V_{DDO} \times f \times n$ [mA]
n = Number of switching output pins

TEST CONFIGURATIONS

Figure 2 through Figure 8 illustrate how the device should be set up for a variety of test configurations.

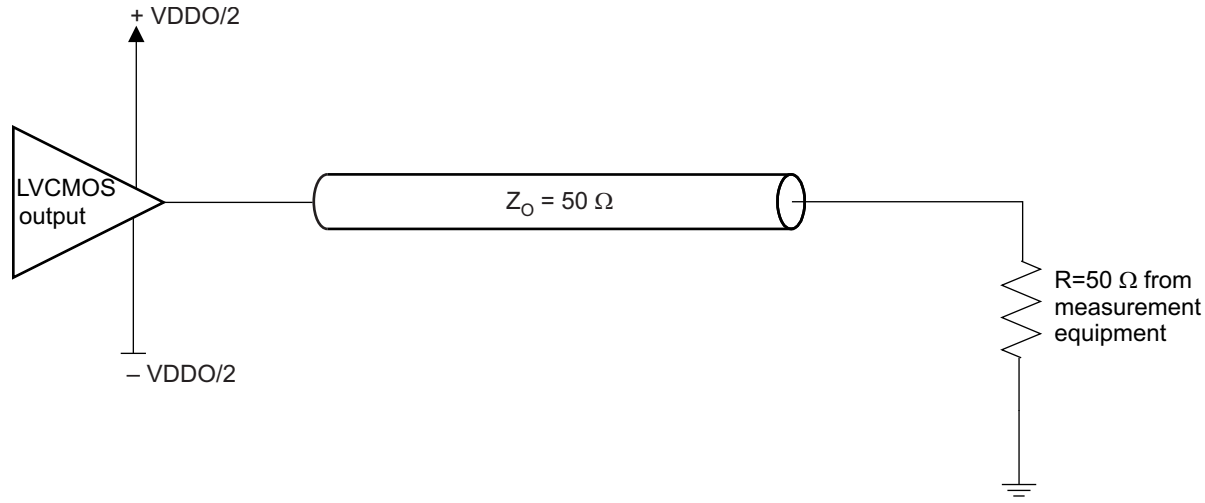


Figure 2. LVCMOS Output DC Configuration; Test Load Circuit

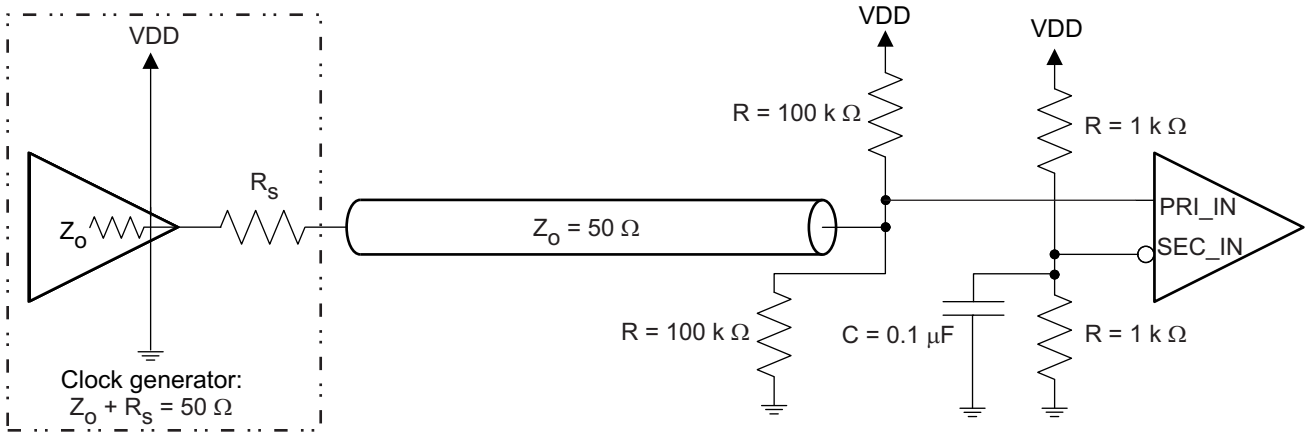


Figure 3. LVCMOS Input DC Configuration During Device Test

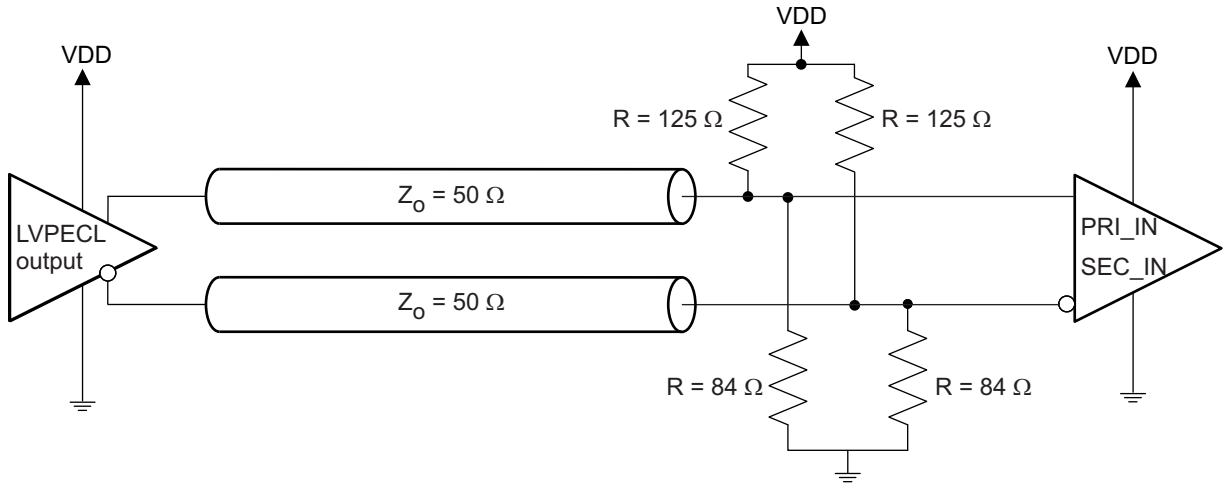


Figure 4. LVPECL Input Configuration During Device Test

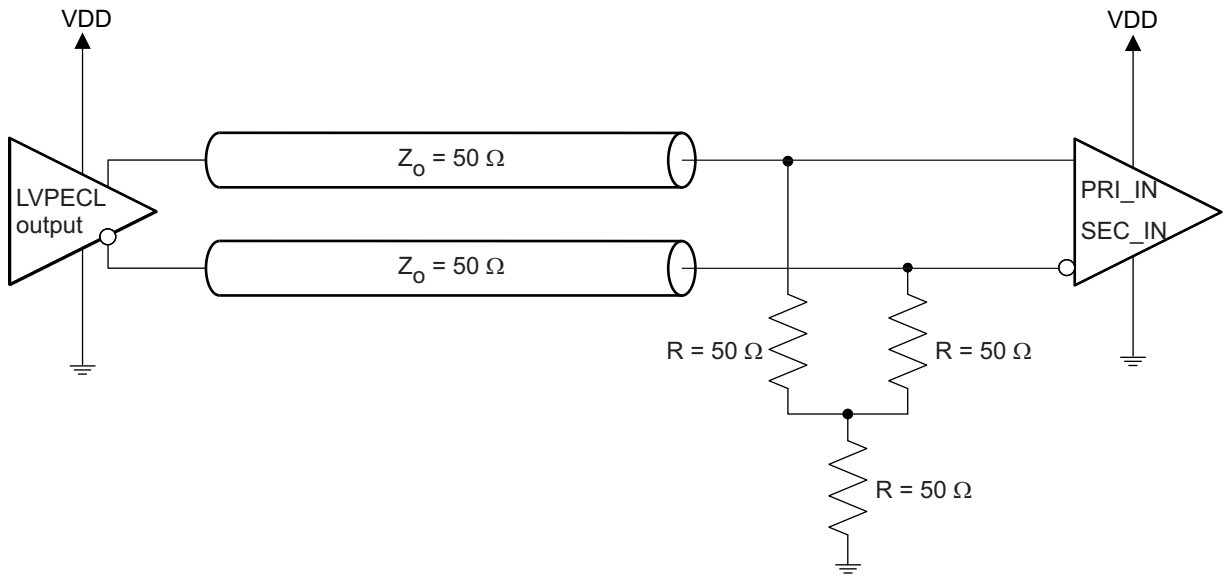


Figure 5. LVPECL Input Configuration During Device Test

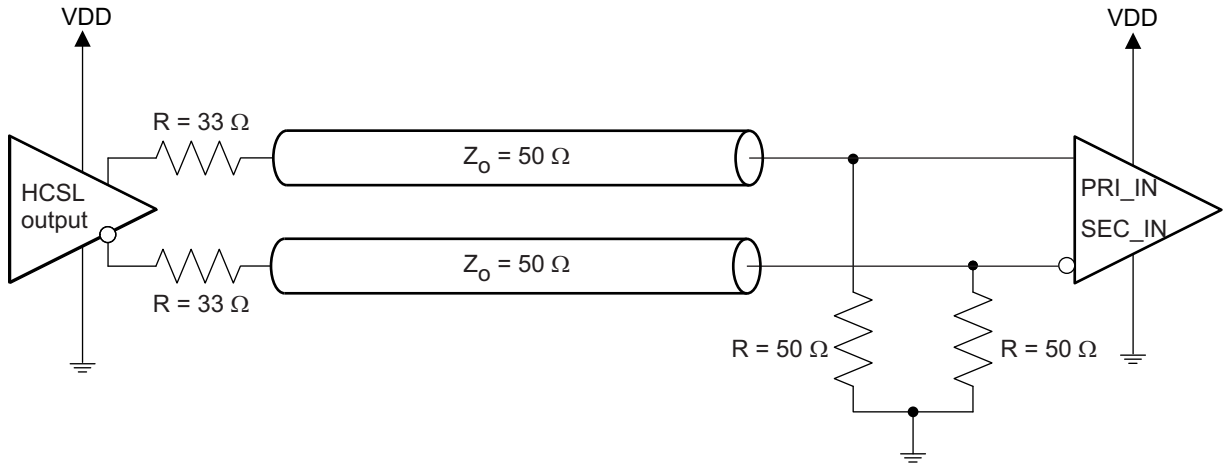


Figure 6. HCSL Input Configuration During Device Test

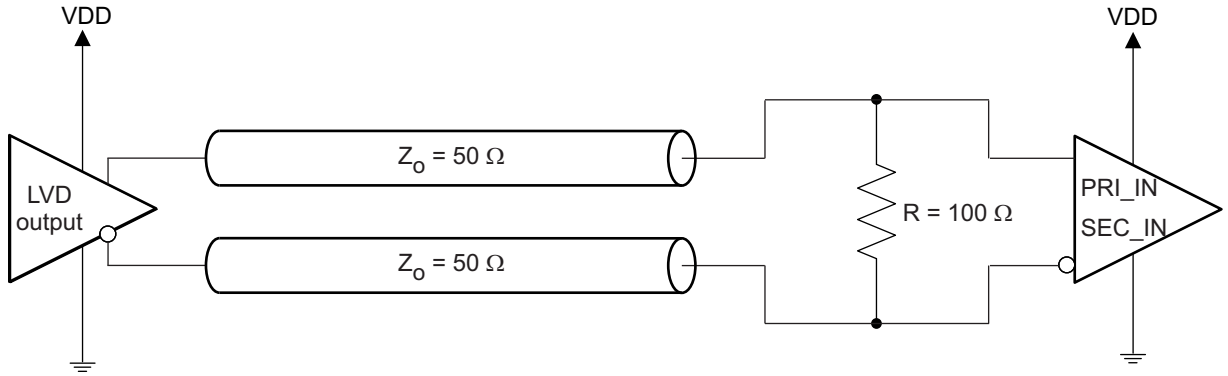


Figure 7. LVDS Input Configuration During Device Test

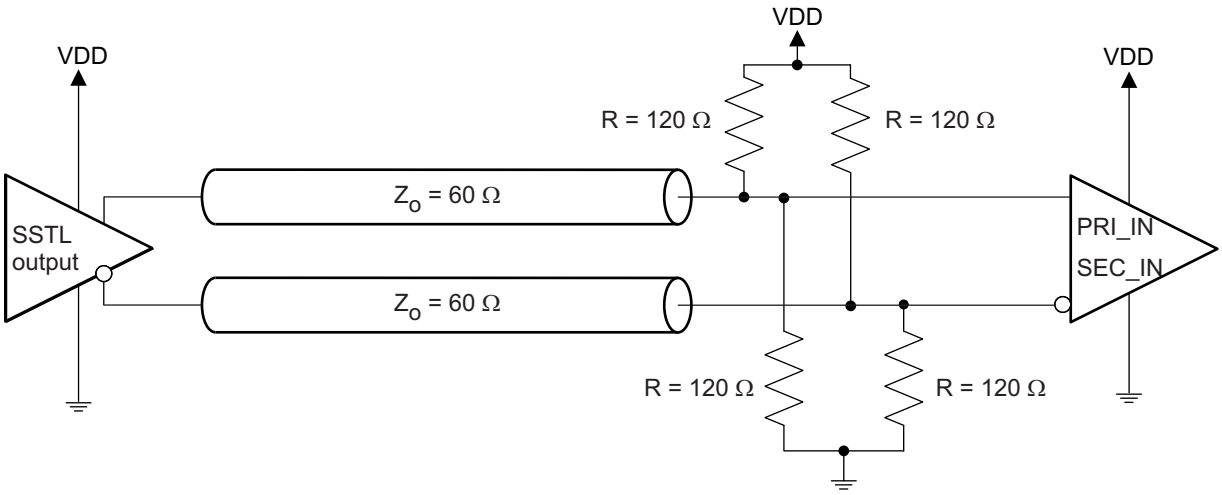


Figure 8. SSTL Input Configuration During Device Test

APPLICATION INFORMATION

Typical Application Load

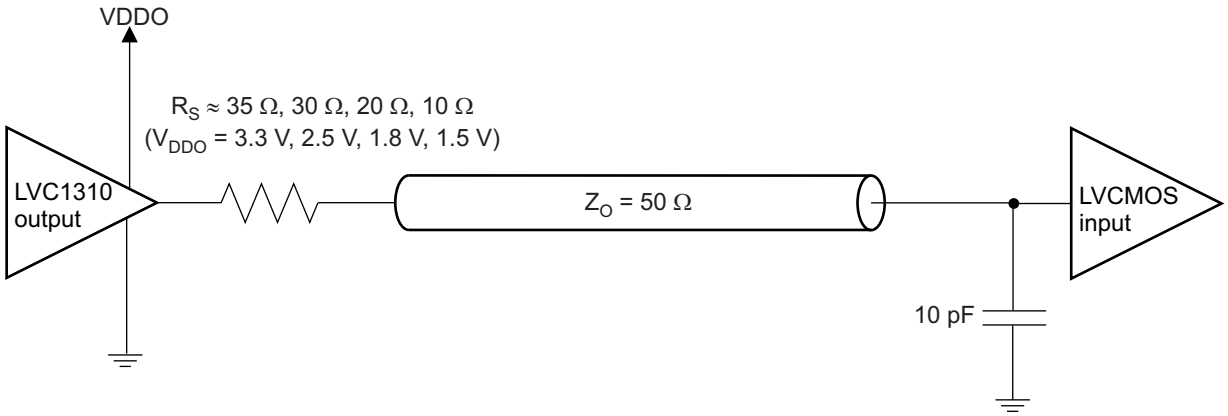


Figure 9. LVCMOS Output DC Configuration: Typical Application Load

Parameter Measurement Information

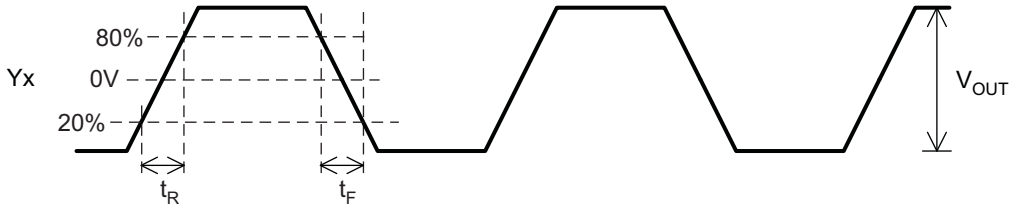


Figure 10. LVCMOS Output Voltage and Rise/Fall Time

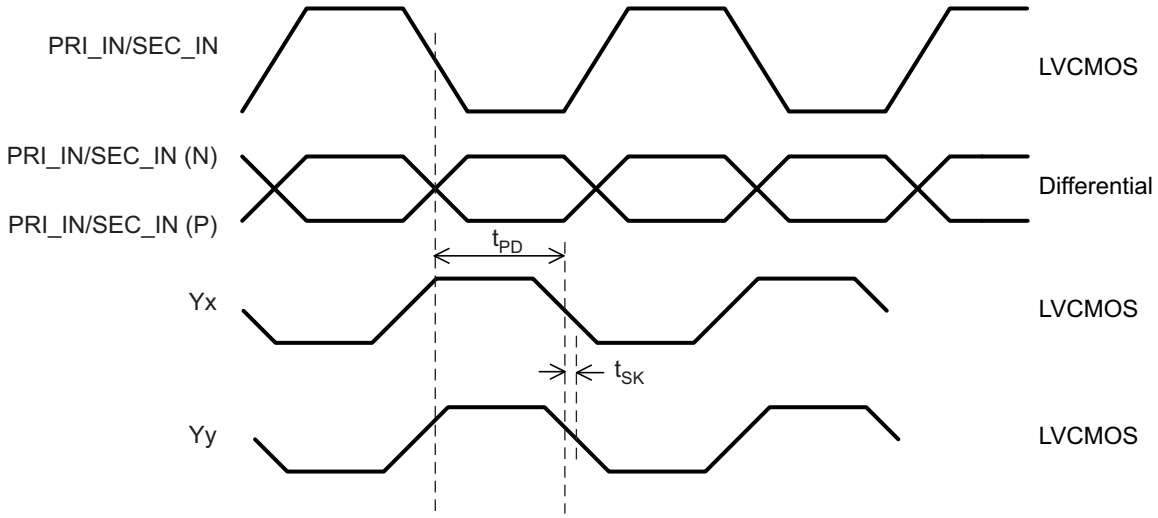


Figure 11. Differential and Single-Ended Output Skew and Propagation Delay

Crystal Oscillator Input

The crystal oscillator circuit is characterized with 18-pF parallel resonant crystals. C1 and C2 were chosen to minimize the ppm error. $R_{OPTIONAL}$ can be placed to limit the drive level of the oscillator circuit.

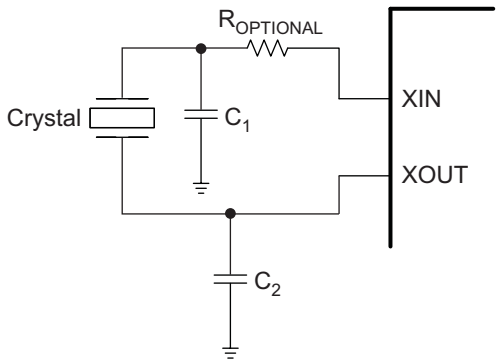


Figure 12. Crystal Reference Input

The input XIN can accept single-ended LVCMOS signals in two configurations. It is possible to overdrive the oscillator stage or to use a pure LVCMOS input (see Table 1). If the oscillator stage is overdriven, the input must be ac-coupled with a capacitor (see Figure 13). Otherwise, if the bypass mode is selected, a coupling capacitor is not required.

NOTE

If overdrive or bypass mode is used, the device is functional, but the ac parameters may not be met.

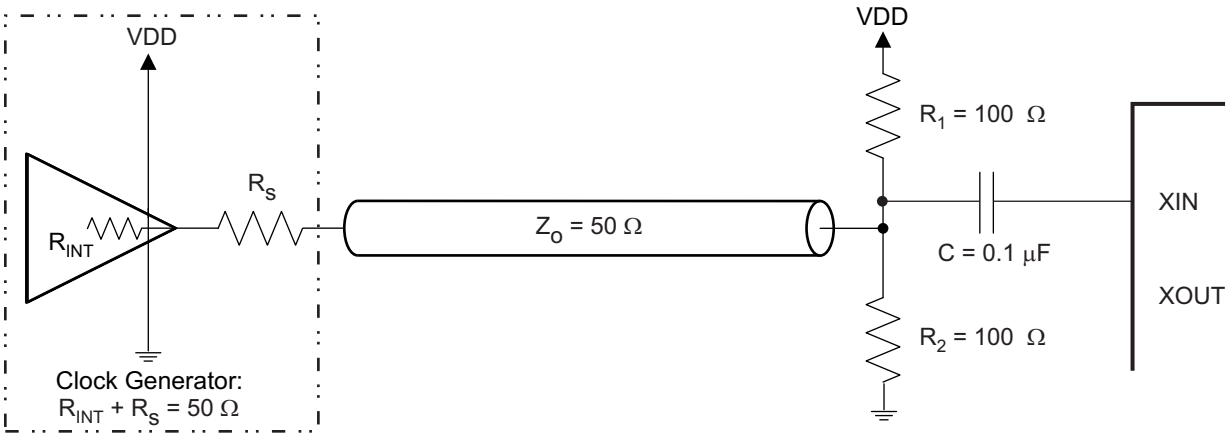


Figure 13. Single-Ended Crystal Input

Phase Noise Performance

The CDCLVC1310 provides ultralow phase-noise outputs (noise floor = –170 dBc/Hz) if a crystal is attached to it. Figure 14 shows the phase-noise plot of the CDCLVC1310 with a 25-MHz crystal at V_{DD} = V_{DDO} = 3.3 V and room temperature.

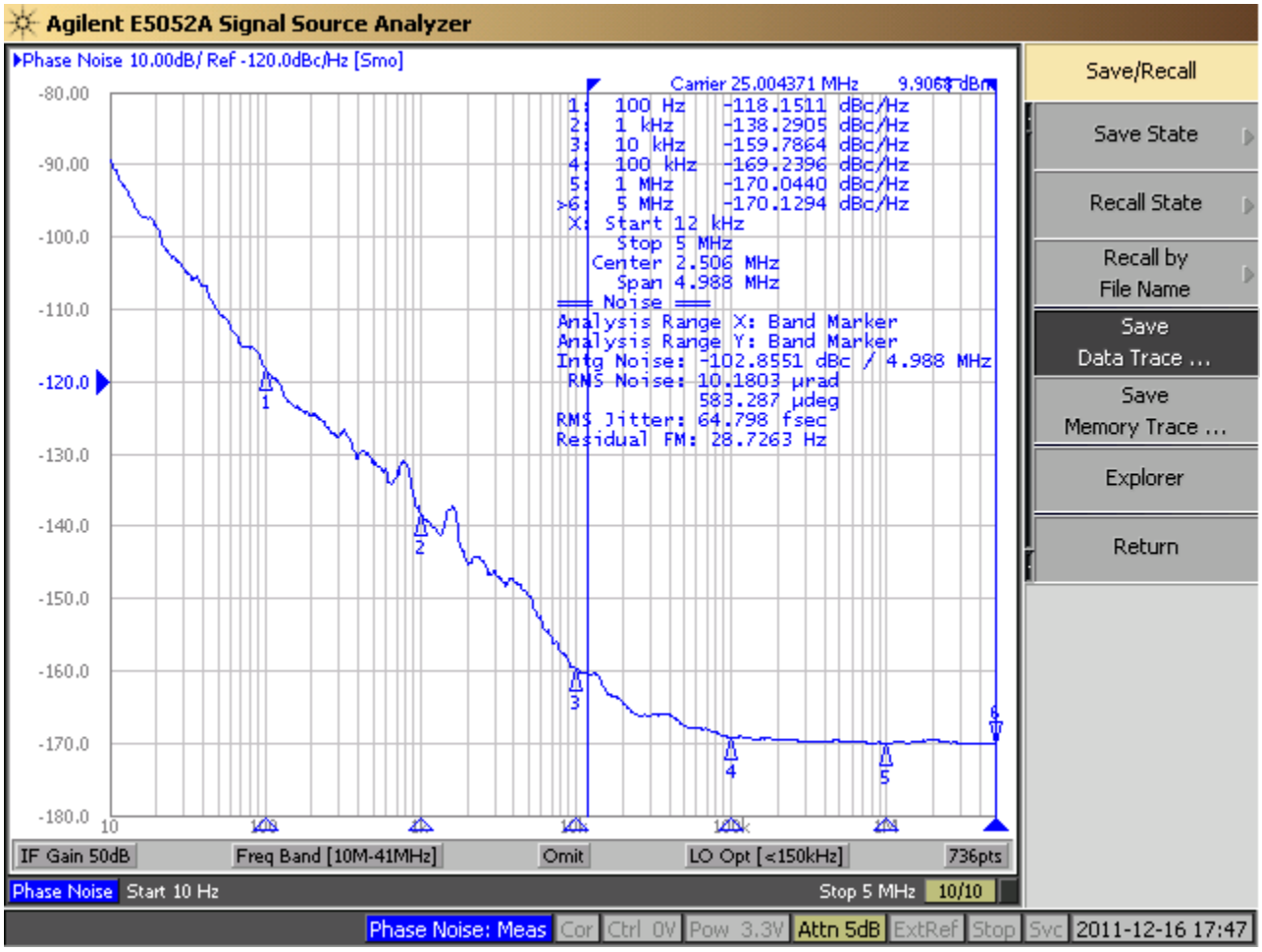


Figure 14. Phase Noise Profile With 25-MHz Crystal at Nominal Conditions

System-Level Additive Jitter Measurement

For high-performance devices, phase-noise measurements are influenced by limitations of the equipment. The noise floor of the equipment often exceeds the noise floor of the device. The real noise floor of the device is probably lower (see LVCMOS Output Characteristics). Phase noise is influenced by the input source and the measurement equipment. Additional measurements and information about system-level additive jitter and noise floor are available in the applications report *Phase Noise Performance of CDCLVC1310* (SCAA115).

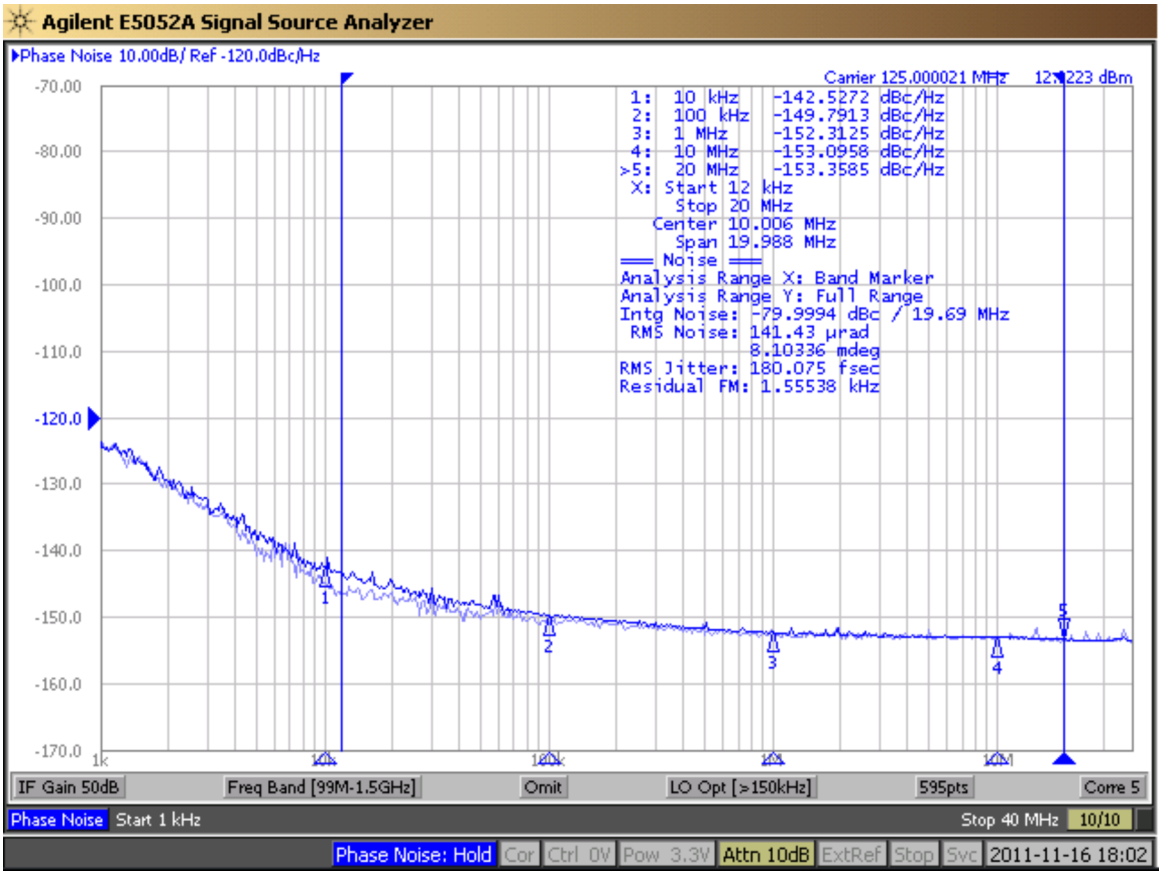


Figure 15. Input Phase Noise (179.4 fs, Light Blue) and Output Phase Noise (180 fs, Dark Blue)

Output Enable

If OE is pulled to LOW (t1), the outputs are forced to the high-impedance state after the next falling edge of the input signal (t2). The outputs remain in the high-impedance state as long as OE is LOW (see Figure 16).

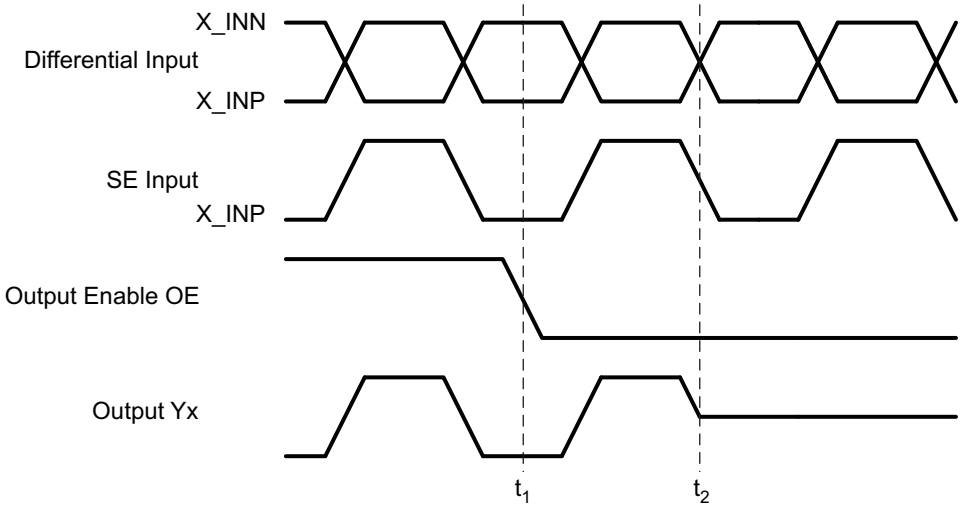


Figure 16. OE: Disable Outputs

If the outputs are in the high-impedance state and OE is pulled to HIGH, all outputs are forced to LOW asynchronously (t3). Within two clock cycles (maximum), the outputs start switching again (t4), after a falling edge of the input signal (see Figure 17).

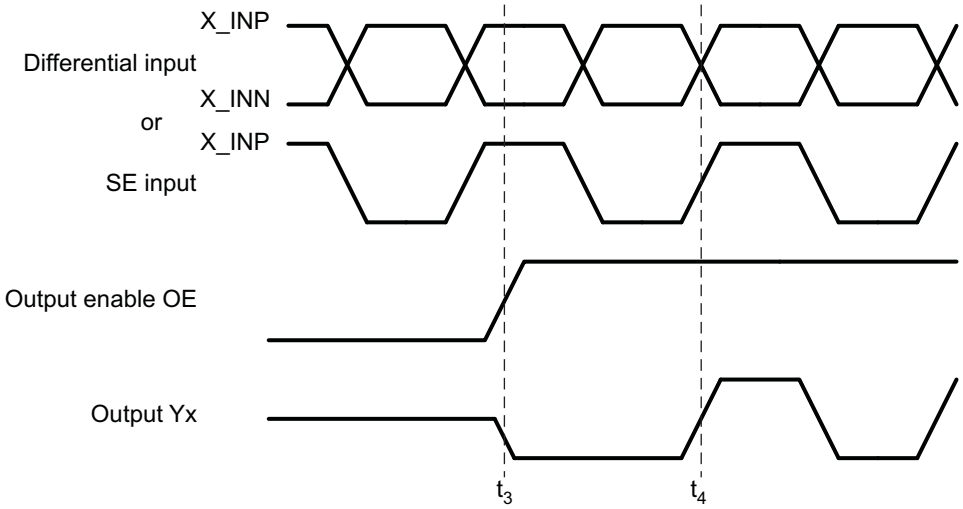


Figure 17. OE: Enable Outputs

If the outputs are in the high-impedance state and the input is static (no clock signal), OE works fully asynchronously. A transition of OE from LOW to HIGH forces the outputs to LOW. A transition from HIGH to LOW does not force to the high-impedance state again. Therefore, a falling edge of the input signal is needed (see Figure 16).

MUX Isolation

MUX isolation is defined as difference in output amplitude (dB) with an active or a static input signal.

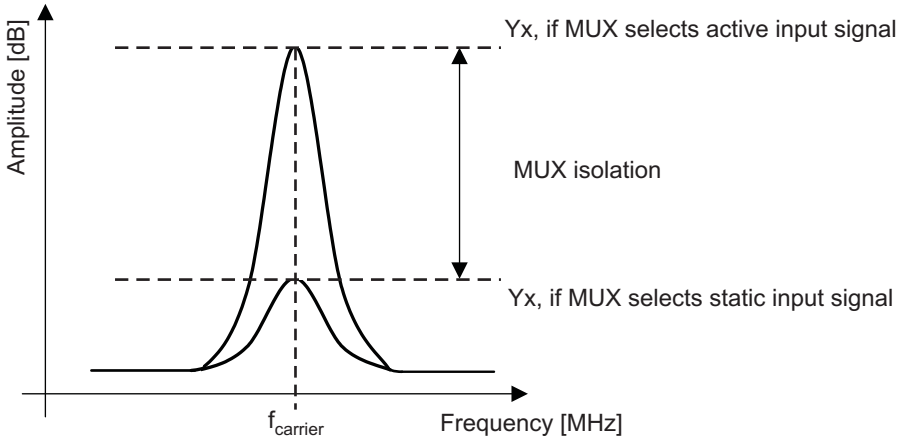
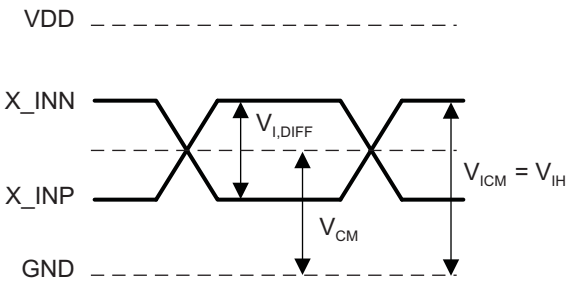


Figure 18. Output Spectrum of an Active and a Static Input Signal

Differential Input Level



NOTE: VCM can be calculated with: $V_{CM} = V_{DD} – V_{ICM} – V_{I,DIFF}/2$

Figure 19. Differential Input Level

Power Consideration

The following power consideration refers to the device-consumed power consumption only. The device power consumption is the sum of static power and dynamic power. The dynamic power usage consists of two components:

- Power used by the device as it switches states
- Power required to charge any output load

The output load can be capacitive-only or capacitive and resistive. The following formula can be used to calculate the power consumption of the device:

$P_{Dev} = P_{stat} + P_{dyn} + P_{Cload}$ (see Figure 20 and Figure 21)

$P_{stat} = I_{DD} \times V_{DD}$

$P_{dyn} + P_{Cload} = (I_{DD,dyn} + I_{DD,Cload}) \times V_{DDO}$

where:

$I_{DD,dyn} = C_{PD} \times V_{DDO} \times f \times n$ [mA] (see Figure 22)

$I_{DD,Cload} = C_{load} \times V_{DDO} \times f \times n$ [mA]

Example for power consumption of the CDCLVC1310: 10 outputs are switching, f = 100 MHz, $V_{DD} = V_{DDO}$ = 3.3 V and assuming C_{load} = 2 pF per output:

P_{Dev} = 46.2 mW + 117.5 mW = 163.7 mW

P_{stat} = 14 mA × 3.3 V = 46.2 mW

$P_{dyn} + P_{Cload}$ = (29 mA + 6.6 mA) x 3.3V = 117.5 mW

$I_{DD,dyn}$ = 8.8 pF × 3.3 V × 100 MHz × 10 = 29 mA

$I_{DD,Cload}$ = 2 pF × 3.3 V x 100 MHz × 10 = 6.6 mA

NOTE

For dimensioning the power supply, the total power consumption must be considered. The total power consumption is the sum of device power consumption and the power consumption of the load.

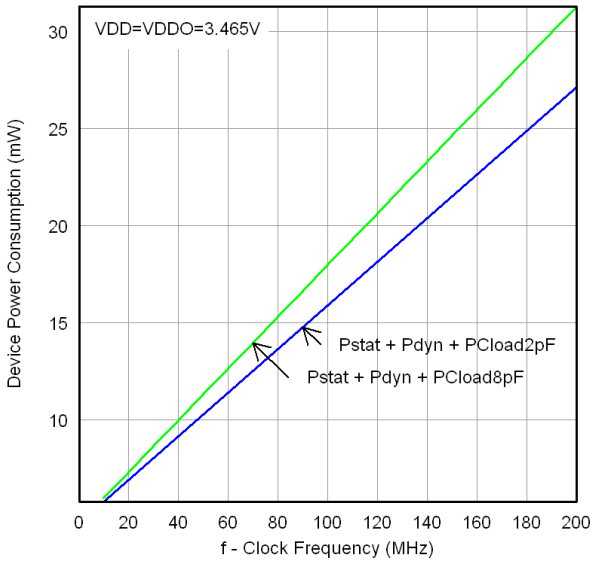


Figure 20. Device Power Consumption vs Clock Frequency (VDD = VDDO = 3.465 V; Load 2 pF, 8 pF; per Output)

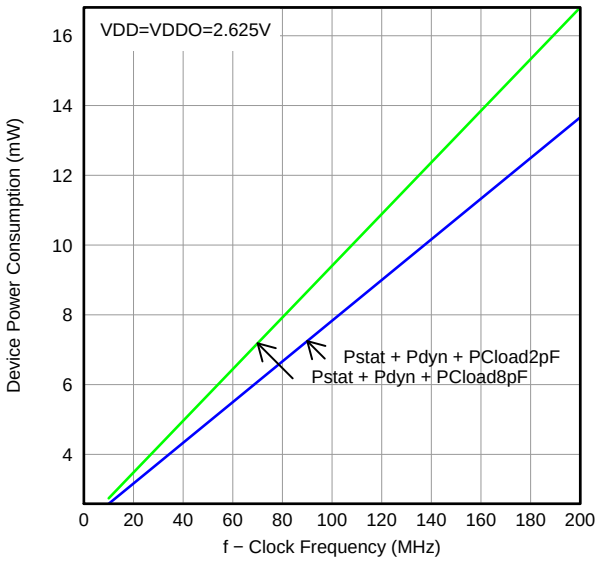


Figure 21. Device Power Consumption vs Clock Frequency (VDD = VDDO = 2.625 V; Load 2 pF, 8 pF; per Output)

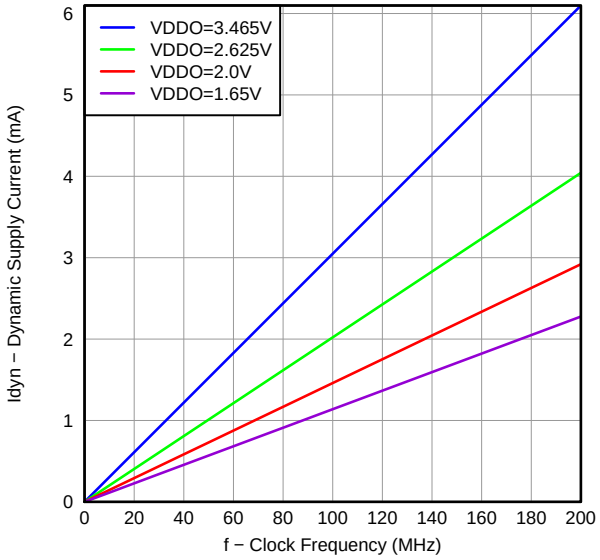


Figure 22. Dynamic Supply Current vs Clock Frequency (per Output)

Thermal Management

Power consumption of the CDCLVC1310 can be high enough to require attention to thermal management. For reliability and performance reasons, the die temperature should be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times θ_{JA} should not exceed 125°C.

The device package has an exposed pad that provides the primary heat removal path as well as an electrical grounding to the printed circuit board (PCB). To maximize the removal of heat from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. A recommended land and via pattern is shown in Figure 23.

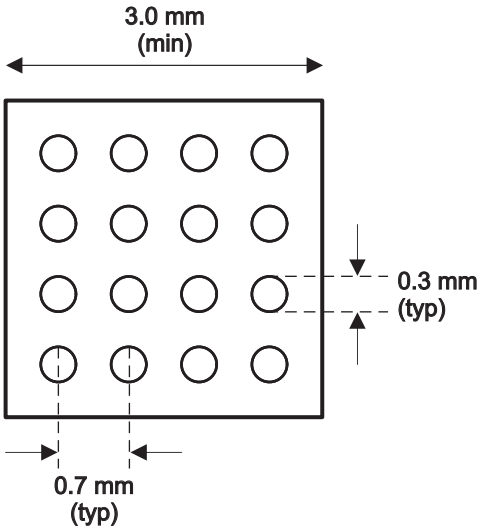


Figure 23. Recommended PCB Layout for CDCLVC1310

Power Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from power supply, where the bypass capacitors provide the very low-impedance path for high-frequency noise and guard the power-supply system against induced fluctuations. The bypass capacitors also provide instantaneous current surges as required by the device, and should have low ESR. To use the bypass capacitors properly, they must be placed very close to the power supply pins and must be laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1-μF) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock driver, preventing them from leaking into the board supply. Choosing an appropriate ferrite bead with very low dc resistance is important, because it is imperative to provide adequate isolation between the board supply and the chip supply, and to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

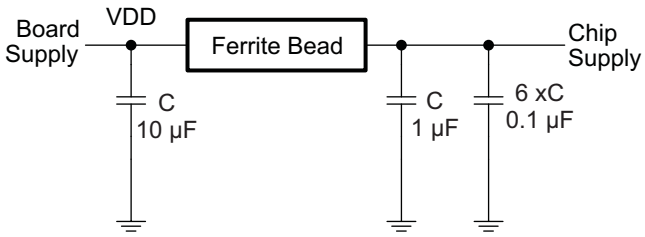


Figure 24. Power-Supply Decoupling

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CDCLVC1310RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	

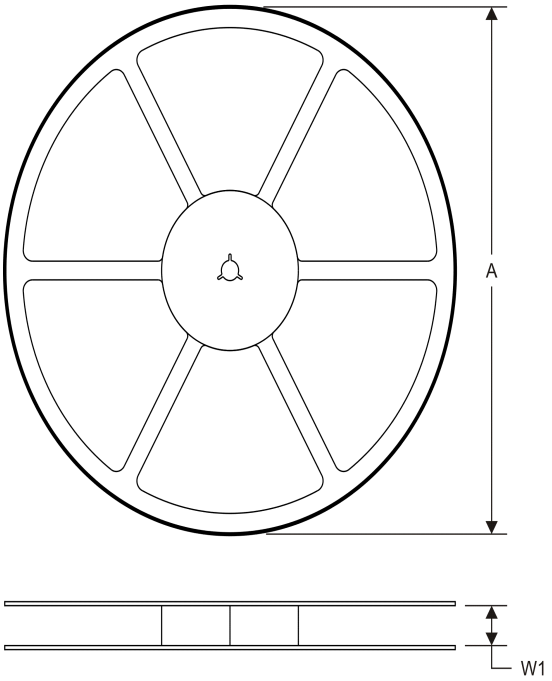
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

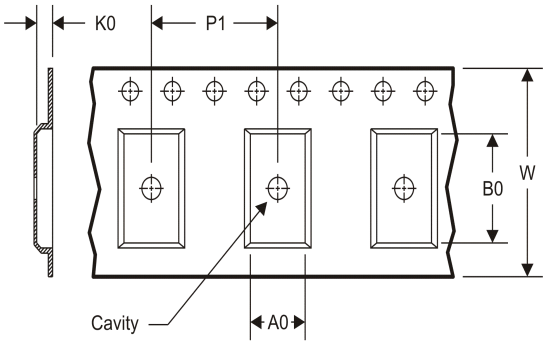
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



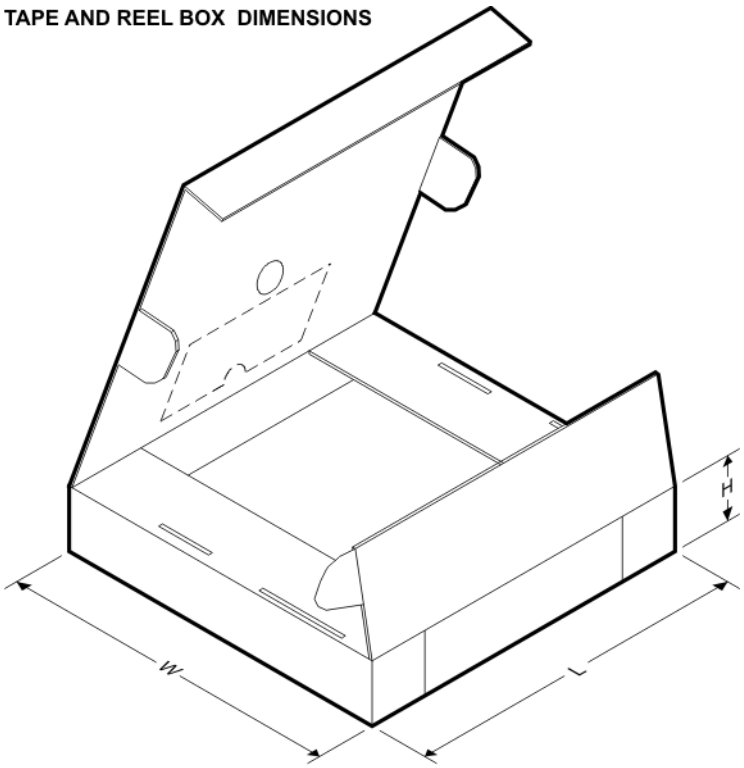
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVC1310RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

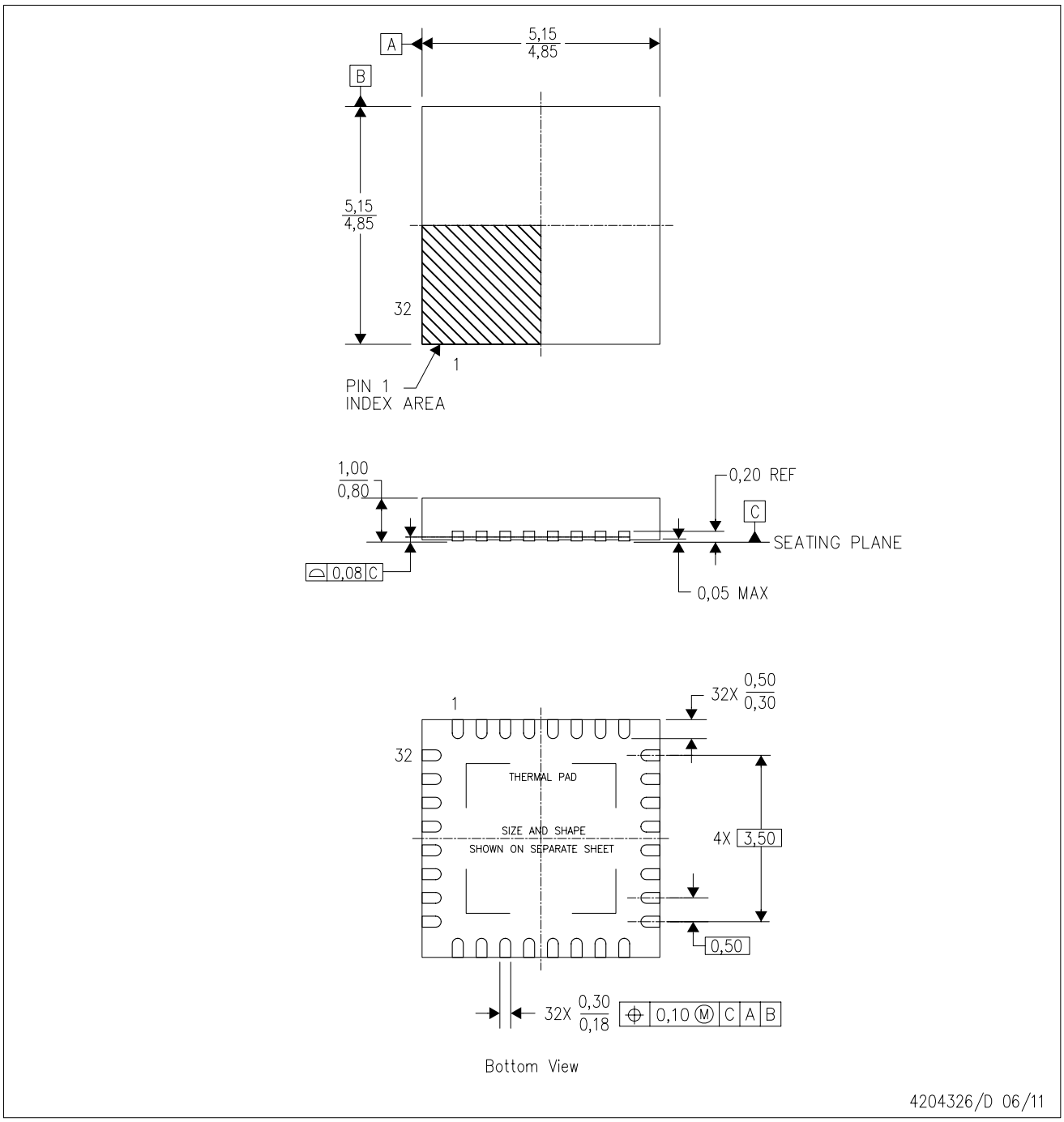
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVC1310RHBR	QFN	RHB	32	3000	367.0	367.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

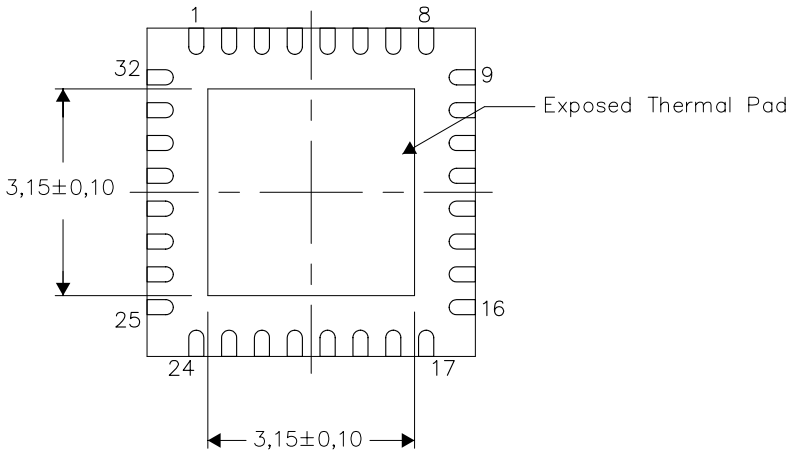
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



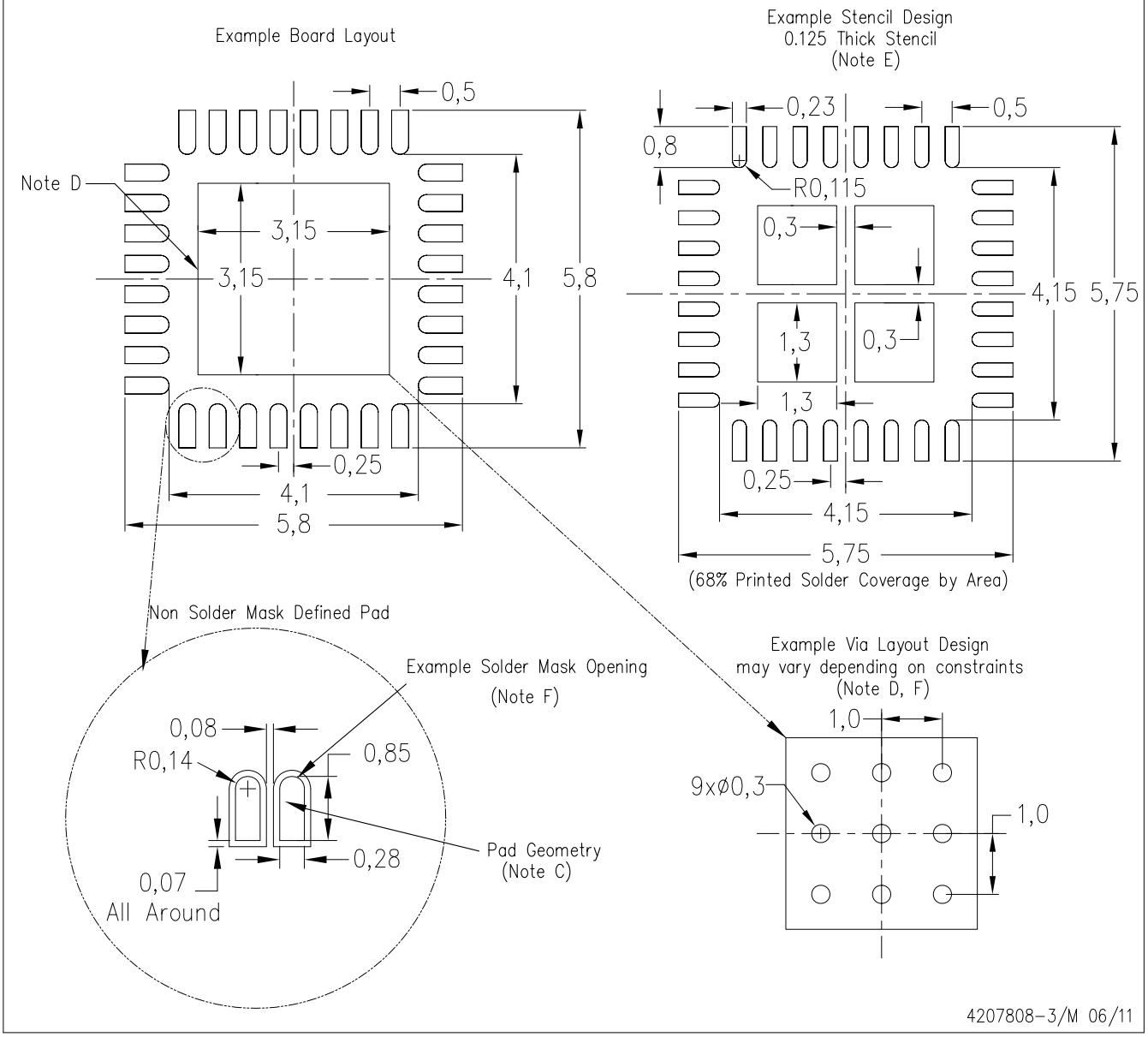
Bottom View

Exposed Thermal Pad Dimensions

4206356–3/U 06/11

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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