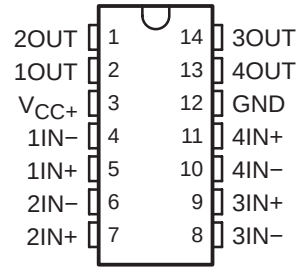
LMV331 SINGLE, LMV393 DUAL, LMV339 QUAD GENERAL-PURPOSE LOW-VOLTAGE COMPARATORS

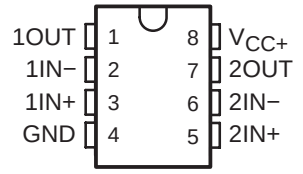
SLCS136M − AUGUST 1999 − REVISED NOVEMBER 2005

- **2.7-V and 5-V Performance**
- **Low Supply Current:**
  - **LMV331 . . . 60 μA Typ**
  - **LMV393 . . . 100 μA Typ**
  - **LMV339 . . . 170 μA Typ**
- **Input Common-Mode Voltage Range Includes Ground**
- **Low Output Saturation Voltage . . . 200 mV Typ**
- **Open-Collector Output for Maximum Flexibility**

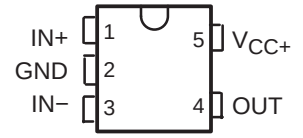
LMV339 . . . D OR PW PACKAGE
(TOP VIEW)



LMV393 . . . D, DDU, DGK, OR PW PACKAGE
(TOP VIEW)



LMV331 . . . DBV OR DCK PACKAGE
(TOP VIEW)



description/ordering information

The LMV393 and LMV339 devices are low-voltage (2.7 V to 5.5 V) versions of the dual and quad comparators, LM393 and LM339, which operate from 5 V to 30 V. The LMV331 is the single-comparator version.

The LMV331, LMV339, and LMV393 are the most cost-effective solutions for applications where low-voltage operation, low power, space saving, and price are the primary specifications in circuit design for portable consumer products. These devices offer specifications that meet or exceed the familiar LM339 and LM393 devices at a fraction of the supply current.

ORDERING INFORMATION

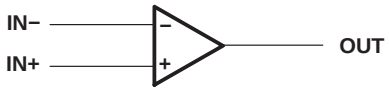
T_A		PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	Single	SC-70 (DCK)	Reel of 3000	LMV331IDCKR	R2_
			Reel of 250	LMV331IDCKT	
		SOT23-5 (DBV)	Reel of 3000	LMV331IDBVR	R1I_
			Reel of 250	LMV331IDBVT	
	Dual	MSOP/VSSOP (DGK)	Reel of 2500	LMV393IDGKR	R9_
		SOIC (D)	Tube of 75	LMV393ID	MV393I
			Reel of 2500	LMV393IDR	
		TSSOP (PW)	Tube of 90	LMV393IPW	MV393I
			Reel of 2000	LMV393IPWR	
		VSSOP (DDU)	Reel of 2000	LMV393IDDUR	RABR
	Quad	SOIC (D)	Tube of 50	LMV339ID	LMV339I
			Reel of 2500	LMV339IDR	
		TSSOP (PW)	Tube of 150	LMV339IPW	MV339I
			Reel of 2000	LMV339IPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

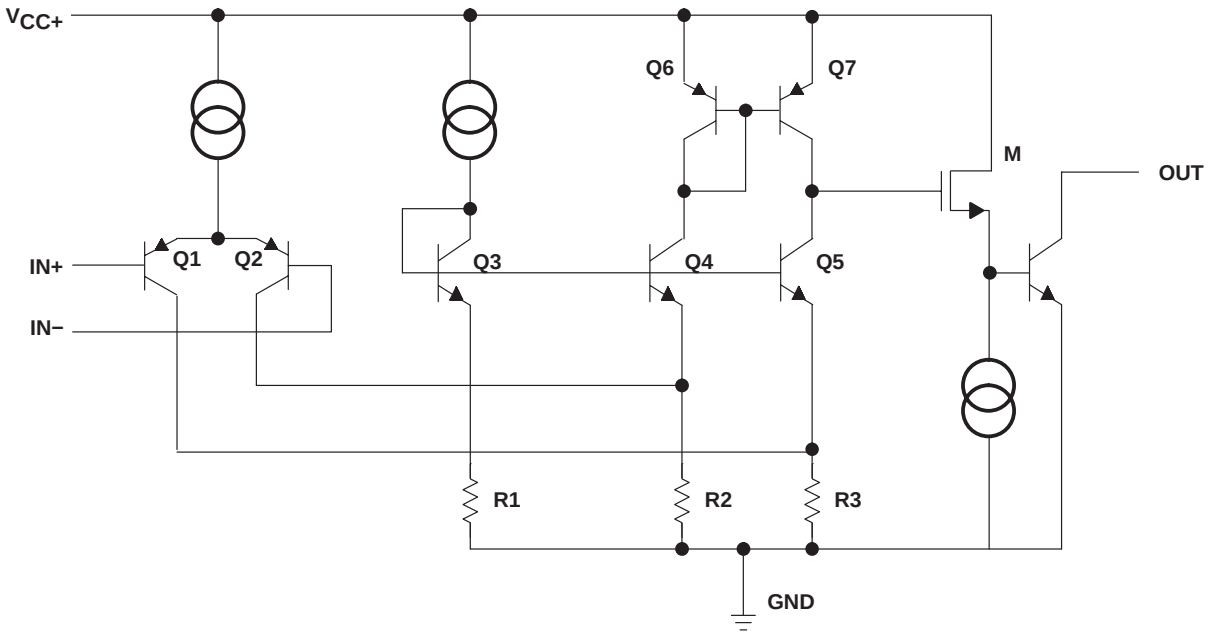
‡ DBV/DCK/DGK: The actual top-side marking has one additional character that designates the assembly/test site.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

symbol (each comparator)



simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	5.5 V
Differential input voltage, V_{ID} (see Note 2)	±5.5 V
Input voltage range, V_I (either input)	0 V to 5.5 V
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D (8-pin) package	97°C/W
D (14-pin) package	86°C/W
DBV package	206°C/W
DCK package	252°C/W
DDU package	TBD°C/W
DGK package	172°C/W
PW (8-pin) package	149°C/W
PW (14-pin) package	113°C/W
Operating virtual junction temperature, T_J	150°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values (except differential voltages and V_{CC+} specified for the measurement of I_{OS}) are with respect to the network GND.
2. Differential voltages are at IN+ with respect to IN−.
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) − T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC+}	Supply voltage (single-supply operation)	2.7	5.5	V
V_{OUT}	Output voltage		V_{CC+} + 0.3	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics at specified free-air temperature, V_{CC+} = 2.7 V, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		1.7	7	mV
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage		−40°C to 85°C		5		μV/°C
I_{IB}	Input bias current		25°C		10	250	nA
			−40°C to 85°C			400	
I_{IO}	Input offset current		25°C		5	50	nA
			−40°C to 85°C			150	
I_O	Output current (sinking)	$V_O \le 1.5$ V	25°C	5	23		mA
	Output leakage current		25°C		0.003		μA
			−40°C to 85°C			1	
V_{ICR}	Common-mode input voltage range		25°C		−0.1 to 2		V
V_{SAT}	Saturation voltage	$I_O \le 1$ mA	25°C		200		mV
I_{CC}	Supply current	LMV331	25°C		40	100	μA
		LMV393 (both comparators)	25°C		70	140	
		LMV339 (all four comparators)	25°C		140	200	

switching characteristics, T_A = 25°C, V_{CC+} = 2.7 V, R_L = 5.1 kΩ, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_{PHL}	Propagation delay, high- to low-level output switching	Input overdrive = 10 mV	1000	ns
		Input overdrive = 100 mV	350	
t_{PLH}	Propagation delay, low- to high-level output switching	Input overdrive = 10 mV	500	ns
		Input overdrive = 100 mV	400	

electrical characteristics at specified free-air temperature, V_{CC+} = 5 V, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		1.7	7	mV
			−40°C to 85°C			9	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage		25°C		5		μV/°C
I_{IB}	Input bias current		25°C		25	250	nA
			−40°C to 85°C			400	
I_{IO}	Input offset current		25°C		2	50	nA
			−40°C to 85°C			150	
I_O	Output current (sinking)	$V_O \le 1.5$ V	25°C	10	84		mA
	Output leakage current		25°C		0.003		μA
			−40°C to 85°C			1	
V_{ICR}	Common-mode input voltage range		25°C		−0.1 to 4.2		V
A_{VD}	Large-signal differential voltage gain		25°C	20	50		V/mV
V_{SAT}	Saturation voltage	$I_O \le 4$ mA	25°C		200	400	mV
			−40°C to 85°C			700	
I_{CC}	Supply current	LMV331	25°C		60	120	μA
			−40°C to 85°C			150	
		LMV393 (both comparators)	25°C		100	200	
			−40°C to 85°C			250	
		LMV339 (all four comparators)	25°C		170	300	
			−40°C to 85°C			350	

switching characteristics, T_A = 25°C, V_{CC+} = 5 V, R_L = 5.1 kΩ, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_{PHL}	Propagation delay, high- to low-level output switching	Input overdrive = 10 mV	600	ns
		Input overdrive = 100 mV	200	
t_{PLH}	Propagation delay, low- to high-level output switching	Input overdrive = 10 mV	450	ns
		Input overdrive = 100 mV	300	

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PACKAGING INFORMATION

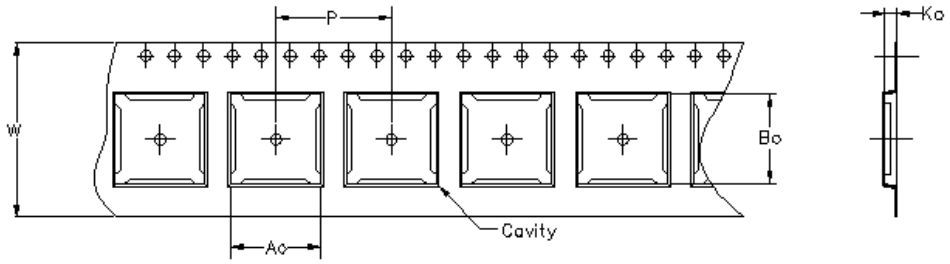
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
LMV331IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV331IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV331IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV331IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV331IDBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV331IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV331IDCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV331IDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV331IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV331IDCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV331IDCKTG4	ACTIVE	SC70	DCK	5	250	TBD	Call TI	Call TI
LMV339ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV339IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV339IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV339IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV339IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV339IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV339IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV339IPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV339IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV339IPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IDDURE4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
LMV393IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV393IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

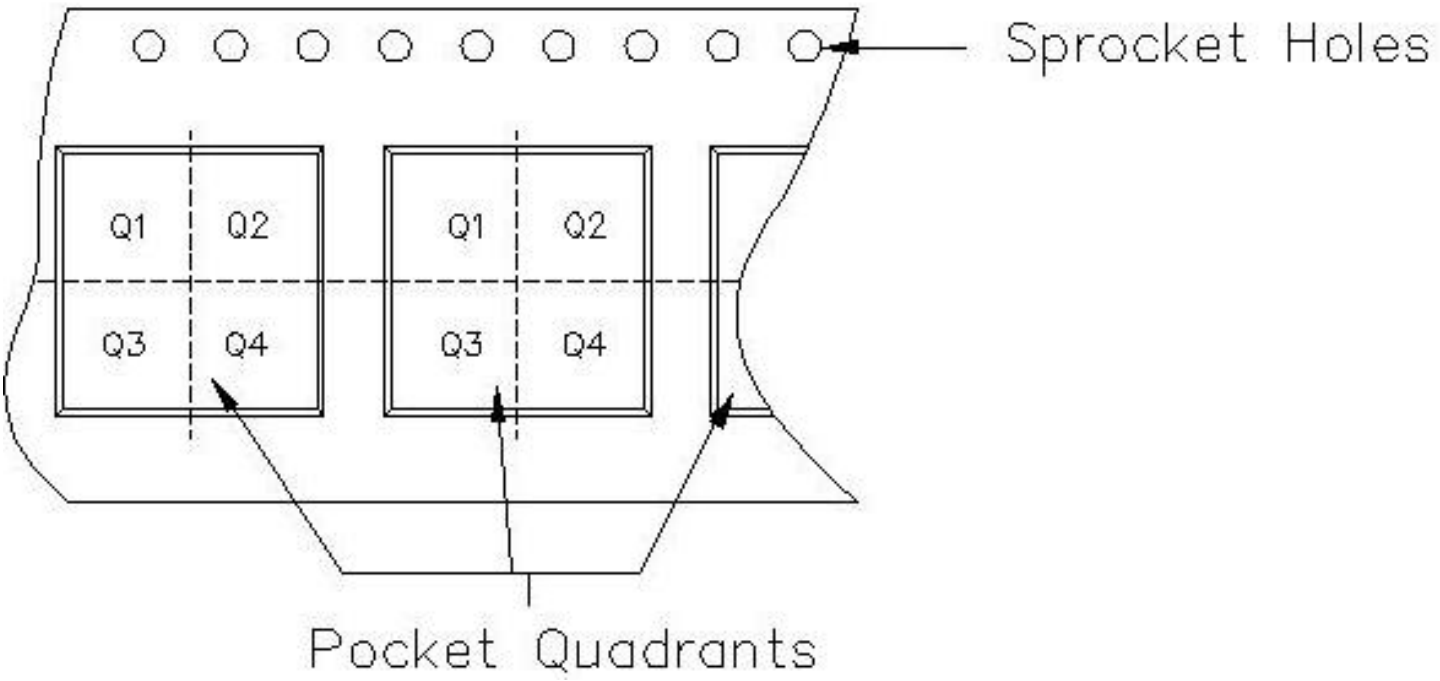
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



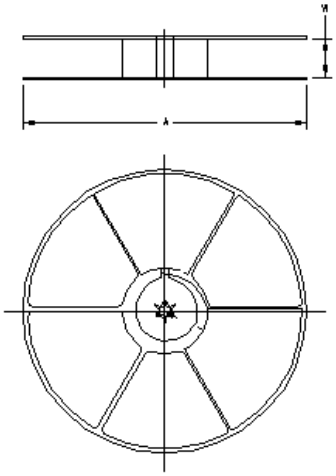
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



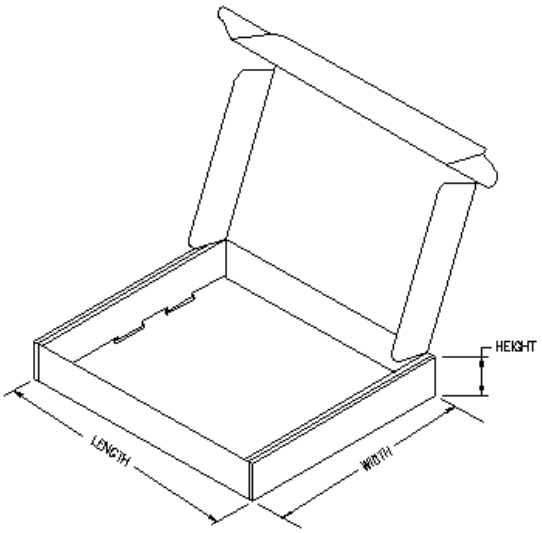
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV339IDR	D	14	MLA	330	16	6.5	9.0	2.1	8	16	Q1
LMV339IPWR	PW	14	MLA	330	12	7.0	5.6	1.6	8	12	Q1
LMV393IDGKR	DGK	8	HNT	180	13	5.3	3.4	1.4	8	12	Q1
LMV393IDR	D	8	FMX	330	12	6.4	5.2	2.1	8	12	Q1
LMV393IPWR	PW	8	MLA	330	12	7.0	3.6	1.6	8	12	Q1

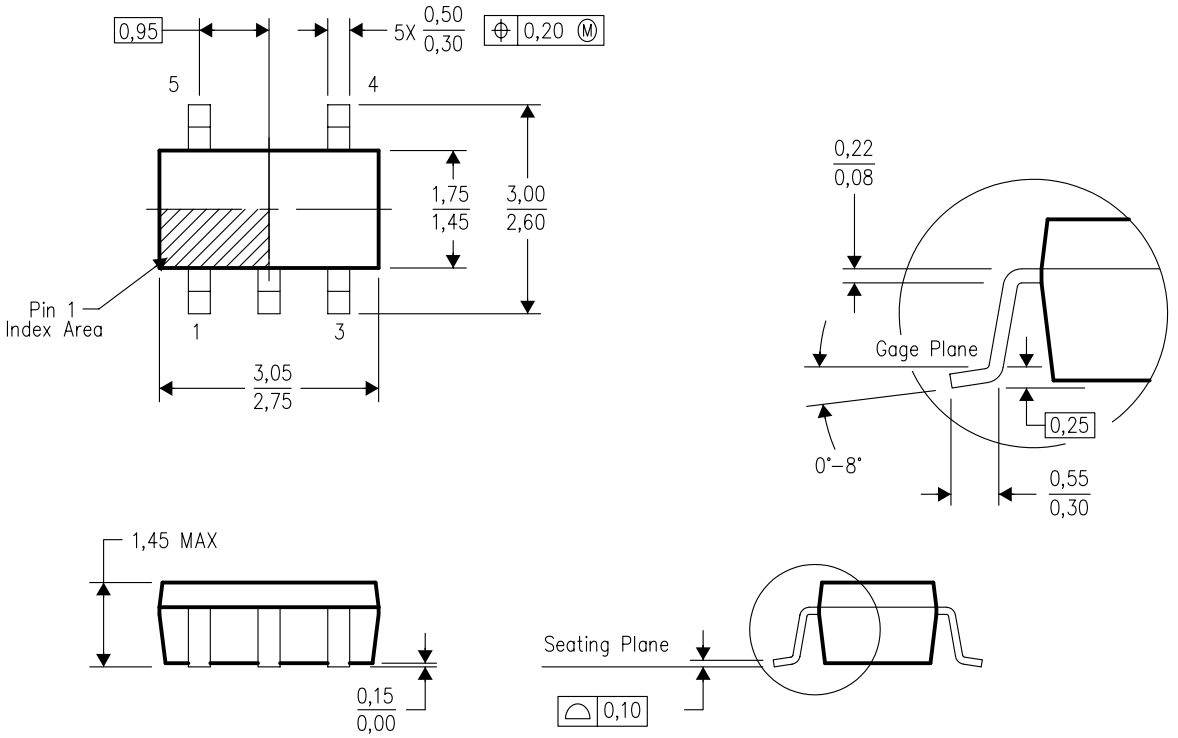


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
LMV339IDR	D	14	MLA	333.2	333.2	28.58
LMV339IPWR	PW	14	MLA	338.1	340.5	20.64
LMV393IDGKR	DGK	8	HNT	0.0	0.0	0.0
LMV393IDR	D	8	FMX	338.1	340.5	20.64
LMV393IPWR	PW	8	MLA	338.1	340.5	20.64


HEIGHT
LENGTH
WIDTH

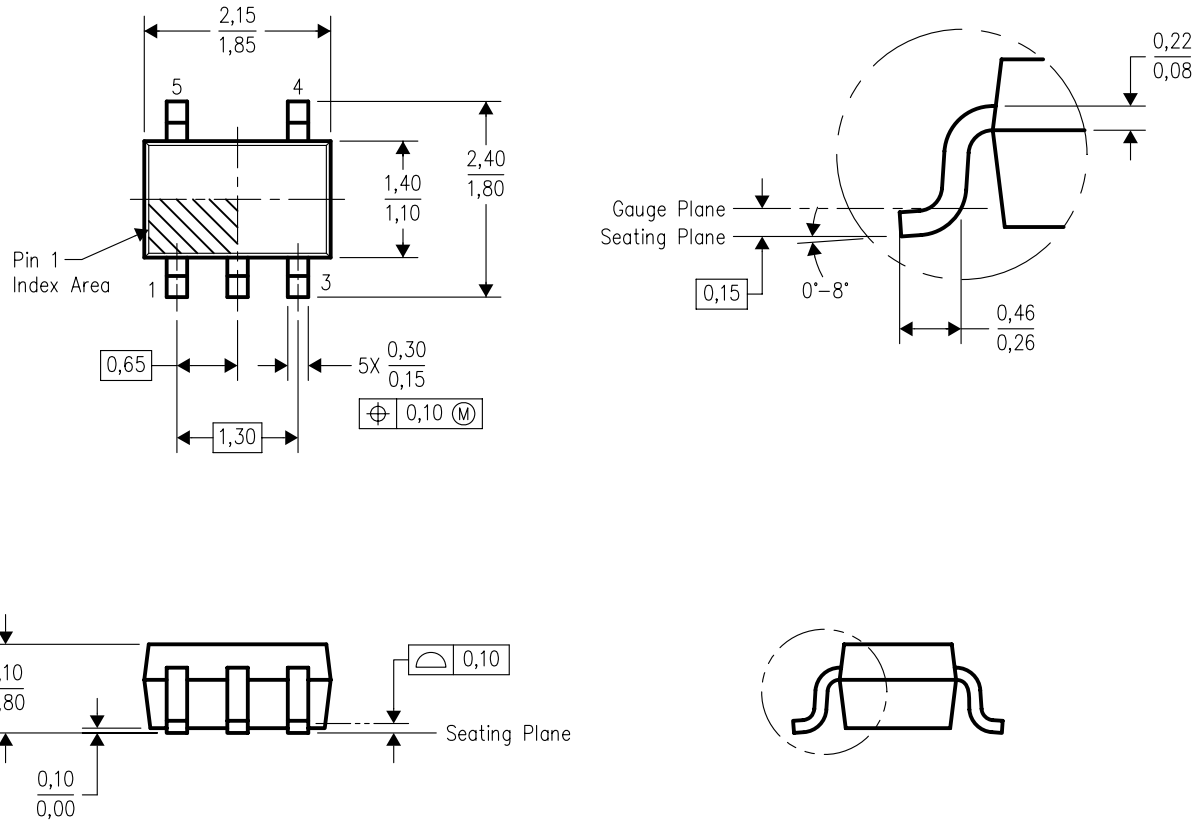
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

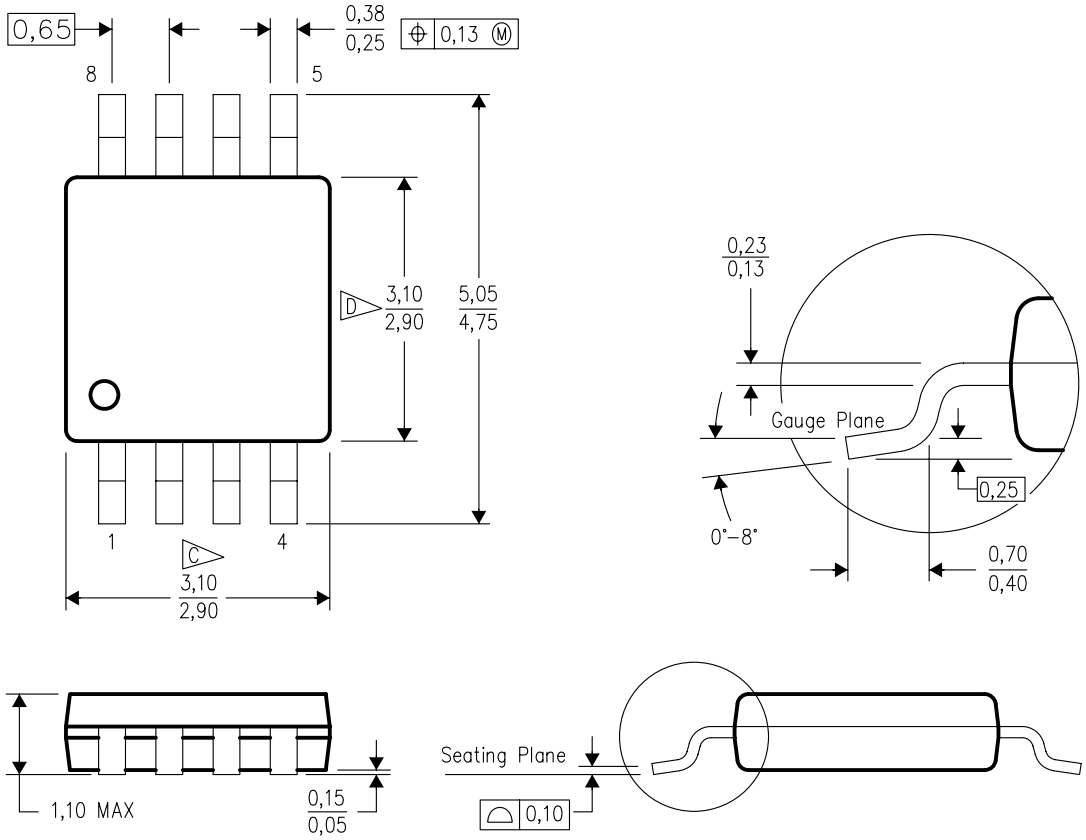
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

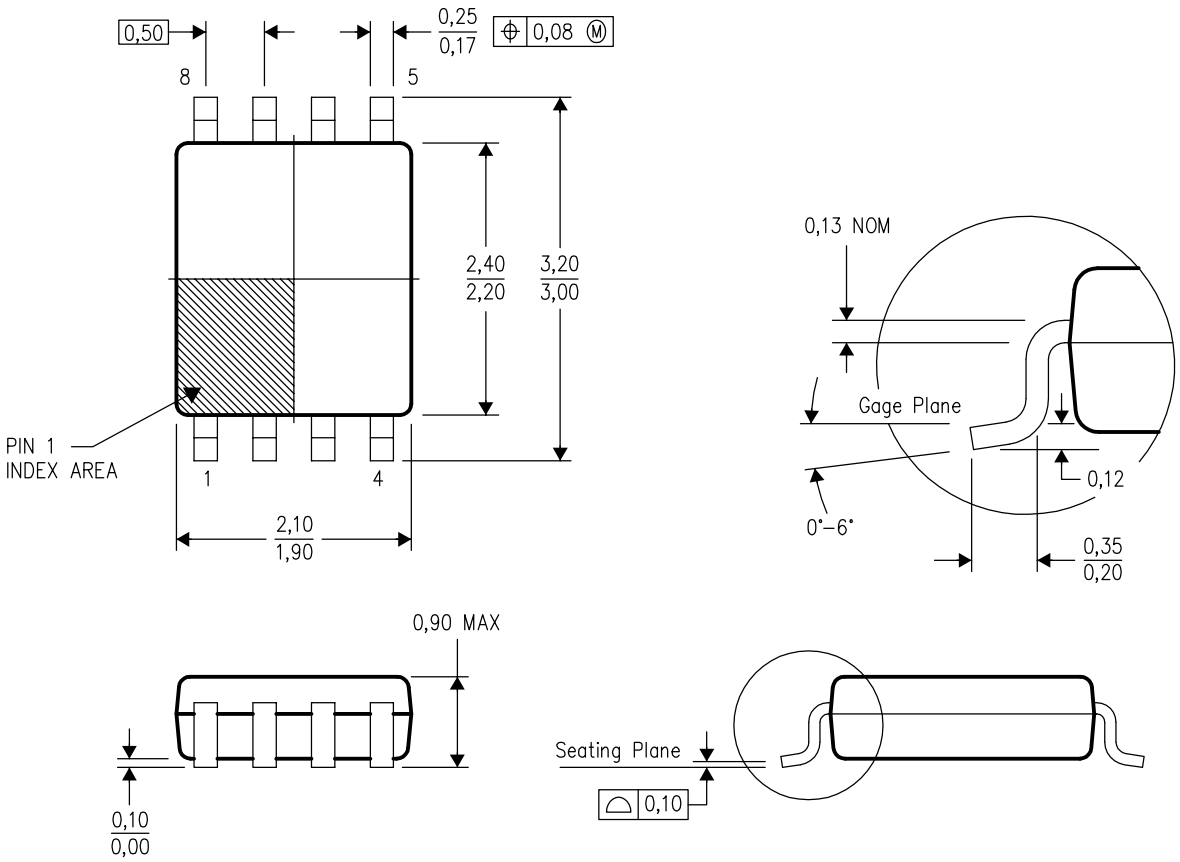
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

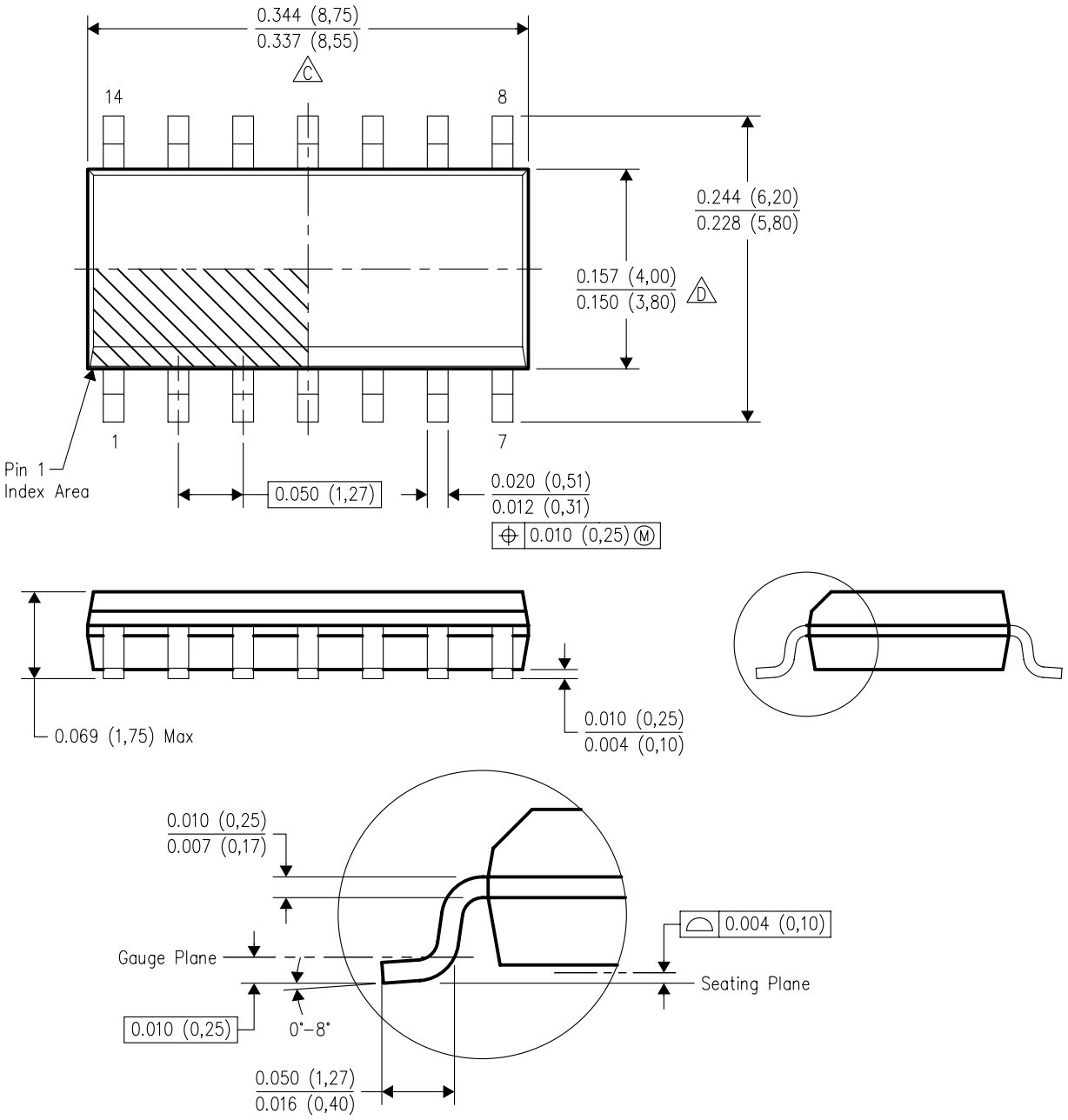
DDU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4205140/A 05/03

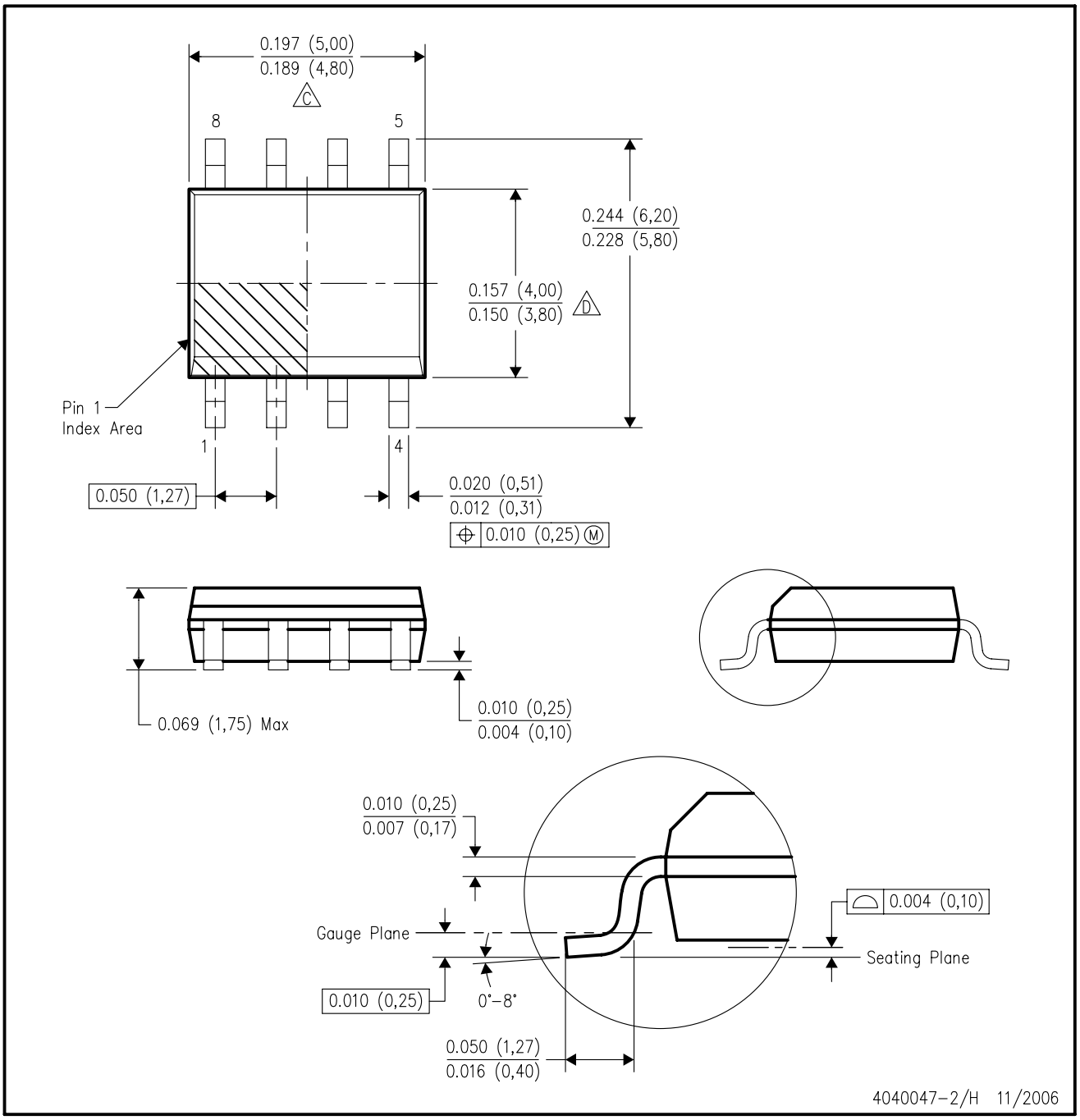
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation CA.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

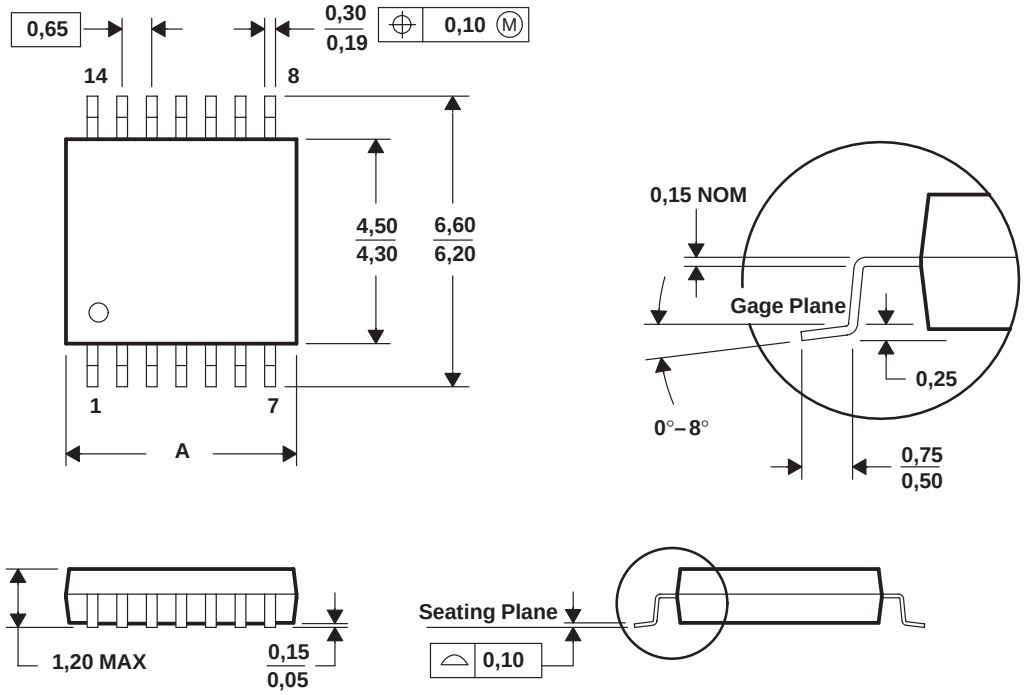
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153