

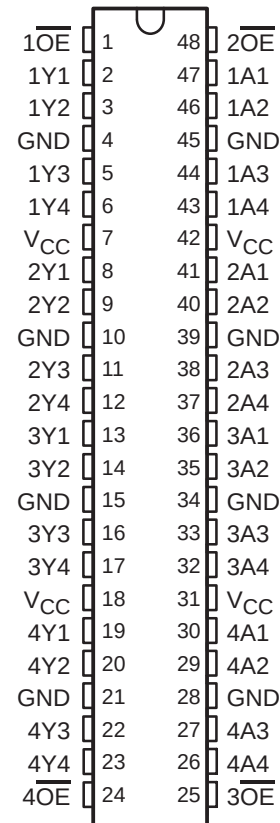
SN74LVC162244A

16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS664E – MARCH 2001 – REVISED SEPTEMBER 2003

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.4 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description/ordering information

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC162244A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (OE) inputs.

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74LVC162244ADL	LVC162244A
		Tape and reel	SN74LVC162244ADLR	
	TSSOP – DGG	Tape and reel	SN74LVC162244ADGGR	LVC162244A
	TVSOP – DGV	Tape and reel	SN74LVC162244ADGVR	LD2244A
	VFBGA – GQL	Tape and reel	SN74LVC162244AGQLR	LD2244A
	VFBGA – ZQL (Pb-free)		SN74LVC162244AZQLR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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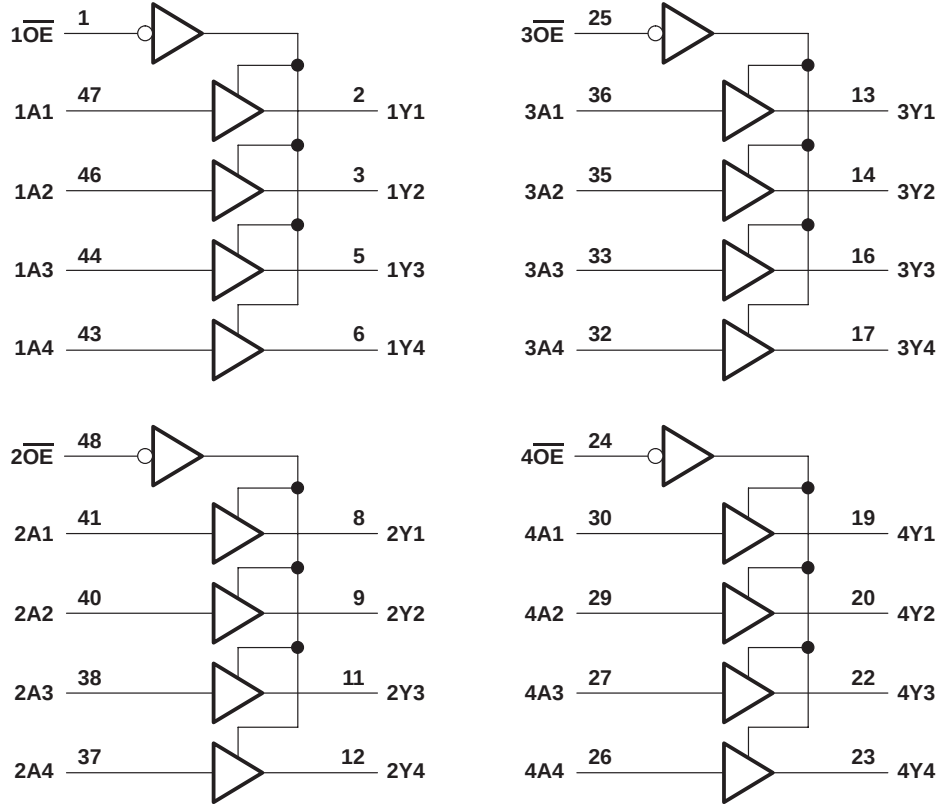
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To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

logic diagram (positive logic)



Pin numbers shown are for the DGG, DGV, and DL packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
GQL/ZQL package	42°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−2		mA
		V _{CC} = 2.3 V	−4		
		V _{CC} = 2.7 V	−8		
		V _{CC} = 3 V	−12		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	2		mA
		V _{CC} = 2.3 V	4		
		V _{CC} = 2.7 V	8		
		V _{CC} = 3 V	12		
Δt/Δv	Input transition rise or fall rate		10	ns/V	
T _A	Operating free-air temperature	−40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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16-BIT BUFFER/DRIVER
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	1.65 V to 3.6 V	V _{CC} - 0.2			V
	I _{OH} = -2 mA	1.65 V	1.2			
	I _{OH} = -4 mA	2.3 V	1.7			
		2.7 V	2.2			
	I _{OH} = -6 mA	3 V	2.4			
	I _{OH} = -8 mA	2.7 V	2			
	I _{OH} = -12 mA	3 V	2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 2 mA	1.65 V	0.45			
	I _{OL} = 4 mA	2.3 V	0.7			
		2.7 V	0.4			
	I _{OL} = 6 mA	3 V	0.55			
	I _{OL} = 8 mA	2.7 V	0.6			
	I _{OL} = 12 mA	3 V	0.8			
I _I	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _{off}	V _I or V _O = 5.5 V	0			±10	µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND	3.6 V			20	µA
	3.6 V ≤ V _I ≤ 5.5 V [‡]				20	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	V _I = V _{CC} or GND	3.3 V			5.5	pF
C _o	V _O = V _{CC} or GND	3.3 V			6	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.5	6	1	4.3	1	5.6	1.1	4.4	ns
t _{en}	$\overline{\text{OE}}$	Y	1.5	7.3	1	5	1	6.9	1	5.5	ns
t _{dis}	$\overline{\text{OE}}$	Y	1.5	8.9	1	5.5	1	6.8	1.8	6.3	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	31	33	35	pF
		Outputs disabled		2	3	4	



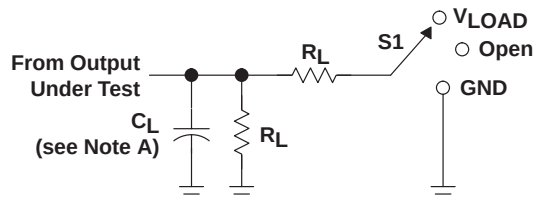
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16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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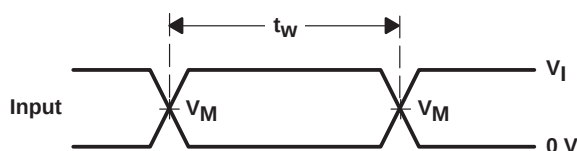
PARAMETER MEASUREMENT INFORMATION



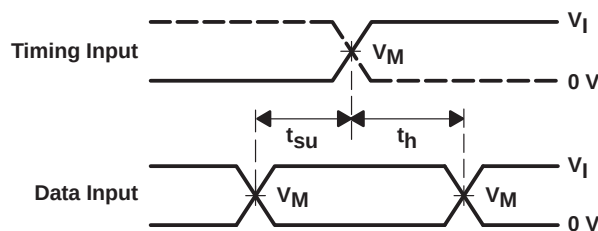
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

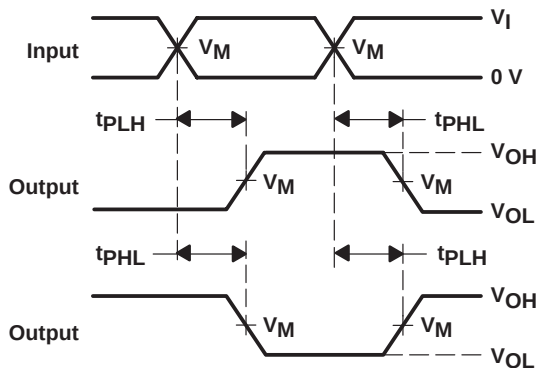
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



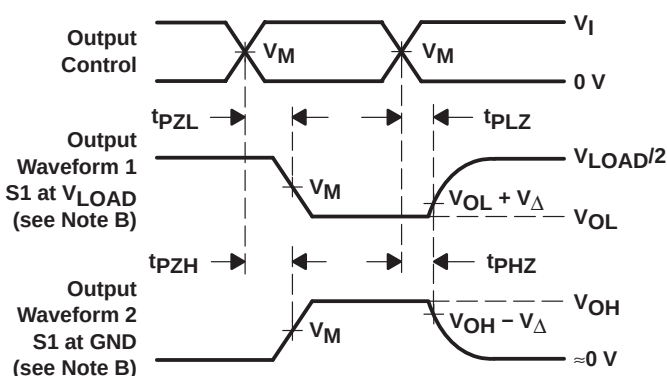
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

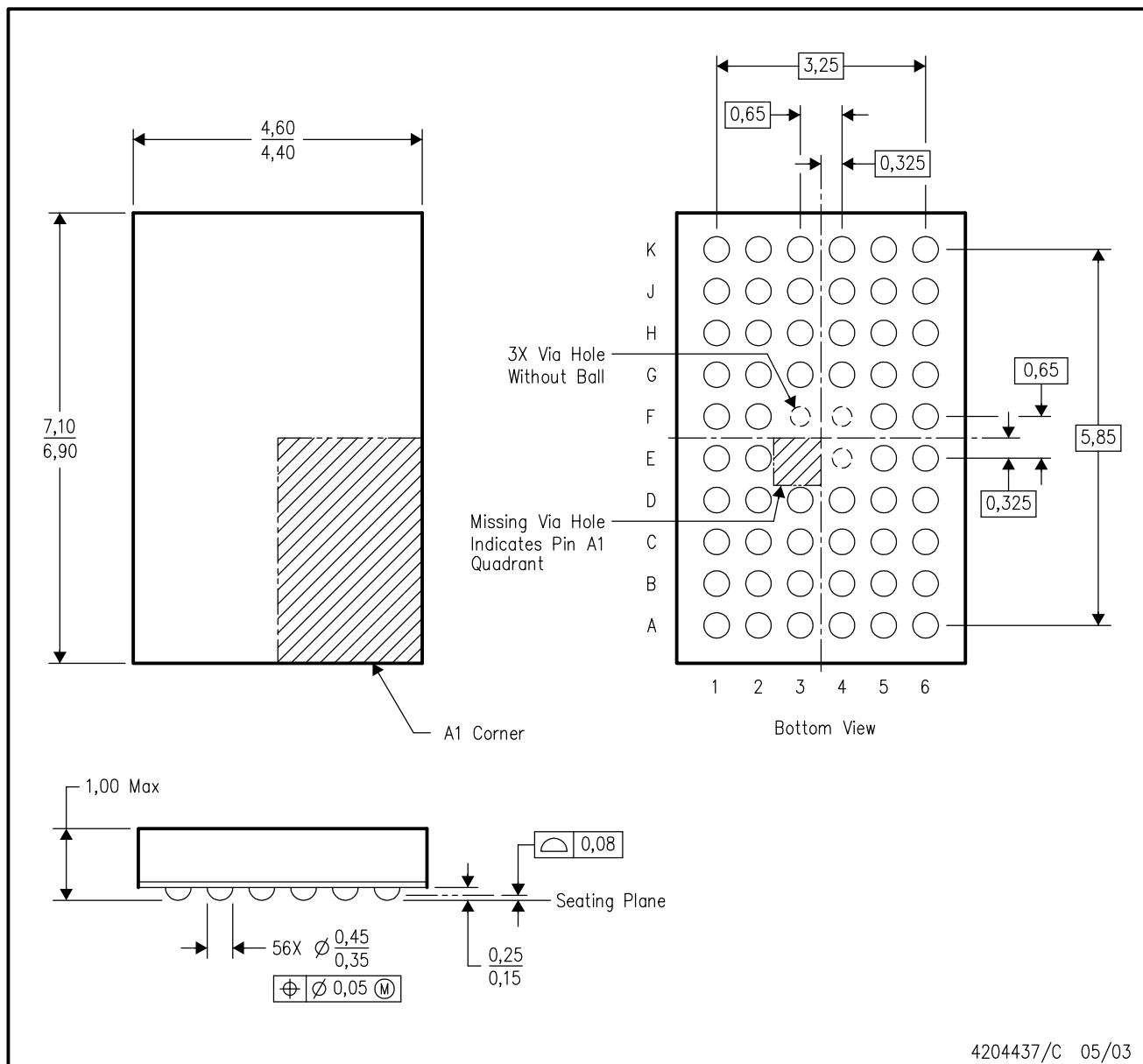
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

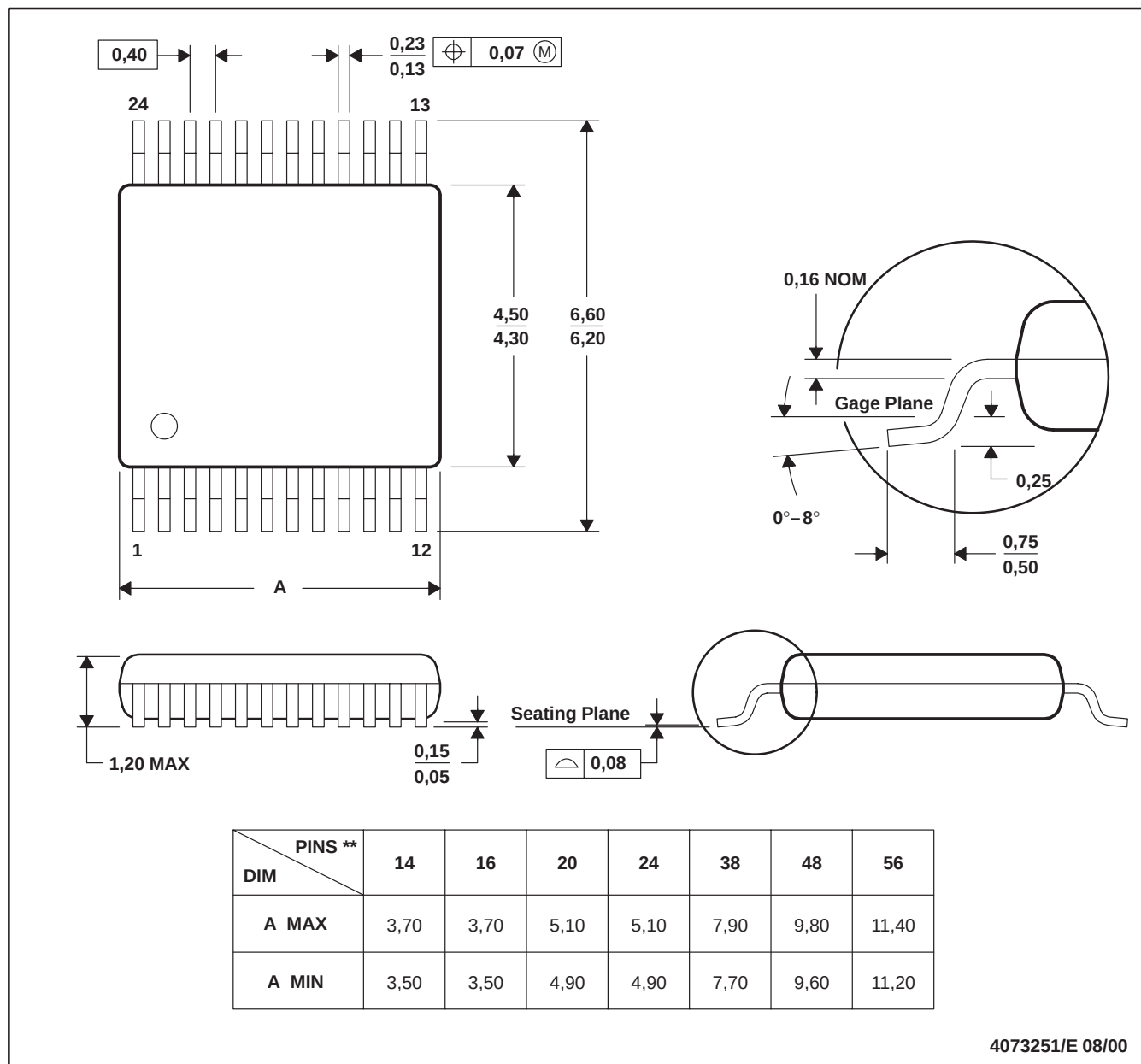


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - MicroStar Junior™ BGA configuration.
 - Falls within JEDEC MO-225 variation BA.
 - This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

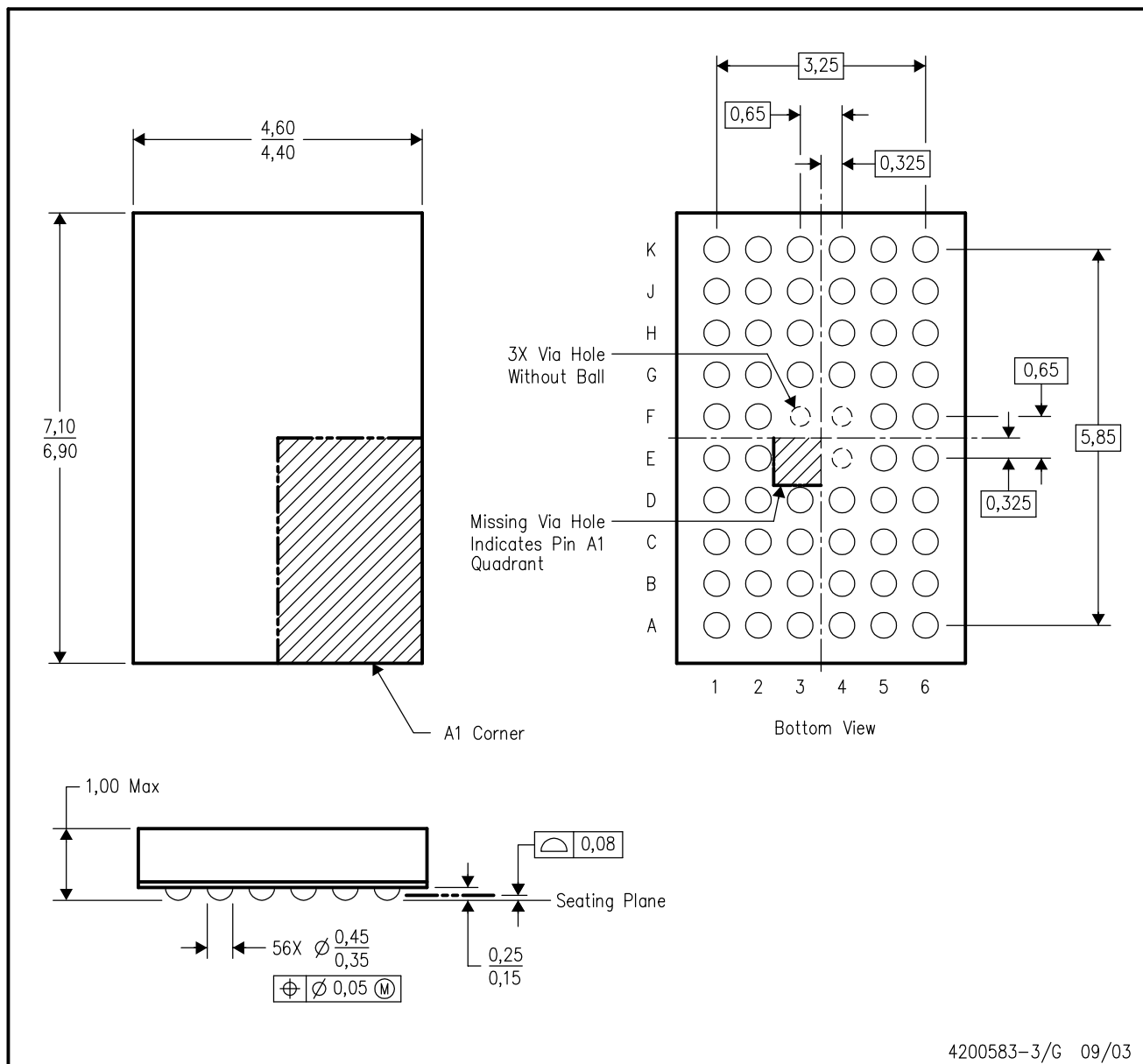
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



4200583-3/G 09/03

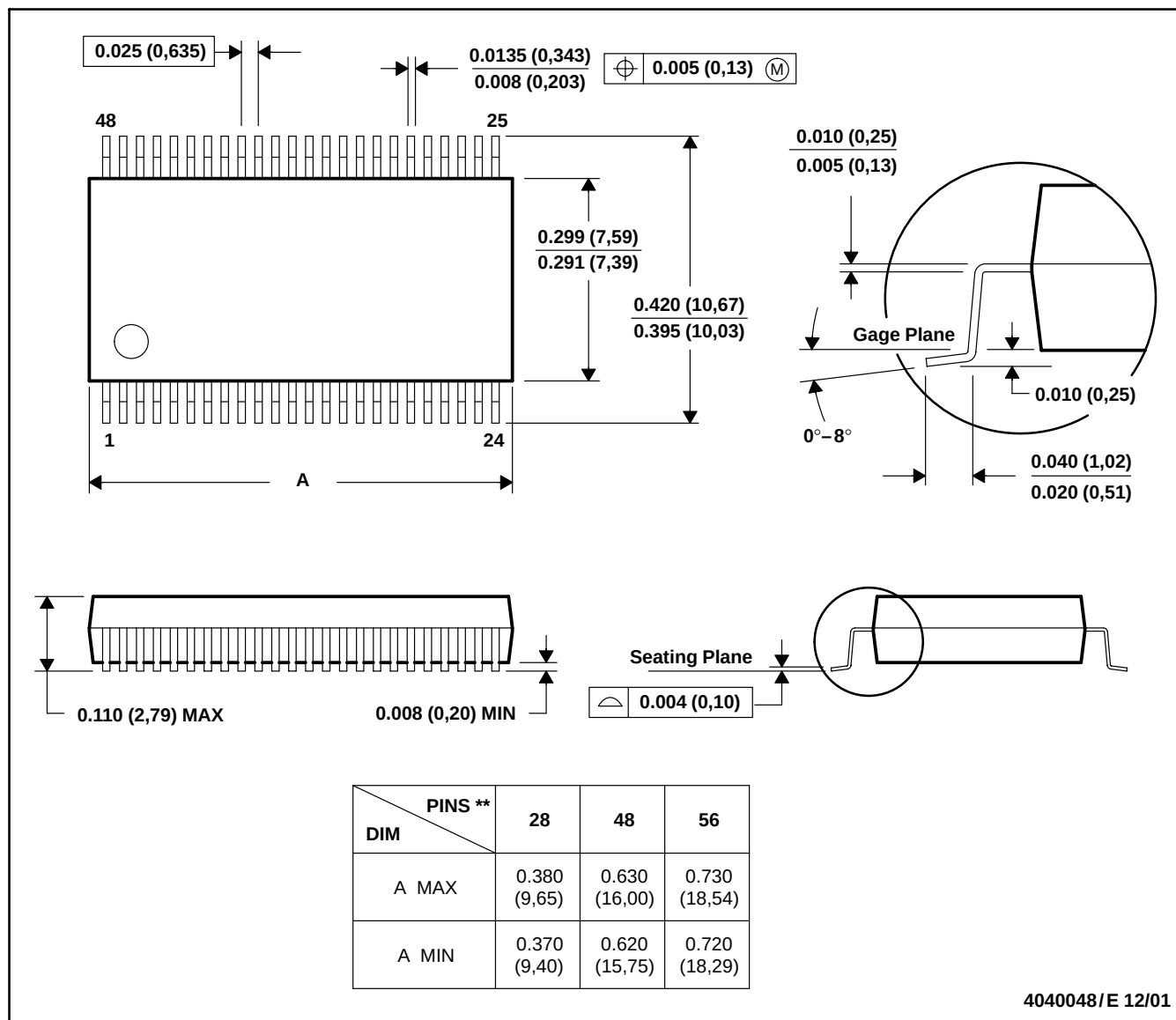
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ BGA configuration.
 - D. Falls within JEDEC MO-225 variation BA.
 - E. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

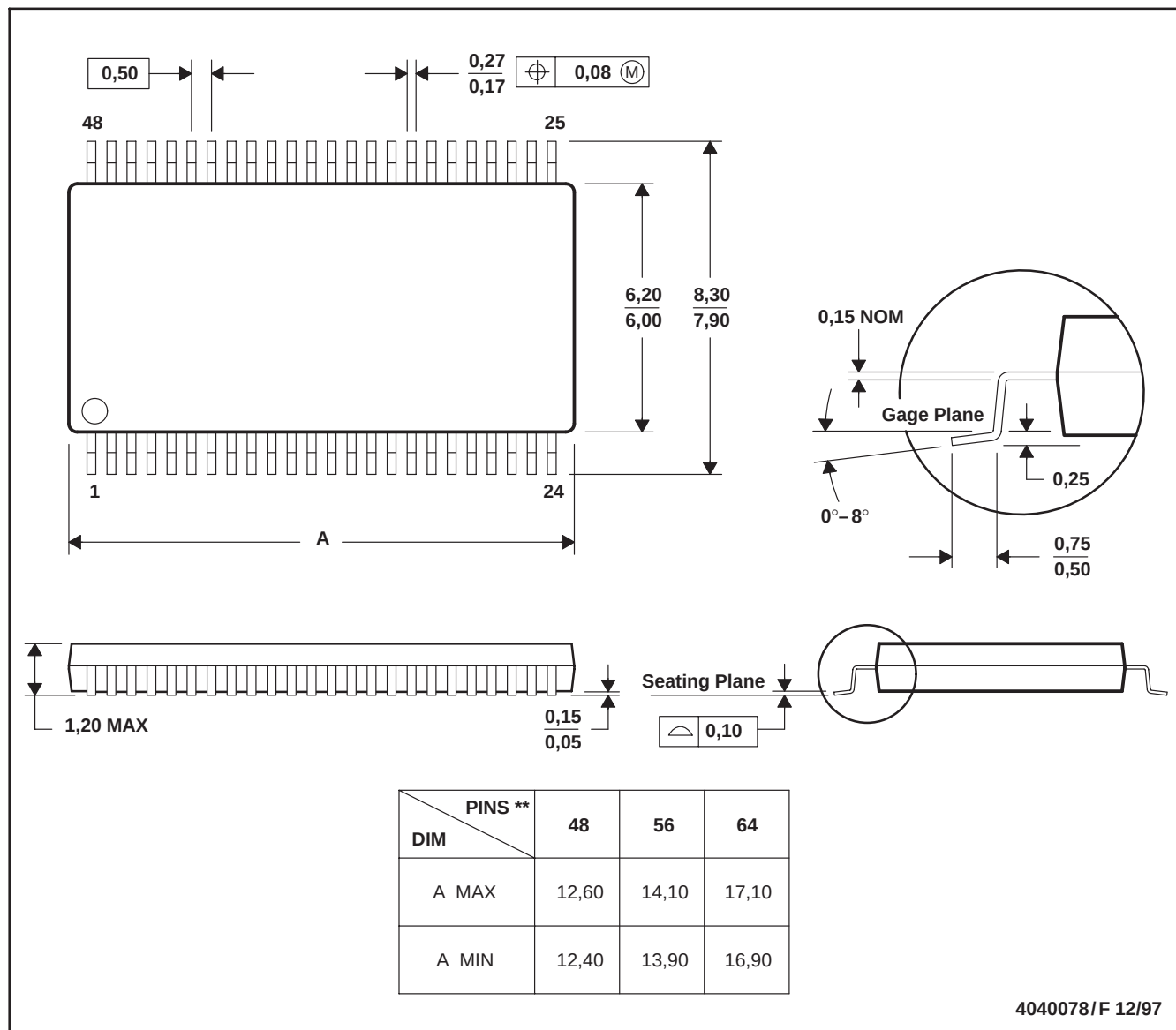


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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