

N-Channel NexFET™ Power MOSFET

Check for Samples: [CSD13201W10](#)

FEATURES

- Ultra Low Qg and Qgd
- Small Footprint 1mm x 1mm
- Low Profile 0.62mm Height
- Pb Free
- RoHS Compliant
- Halogen Free
- Gate-Source Voltage Clamp

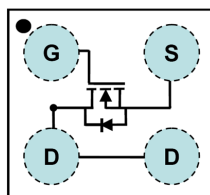
APPLICATIONS

- Battery Management
- Load Switch
- Battery Protection

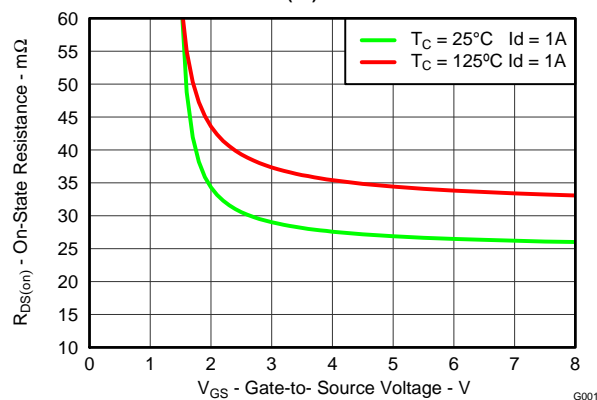
DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

Figure 1. Top View



$R_{DS(on)}$ vs V_{GS}



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	12	V
Q_g	Gate Charge Total (4.5V)	2.3	nC
Q_{gd}	Gate Charge Gate to Drain	0.3	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 1.8V$	38
		$V_{GS} = 2.5V$	29
		$V_{GS} = 4.5V$	26
$V_{GS(th)}$	Threshold Voltage	0.8	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD13201W10	1 x 1 Wafer Level Package	7-inch reel	3000	Tape and Reel

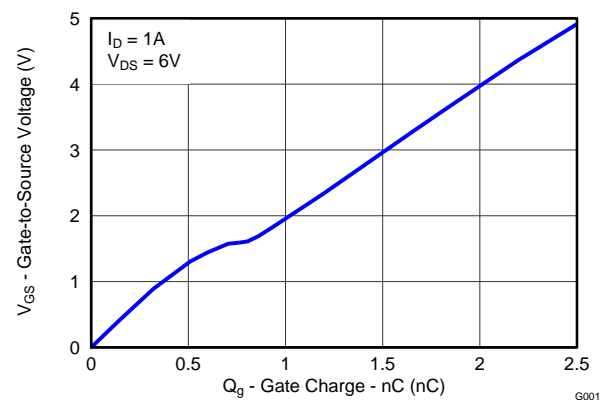
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	12	V
V_{GS}	Gate to Source Voltage	± 8	V
I_D	Continuous Drain Current, $T_A = 25^\circ\text{C}^{(1)}$	1.6	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}^{(2)}$	20.2	A
P_D	Power Dissipation ⁽¹⁾	1.2	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

(1) $R_{\theta JA} = 105^\circ\text{C/W}$ on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$

GATE CHARGE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

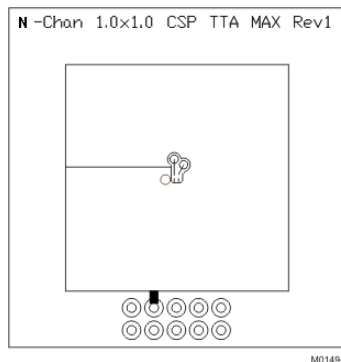
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Static Characteristics							
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	12			V	
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 9.6V	1			μA	
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = 8V	100			nA	
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	0.65	0.8	1.1	V	
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 1.8V, I _D = 1A	38			mΩ	
		V _{GS} = 2.5V, I _D = 1A	29				
		V _{GS} = 4.5V, I _D = 1A	26			34	mΩ
g _{fs} Transconductance		V _{DS} = 6V, I _D = 1A	23			S	
Dynamic Characteristics							
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = 6V, f = 1MHz	385			462	pF
C _{OSS}	Output Capacitance		245			294	pF
C _{RSS}	Reverse Transfer Capacitance		18.1			22.6	pF
R _g	Series Gate Resistance	V _{DS} = 6V, I _D = 1A	3			Ω	
Q _g	Gate Charge Total (4.5V)		2.3			2.9	nC
Q _{gd}	Gate Charge Gate to Drain		0.3			nC	
Q _{gs}	Gate Charge Gate to Source		0.5			nC	
Q _{g(th)}	Gate Charge at V _{th}		0.3			nC	
Q _{OSS}	Output Charge	V _{DS} = 6.0V, V _{GS} = 0V	1.8			nC	
t _{d(on)}	Turn On Delay Time	V _{DS} = 6V, V _{GS} = 4.5V, I _D = 1A R _G = 20Ω	3.9			ns	
t _r	Rise Time		5.9			ns	
t _{d(off)}	Turn Off Delay Time		14.4			ns	
t _f	Fall Time		9.7			ns	
Diode Characteristics							
V _{SD}	Diode Forward Voltage	I _S = 1A, V _{GS} = 0V	0.7			1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 6V, I _S = 1A, di/dt = 100A/μs	2.4			nC	
t _{rr}	Reverse Recovery Time		11.5			ns	

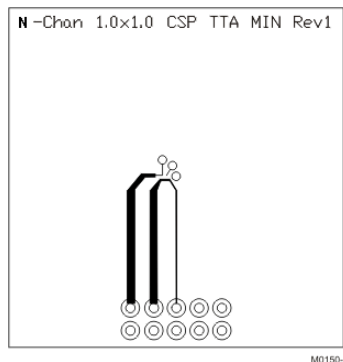
THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Minimum Cu area)			228.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (1 in ² Cu area)			131.1	$^\circ\text{C/W}$



Max $R_{\theta JA} = 131.1^{\circ}\text{C/W}$
when mounted on
1inch² of 2 oz. Cu.



Max $R_{\theta JA} = 228.6^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

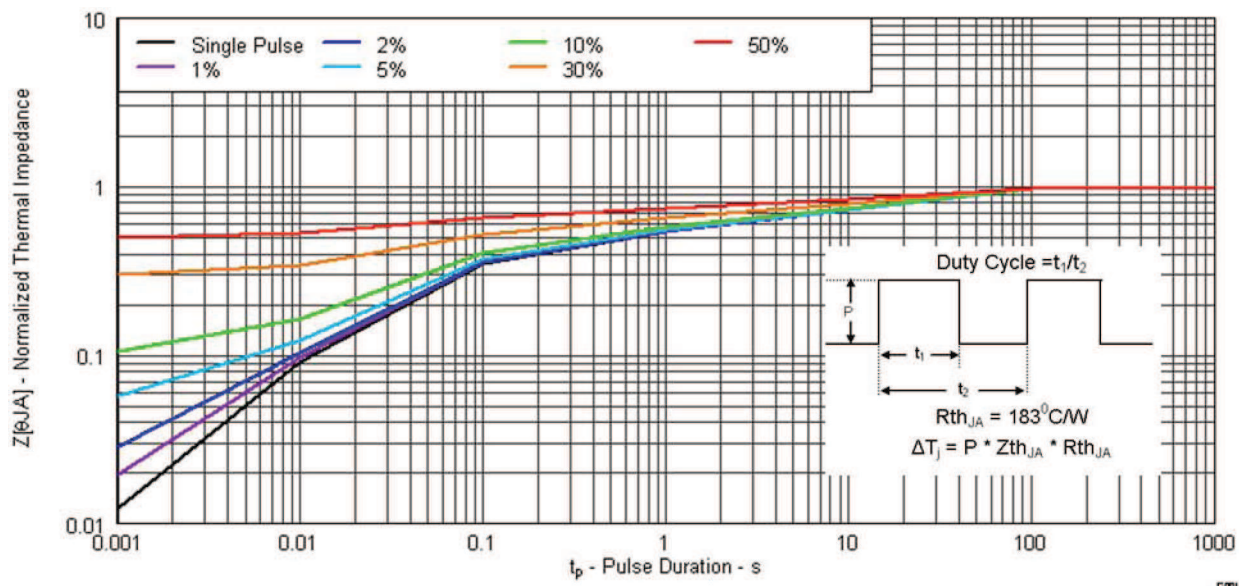


Figure 2. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

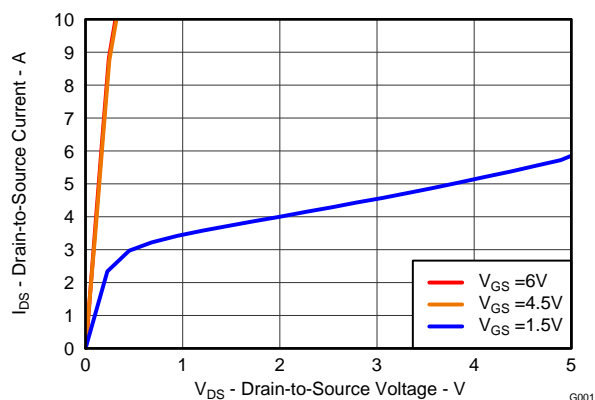


Figure 3. Saturation Characteristics

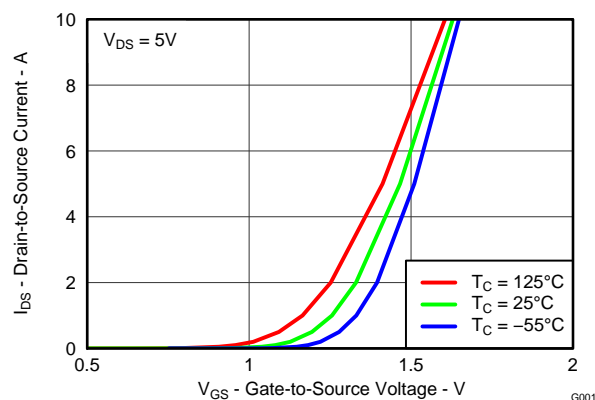


Figure 4. Transfer Characteristics

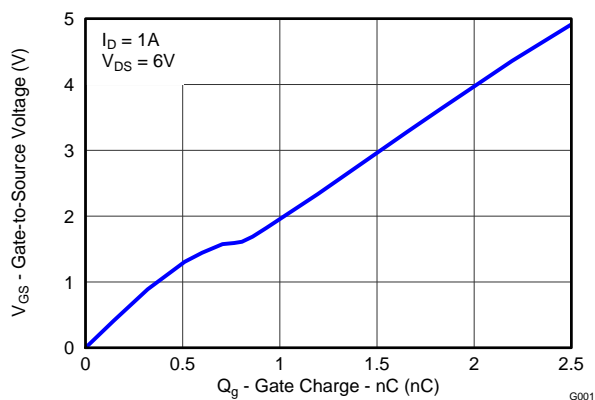


Figure 5. Gate Charge

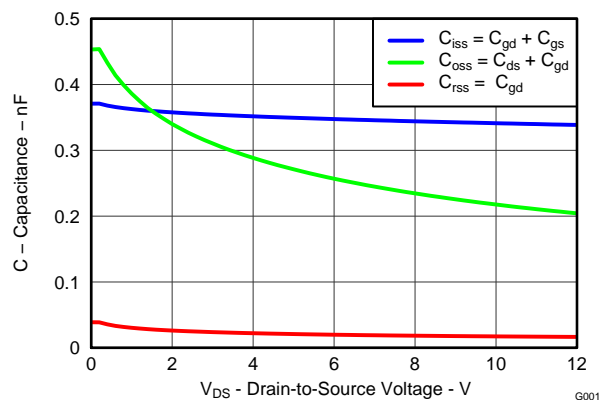


Figure 6. Capacitance

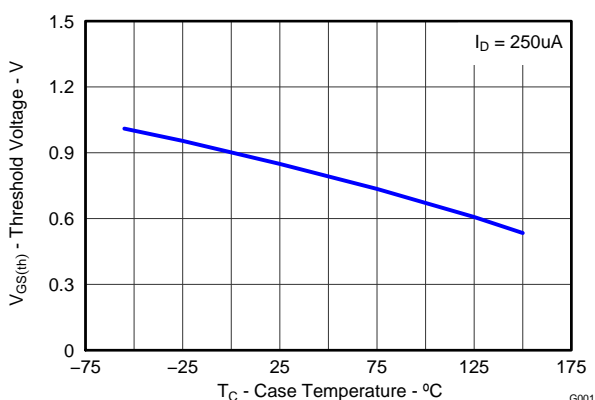


Figure 7. Threshold Voltage vs. Temperature

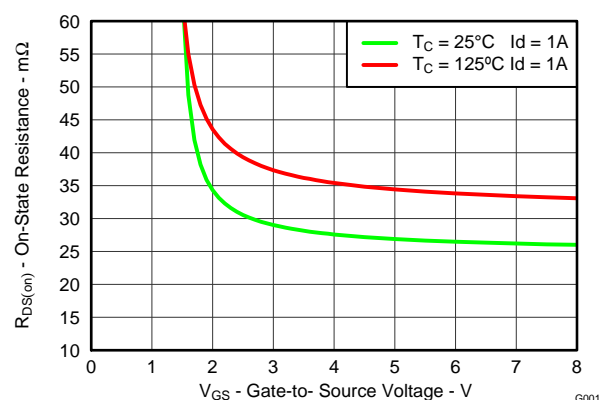


Figure 8. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

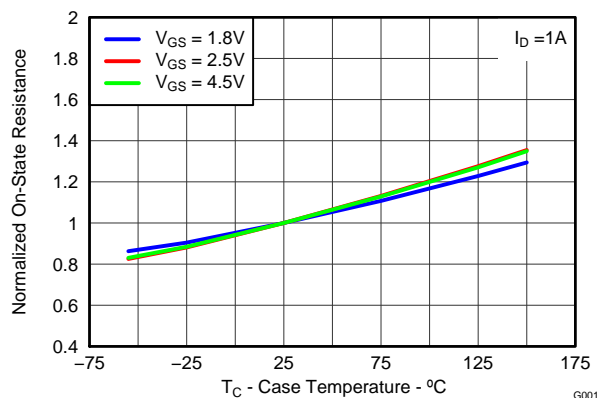


Figure 9. On Resistance vs. Temperature

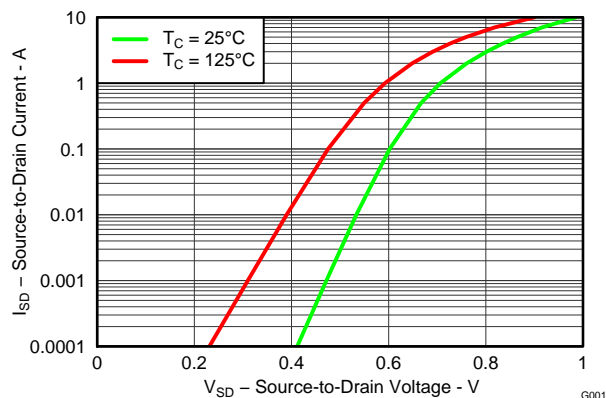


Figure 10. Typical Diode Forward Voltage

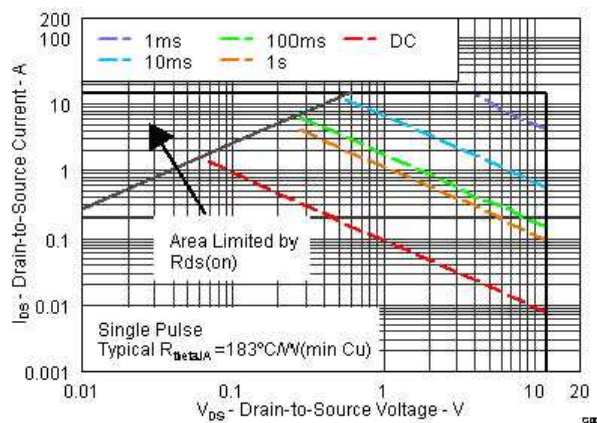


Figure 11. Maximum Safe Operating Area

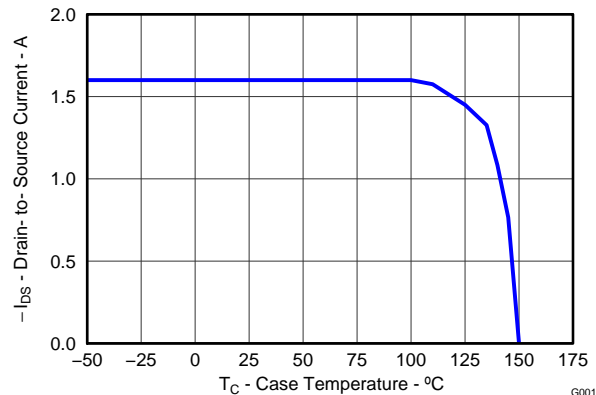
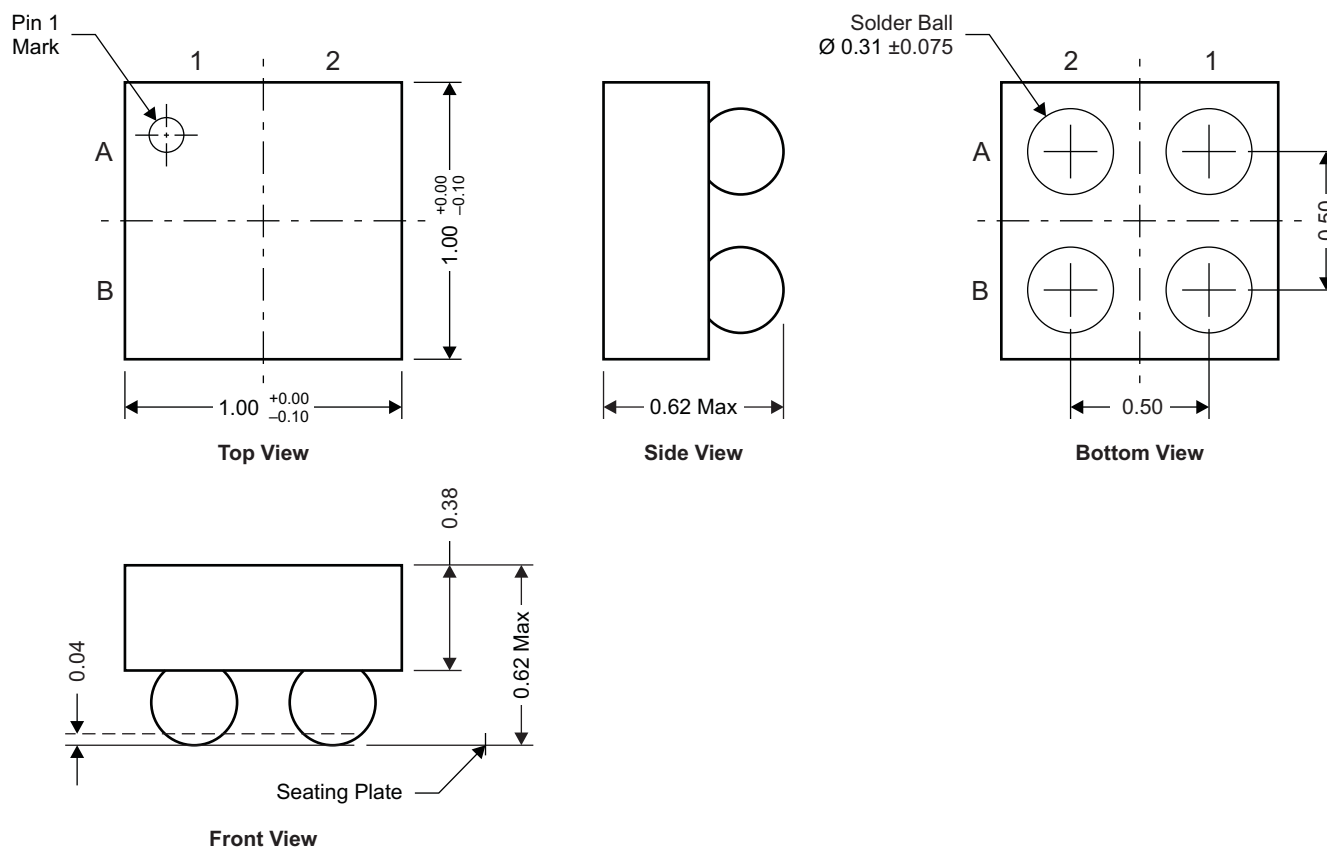


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD13201W10 Package Dimensions



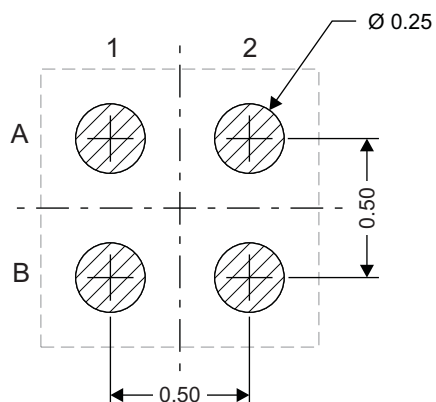
M0151-01

NOTE: All dimensions are in mm (unless otherwise specified)

Pin Configuration Table

POSITION	DESIGNATION
A2	Source
A1	Gate
B1, B2	Drain

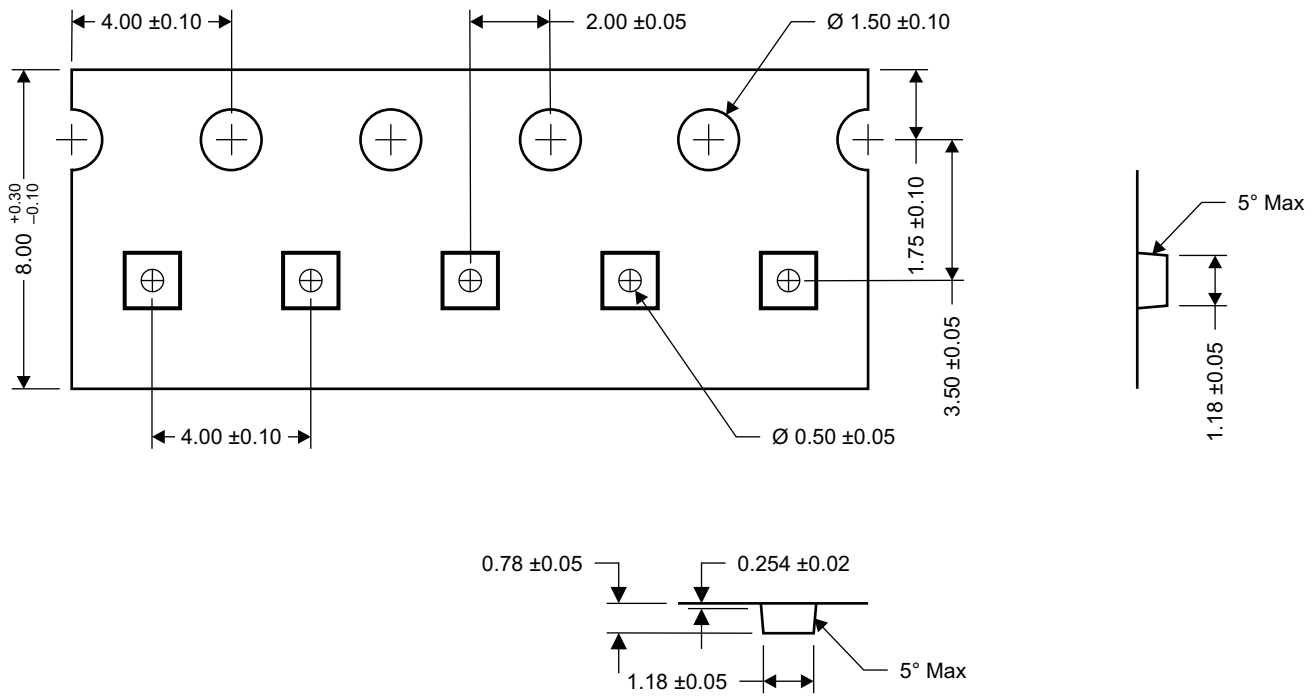
Land Pattern Recommendation



M0152-01

NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified)

M0153-01

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13201W10	ACTIVE	DSBGA	YZB	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-55 to 150	201	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13201W10	DSBGA	YZB	4	3000	180.0	8.4	1.06	1.06	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

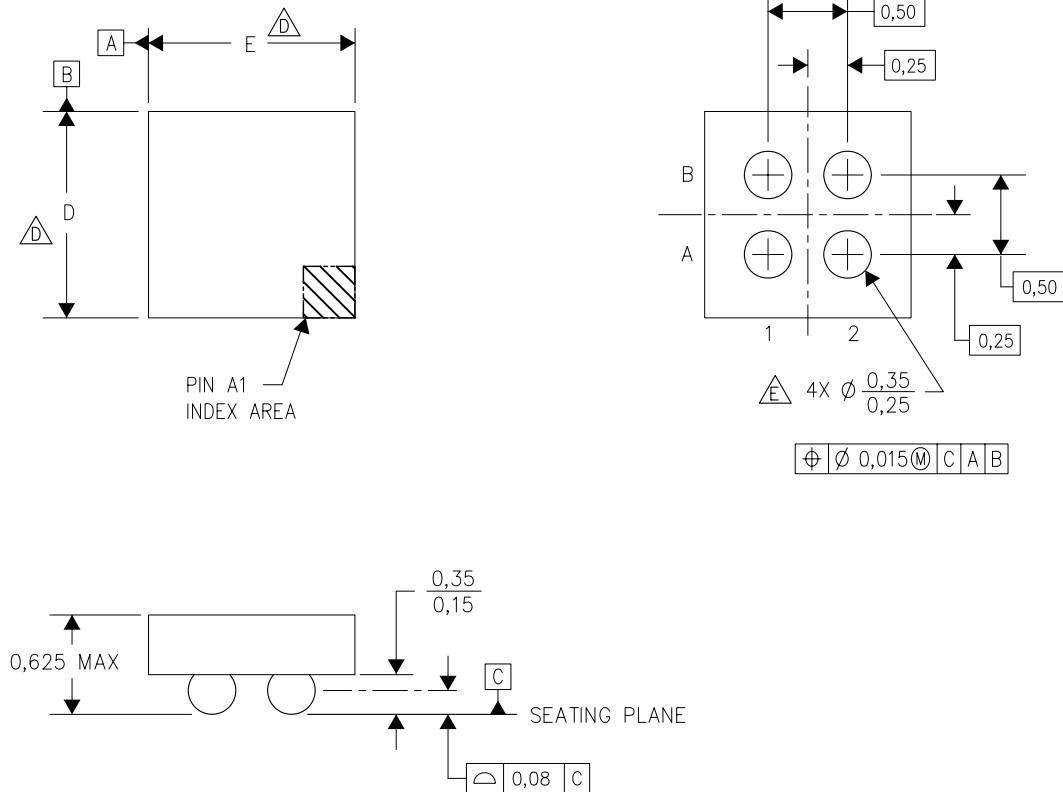


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13201W10	DSBGA	YZB	4	3000	182.0	182.0	17.0


YZB (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



4205055/D 07/08

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
-  D. Devices in YZB package can have dimension D ranging from 0.94 to 1.65 mm and dimension E ranging from 0.94 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
- E. Reference Product Data Sheet for array population.
2 x 2 matrix pattern is shown for illustration only.
- F. This package contains lead-free balls.
Refer to YEB (Drawing #4204178) for tin-lead (SnPb) balls.

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