1.8-V HIGH-SPEED DIFFERENTIAL LINE RECEIVER

Check for Samples: SN65LVDS4

FEATURES

- **Designed for Signaling Rates up to:**
  - **500-Mbps Receiver**

The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second)

- **Operates From a 1.8-V or 2.5-V Core Supply**
- **Available in 1.5-mm × 2-mm QFN Package**
- **Bus-Terminal ESD Exceeds 2 kV (HBM)**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV Into a 100-Ω Load**
- **Propagation Delay Times**
  - **2.1 ns Typical Receiver**
- **Power Dissipation at 250 MHz**
  - **40 mW Typical**
- **Requires External Failsafe**
- **Differential Input Voltage Threshold Less Than 50 mV**
- **Can Provide Output Voltage Logic Level (3.3-V LVTTL, 2.5-V LVCMOS, 1.8-V LVCMOS) Based on External VDD Pin, Thus Eliminating External Level Translation**

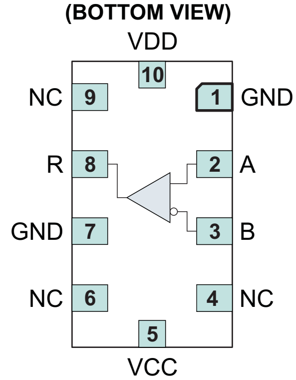
APPLICATIONS

- **Clock Distribution**
- **Wireless Base Stations**
- **Newtwork Routers**

DESCRIPTION

The SN65LVDS4 is a single, low-voltage, differential line receiver in a small-outline QFN package.

SN65LVDS4 (Receiver)
LVDS4 in QFN Package
(BOTTOM VIEW)



SN65LVDS4 (Receiver)
LVDS4 in QFN Package
(TOP VIEW)

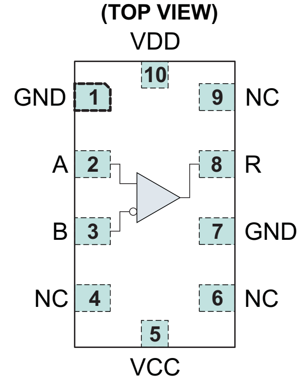


Table 1. Pin Description Table

PIN NAME	PIN NO.	I/O	DESCRIPTION
A	2	I	LVDS input, positive
B	3	I	LVDS input, negative
GND	1, 7	–	Ground
NC	4, 6, 9	–	No connect
R	8	O	1.8/2.5 LVCMOS/3.3 LVTTL output
VCC	5	–	Core supply voltage
VDD	10	–	Output drive voltage

AVAILABLE OPTIONS

PART NUMBER	INTEGRATED TERMINATION	PACKAGE	PACKAGE MARKING
SN65LVDS4RSE	No	QFN	QXB

The SN65LVDS4 is characterized for operation from –40°C to 85°C.

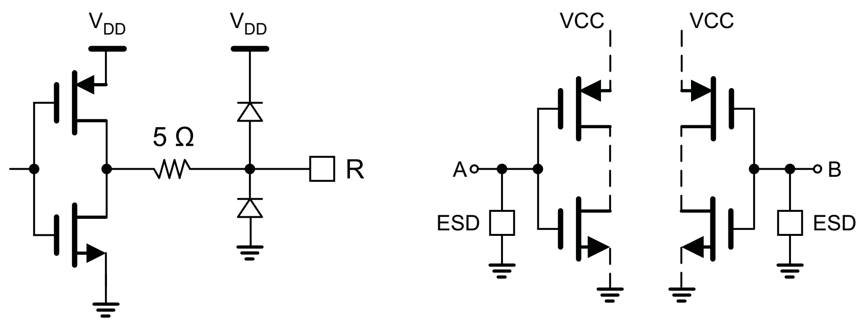
Table 2. FUNCTION TABLE

INPUTS	OUTPUT(1)
$V_{ID} = V_A – V_B$	R
$V_{ID} \geq 50$ mV	H
$V_{ID} \leq –50$ mV	L

(1) H = high level, L = low level, ? = indeterminate

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

RECEIVER EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[(1)]

PARAMETER		Values MIN	Values MAX	Units
Supply voltage range, V_{CC} [(2)]		–0.5	4	V
Receiver output voltage logic level and driver input voltage logic level supply, V_{DD}		–0.5	4	V
Input voltage range, V_I	(A or B)	–0.5	V_{CC} + 0.3	V
Output voltage, V_O	(R)	–0.5	V_{DD} + 0.3	V
Differential input voltage magnitude, $\|V_{ID}\|$			1 V	
Receiver output current, I_O		–12	12	mA
Human-body model electrostatic discharge, HBM ESD[(3)]				
	All pins		2000	V
	Bus pins (A, B, Y, Z)		2000	V
Field-induced-charge device model electrostatic discharge, FCDM ESD[(4)]			500	V
Continuous total power dissipation, P_D		See the Thermal Information Table		
Storage Temperature Range (non operating)		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Test method based upon JEDEC Standard 22, Test Method A114-A. Bus pins stressed with respect to GND and V_{CC} separately.
(4) Test method based upon EIA-JEDEC JESD22-C101C.

THERMAL INFORMATION

THERMAL METRIC (1)		SN65LVDS4 RSE 10 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance (2)	171.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance (3)	60.7	°C/W
θ_{JB}	Junction-to-board thermal resistance (4)	71.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter (5)	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter (6)	64.7	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance (7)	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{CC1.8}$	Core supply voltage		1.62	1.8	1.98	V
$V_{CC2.5}$	Core supply voltage		2.25	2.5	2.75	V
$V_{DD1.8}$	Output drive voltage		1.62	1.8	1.98	V
$V_{DD2.5}$	Output drive voltage		2.25	2.5	2.75	V
$V_{DD3.3}$	Output drive voltage		3	3.3	3.6	V
T_A	Operating free-air temperature		–40		85	°C
$\|V_{ID}\|$	Magnitude of differential input voltage		0.15		0.6	V
f_{op}	Operating frequency range		10		250	MHz
$\|VIN_{MAX}\|$	Input voltage (any combination of input or common-mode voltage) (1) See VIN_{MAX}.		0		V_{CC}	V

(1) Any combination of input or common-mode voltage should not be below 0 V or above V_{CC}.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions, V_{CC} = 2.5 V, V_{ID} = 150 mV–600 mV, V_{CM} = V_{ID}/2 to V_{CC} – V_{ID}/2 V, 10 pF load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 1, $V_{CC1.8}$, $V_{CC2.5}$			50	mV
$V_{ITH–}$	Negative-going differential input voltage threshold		–50			
V_{OH}	High-level output voltage	V_{DD} = 3.3V, I_{OH} = –8 mA	V_{DD} – 0.25			V
		V_{DD} = 2.5V, I_{OH} = –6 mA	V_{DD} – 0.25			
		V_{DD} = 1.8 V, I_{OH} = –4 mA	V_{DD} – 0.25			
V_{OL}	Low-level output voltage	V_{DD} = 3.3 V, I_{OL} = 8 mA			0.25	V
		V_{DD} = 2.5 V, I_{OL} = 6 mA			0.25	
		V_{DD} = 1.8 V, I_{OL} = 4 mA			0.25	
P_{static}	Static power	No load, steady state, V_{DD} = 3.3 V, V_{ID}+		22	28	mW
		No load, steady state, V_{DD} = 2.5 V, V_{ID}+		20	25	
C_I	Input capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		4		pF
C_O	Output capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		4		pF

(1) The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.
(2) All typical values are at 25°C .

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions, V_{CC} = 1.8 V, V_{ID} = 150 mV–600 mV, V_{CM} = V_{ID}/2 to V_{CC} – V_{ID}/2 V, 10 pF load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 1, $V_{CC1.8}$, $V_{CC2.5}$			50	mV
$V_{ITH–}$	Negative-going differential input voltage threshold		–50			
V_{OH}	High-level output voltage	V_{DD} = 3.3V, I_{OH} = –8 mA	V_{DD} – 0.25			V
		V_{DD} = 2.5V, I_{OH} = –6 mA	V_{DD} – 0.25			
		V_{DD} = 1.8 V, I_{OH} = –4 mA	V_{DD} – 0.25			
V_{OL}	Low-level output voltage	V_{DD} = 3.3 V, I_{OL} = 8 mA			0.25	V
		V_{DD} = 2.5 V, I_{OL} = 6 mA			0.25	
		V_{DD} = 1.8 V, I_{OL} = 4 mA			0.25	
P_{static}	Static power	No load, steady state, V_{DD} = 3.3 V, V_{ID}+		18	21	mW
		No load, steady state, V_{DD} = 2.5 V, V_{ID}+		16	19	
		No load, steady state, V_{DD} = 1.8 V, V_{ID}+		13	16	
C_I	Input capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		4		pF
C_O	Output capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		4		pF

(1) The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.
(2) All typical values are at 25°C .

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions, V_{CC} = 2.5 V, V_{ID} = 150 mV–600 mV, V_{CM} = V_{ID}/2 to V_{CC} – V_{ID}/2 V, 10 pF load (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[(1)]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 3			2.5	3.3	ns
t_{PHL}	Propagation delay time, high-to-low-level output				2.5	3.3	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)[(2)]					240	ps
t_r	Output signal rise time		V_{DD} = 3.3 V			550	ps
			V_{DD} = 2.5 V			600	
t_f	Output signal fall time		V_{DD} = 3.3 V			550	ps
			V_{DD} = 2.5 V			600	
t_{jit}	Residual jitter added	Carrier frequency = 122.8 MHz, input signal amplitude = 500 mVpp sine wave, integration bandwidth for rms jitter = 20 khz-20 MHz, VDD = 2.5 V			370		fs

(1) All typical values are at 25°C.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions, V_{CC} = 1.8 V, V_{ID} = 150 mV–600 mV, V_{CM} = V_{ID}/2 to V_{CC} – V_{ID}/2 V, 10 pF load (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[(1)]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 3			3.2	3.8	ns
t_{PHL}	Propagation delay time, high-to-low-level output				3.2	3.8	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)[(2)]					240	ps
t_r	Output signal rise time		V_{DD} = 3.3 V			550	ps
			V_{DD} = 2.5 V			600	
			V_{DD} = 1.8 V			750	
t_f	Output signal fall time		V_{DD} = 3.3 V			550	ps
			V_{DD} = 2.5 V			600	
			V_{DD} = 1.8 V			750	
t_{jit}	Residual jitter added	Carrier frequency = 122.8 MHz, input signal amplitude = 500 mVpp sine wave, integration bandwidth for rms jitter = 20 khz-20 MHz, VDD = 1.8 V			370		fs

(1) All typical values are at 25°C.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

PARAMETER MEASUREMENT INFORMATION

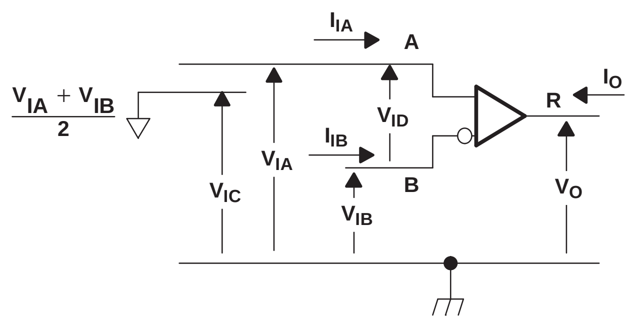


Figure 1. Receiver Voltage and Current Definitions

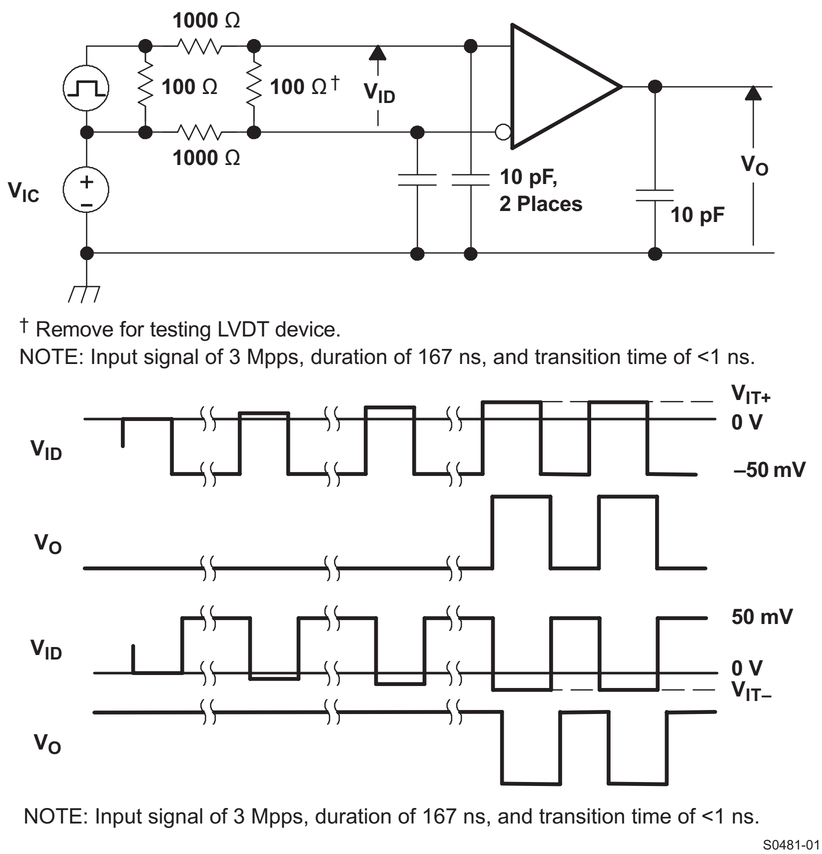
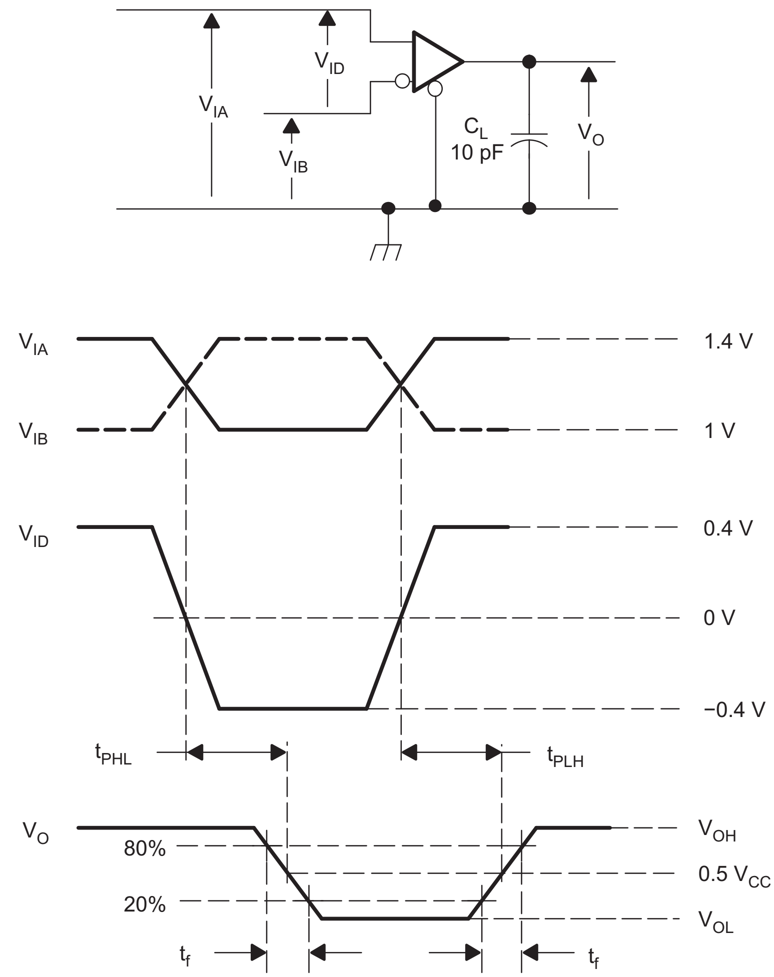


Figure 2. V_{IT+} and V_{IT-} Input Voltage Threshold Test Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 3. Receiver Timing Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

VICM = 1.2 V, VID = 300 mV, C_L = 10 pF, input rise time and fall time = 1 ns, input frequency = 250 MHz, 50% duty cycle, T_A = 25°C, unless otherwise noted

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

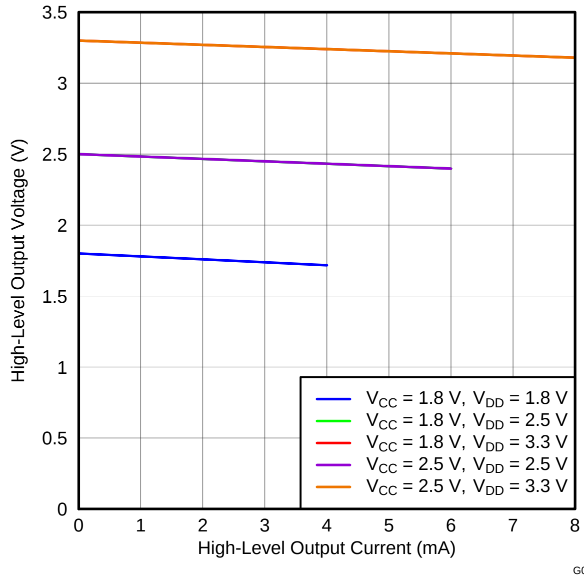


Figure 4.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

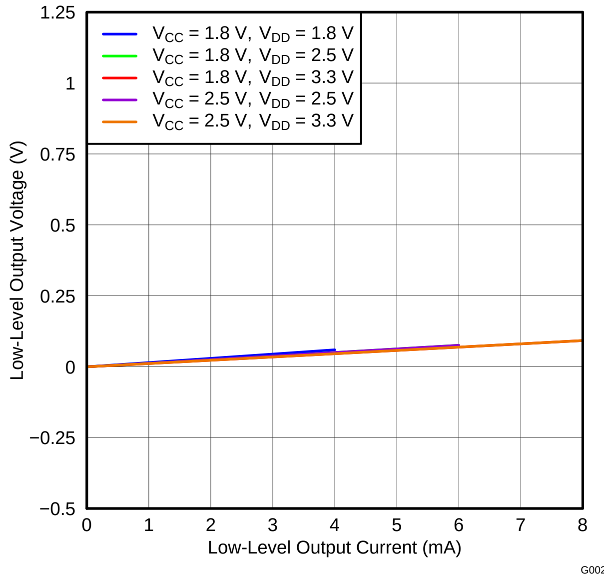


Figure 5.

HIGH- TO LOW-LEVEL PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

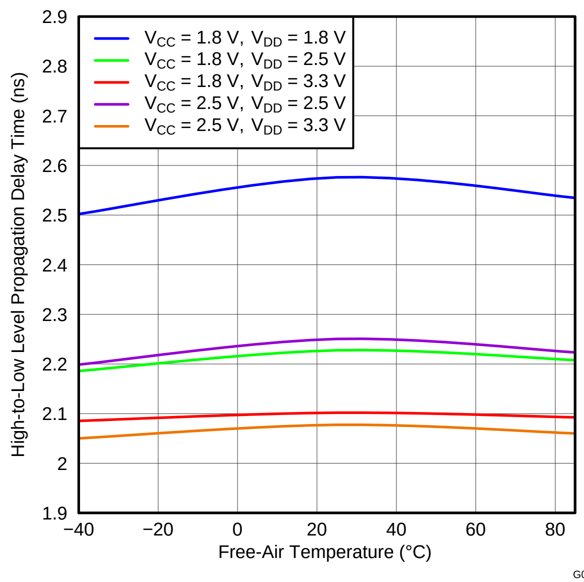


Figure 6.

LOW- TO HIGH-LEVEL PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

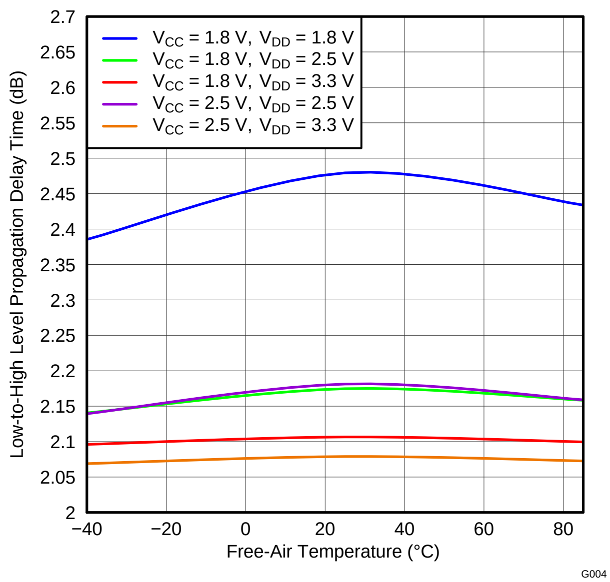


Figure 7.

TYPICAL CHARACTERISTICS (continued)

VICM = 1.2 V, VID = 300 mV, C_L = 10 pF, input rise time and fall time = 1 ns, input frequency = 250 MHz, 50% duty cycle, T_A = 25°C, unless otherwise noted

RISE TIME vs CAPACITIVE LOAD

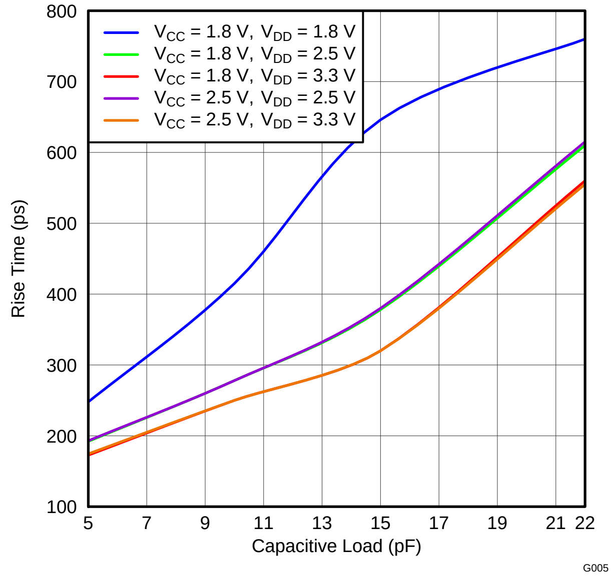


Figure 8.

FALL TIME vs CAPACITIVE LOAD

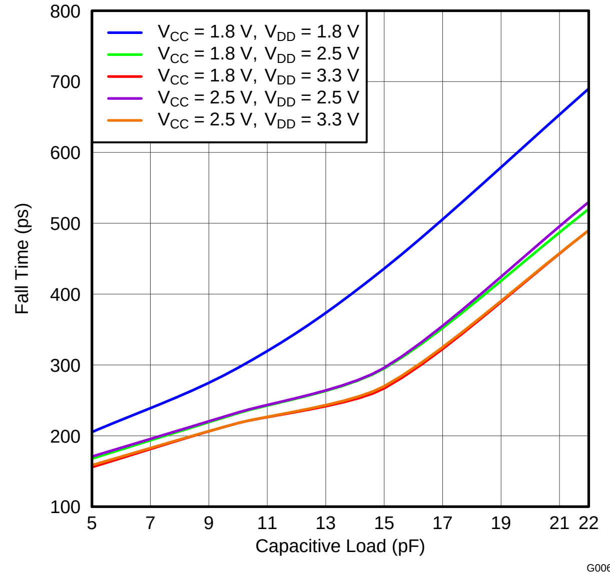


Figure 9.

SUPPLY CURRENT vs FREQUENCY

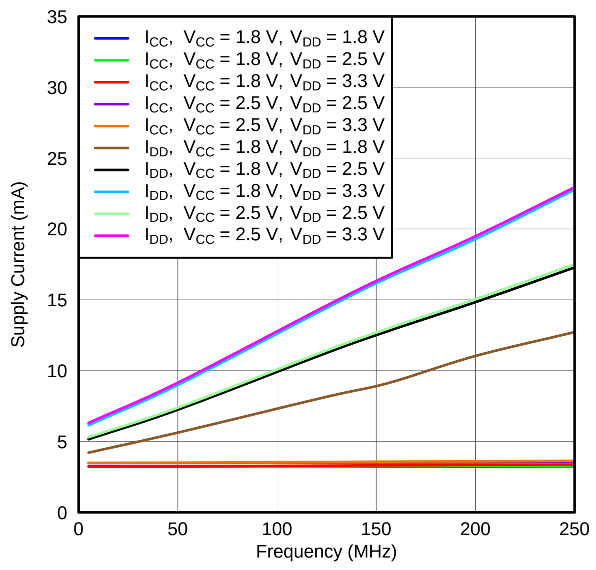


Figure 10.

SUPPLY CURRENT vs TEMPERATURE

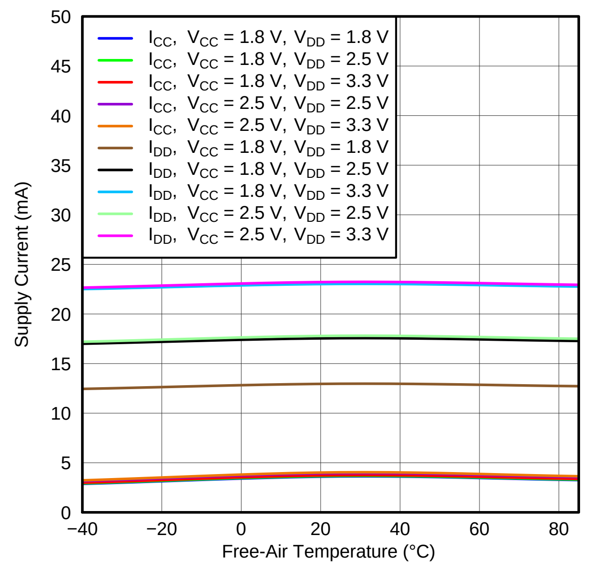


Figure 11.

TYPICAL CHARACTERISTICS (continued)

VICM = 1.2 V, VID = 300 mV, C_L = 10 pF, input rise time and fall time = 1 ns, input frequency = 250 MHz, 50% duty cycle, T_A = 25°C, unless otherwise noted

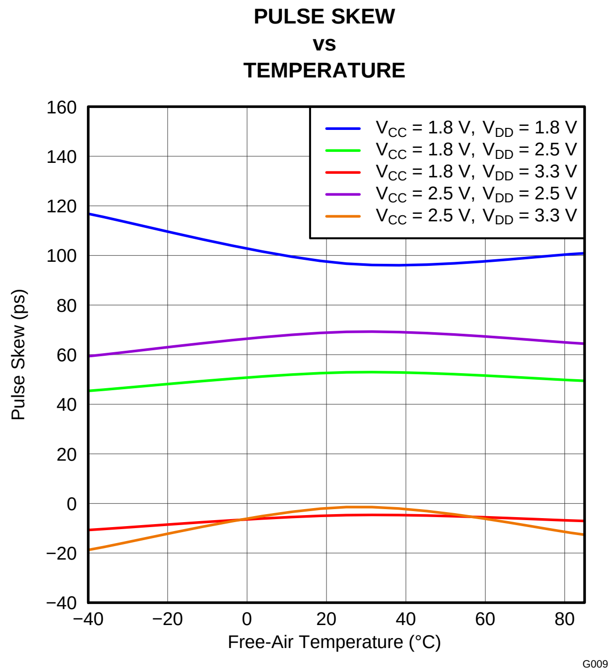


Figure 12.

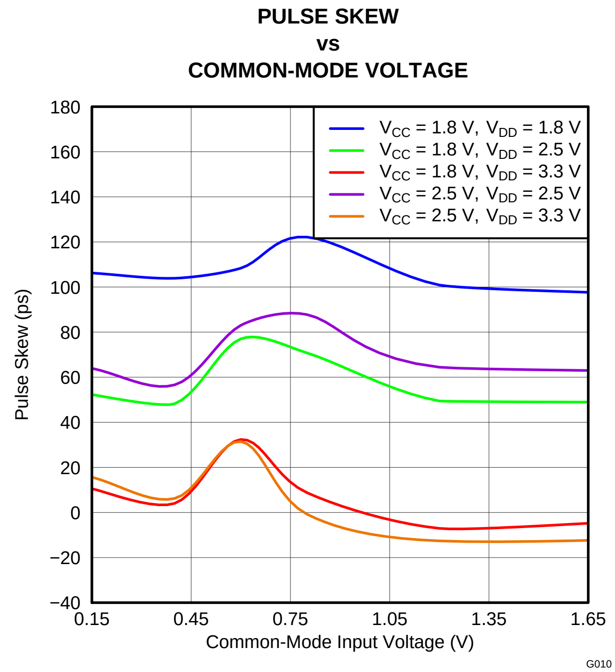


Figure 13.

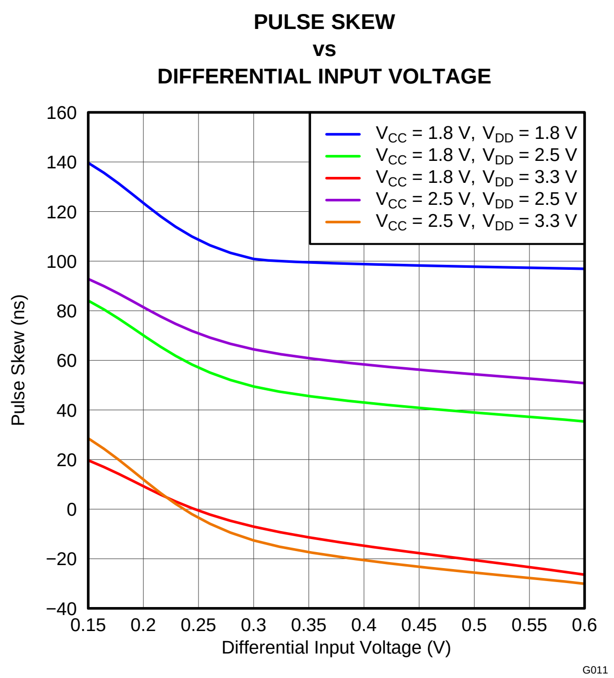


Figure 14.

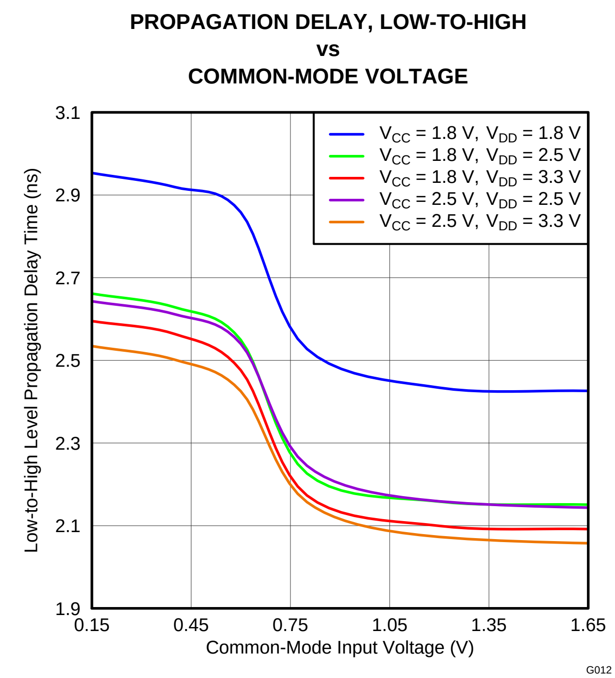


Figure 15.

TYPICAL CHARACTERISTICS (continued)

VICM = 1.2 V, VID = 300 mV, C_L = 10 pF, input rise time and fall time = 1 ns, input frequency = 250 MHz, 50% duty cycle, T_A = 25°C, unless otherwise noted

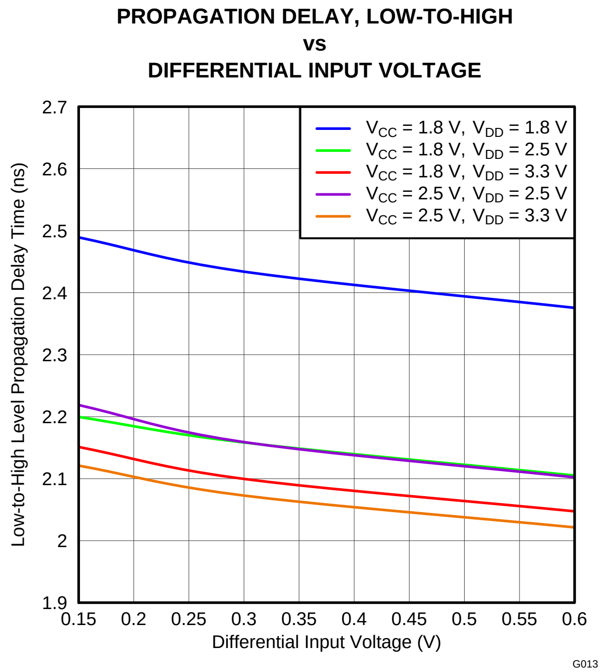


Figure 16.

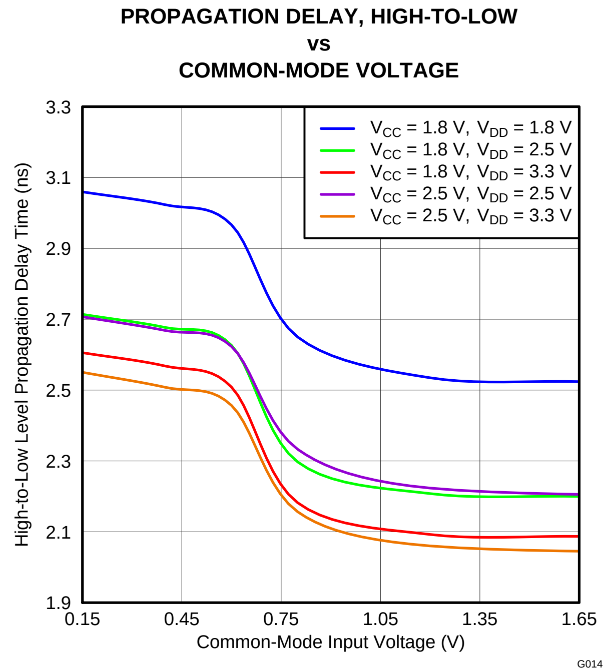


Figure 17.

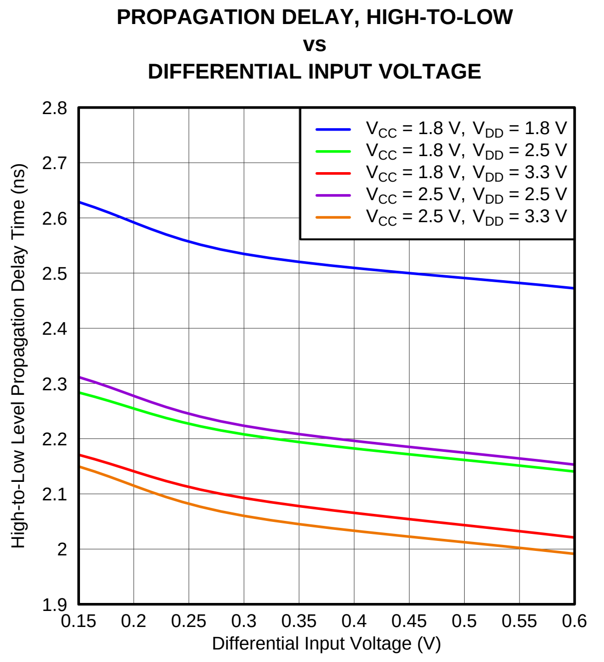


Figure 18.

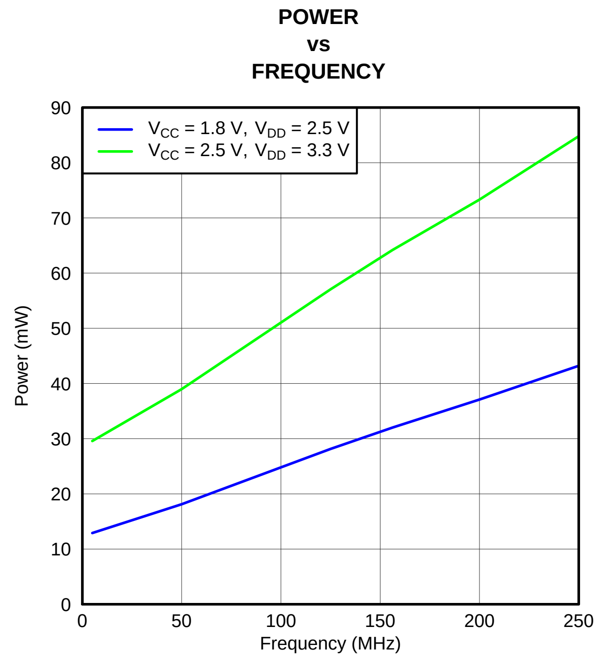
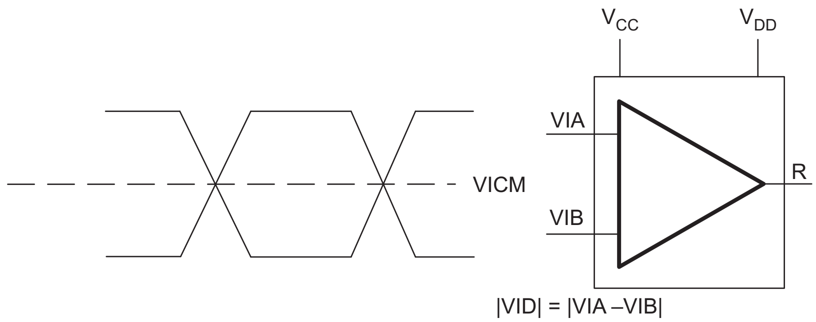


Figure 19.

APPLICATION INFORMATION

VIN_{MAX}



$V_{CC2.5}$ (Note: Worst-Case VCC = 2.5 – 10% = 2.25 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.25	1.2	50	1.225
1.2	1.25	50	1.225
2.2	**2.25**	50	2.225
2.25	2.2	50	2.225
0.05	0	50	0.025
0	0.05	50	0.025

$V_{CC2.5}$ (Note: Worst-Case VCC = 2.5 – 10% = 2.25 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.5	0.9	600	1.2
0.9	1.5	600	1.2
1.65	**2.25**	600	1.95
2.25	1.65	600	1.95
0.6	0	600	0.3
0	0.6	600	0.3

$V_{CC1.8}$ (Note: Worst-Case VCC = 1.8 – 10% =1.62 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.25	1.2	50	1.225
1.2	1.25	50	1.225
1.57	**1.62**	50	1.595
1.62	1.57	50	1.595
0.05	0	50	0.025
0	0.05	50	0.025

$V_{CC1.8}$ (Note: Worst-Case VCC = 1.8 – 10% =1.62 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.5	0.9	600	1.2
0.9	1.5	600	1.2
1.02	**1.62**	600	1.32
1.62	1.02	600	1.32
0.6	0	600	0.3
0	0.6	600	0.3

Figure 20. Maximum Input Voltage Combination Allowed

POWER SUPPLY

There are two power supplies in SN65LVDS4, VCC which is the core power supply and VDD which is the output drive power supply. For proper device operation it is recommended that VCC should be powered up first and then VDD or VCC applied at the same time as VDD (VCC and VDD tied together). It is also recommended that VCC should be equal to or less than VDD as shown in Table 3.

Table 3. Power Supply Acceptable Combinations

VCC (V)	VDD (V)	Recommended
1.8	1.8	yes
1.8	2.5	yes
1.8	3.3	yes
2.5	1.8	no
2.5	2.5	yes
2.5	3.3	yes

FAILSAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –50 mV and 50 mV and within its recommended input common-mode voltage range.

Open circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, it is recommended to have an external failsafe solution as shown in Figure 21. In the external failsafe solution, the A side is pulled to V_{CC} via a weak pullup resistor and the B side is pulled down via a weak pulldown resistor. This creates a voltage offset and prevents the receiver from switching based on noise.

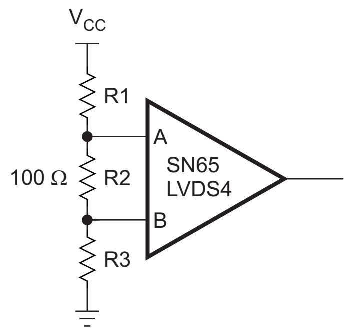


Figure 21. Open-Circuit Failsafe of the LVDS Receiver

R1 and R3 Calculation With VCC = 1.8 V

Assume that an external failsafe bias of 25 mV is desired

Bias current in this case is = 25 mV/100 Ω = 250 µA

Next, determine the total resistance from VCC to ground = 1.8 V/250 µA = 7.2 kΩ

Keeping the common mode bias of 1.25 V to the receiver, the value of R3 = 1.25 V/250 µA = 5 kΩ

Thus, R1 = 2.2 kΩ

R1 and R3 Calculation With VCC = 2.5 V

Assume that an external failsafe bias of 25 mV is desired

Bias current in this case is = 25 mV/100 Ω = 250 µA

Next, determine the total resistance from VCC to ground = 2.5 V/250 µA = 10 kΩ

Keeping the common mode bias of 1.25 V to the receiver, the value of R3 = 1.25 V/250 µA = 5 kΩ

Thus, R1 = 5 kΩ

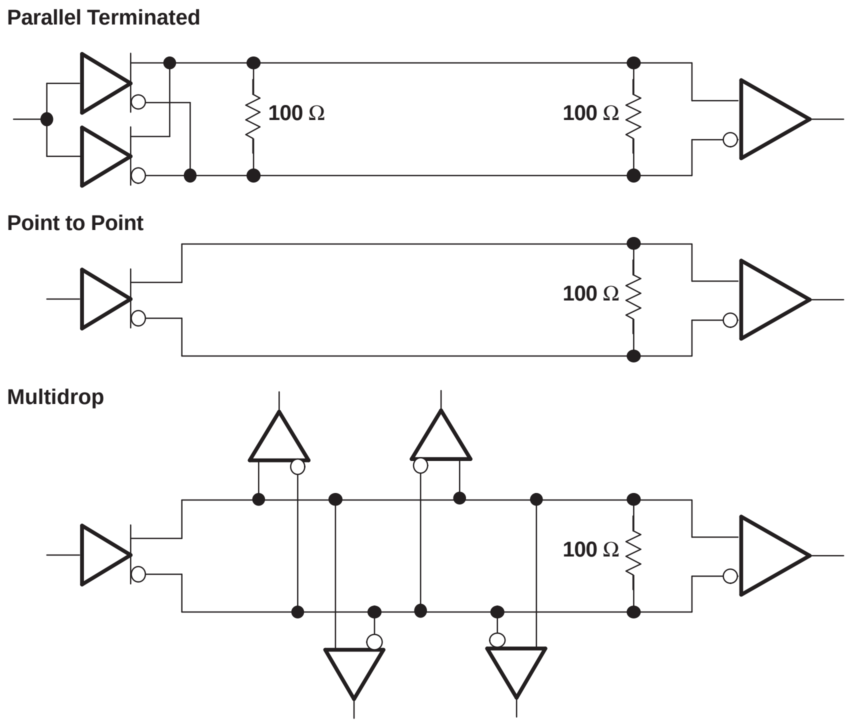


Figure 22. Typical Application Circuits

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65LVDS4RSER	ACTIVE	UQFN	RSE	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVDS4RSET	ACTIVE	UQFN	RSE	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

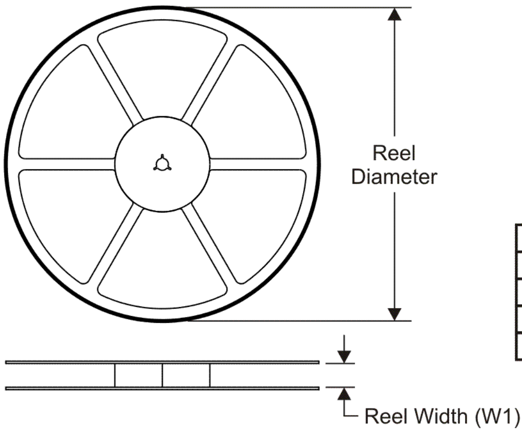
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

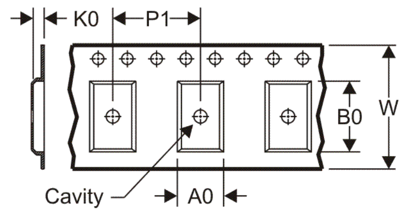
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

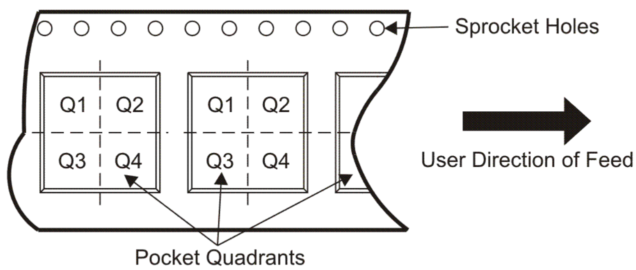


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

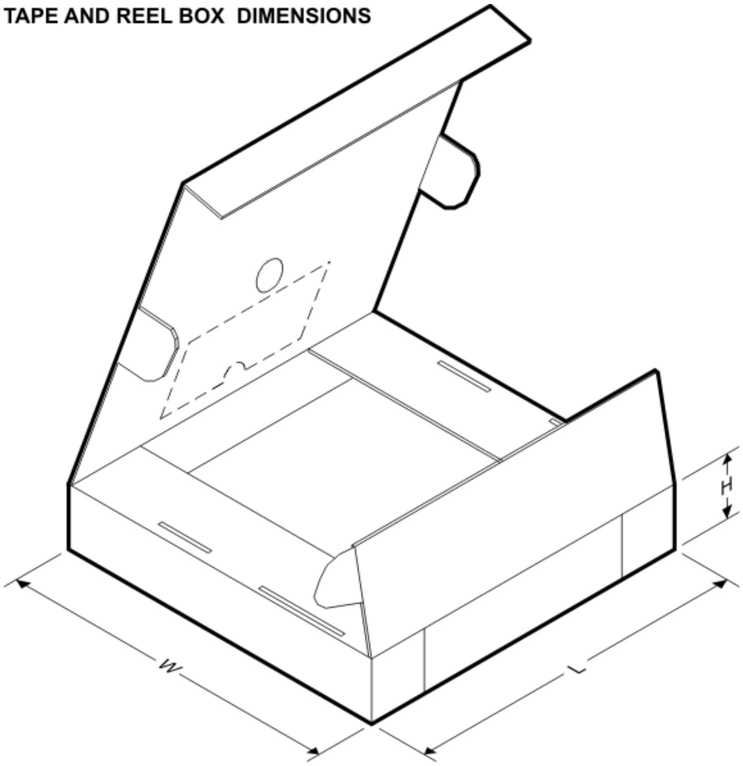
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS4RSER	UQFN	RSE	10	3000	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1
SN65LVDS4RSET	UQFN	RSE	10	250	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

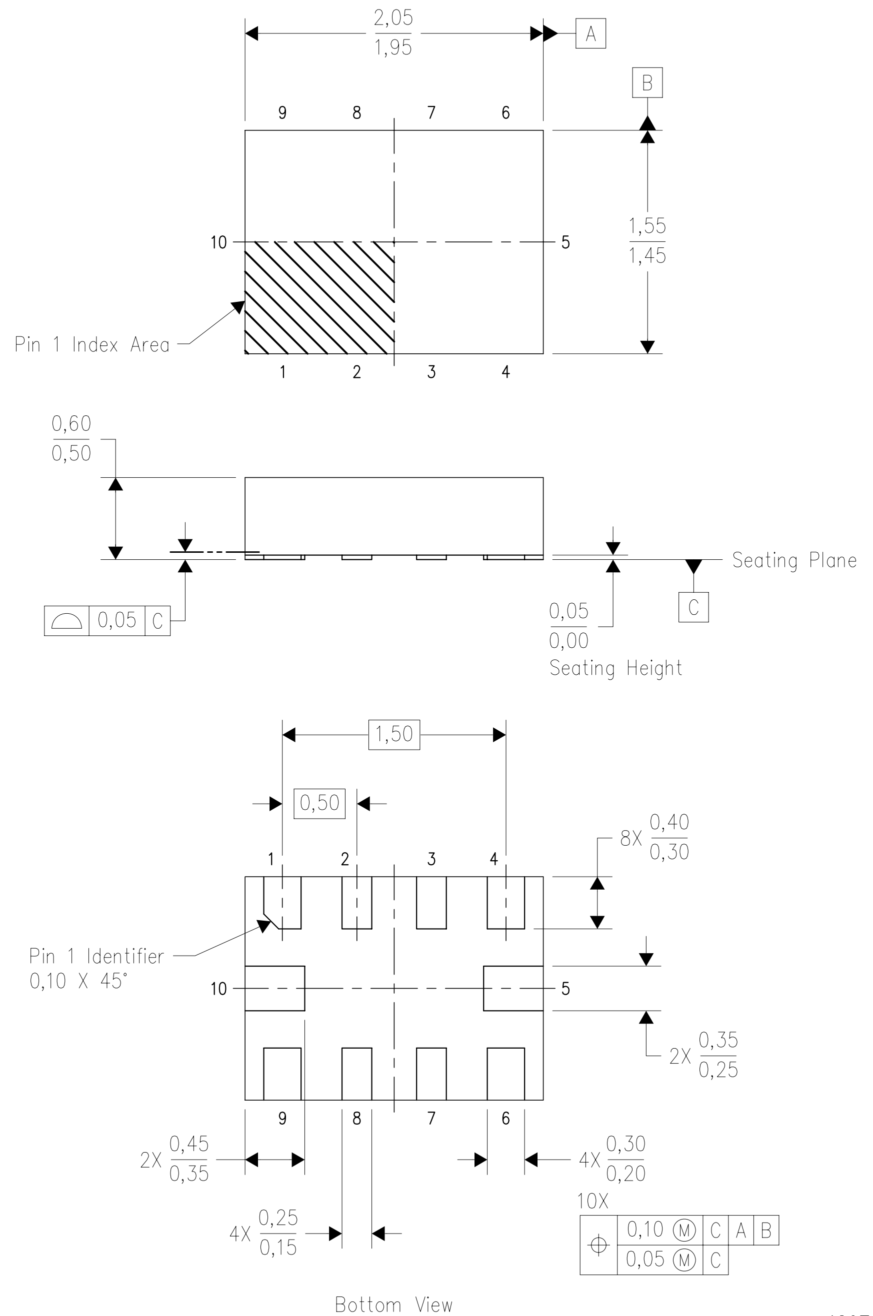
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS4RSER	UQFN	RSE	10	3000	202.0	201.0	28.0
SN65LVDS4RSET	UQFN	RSE	10	250	202.0	201.0	28.0

RSE (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD

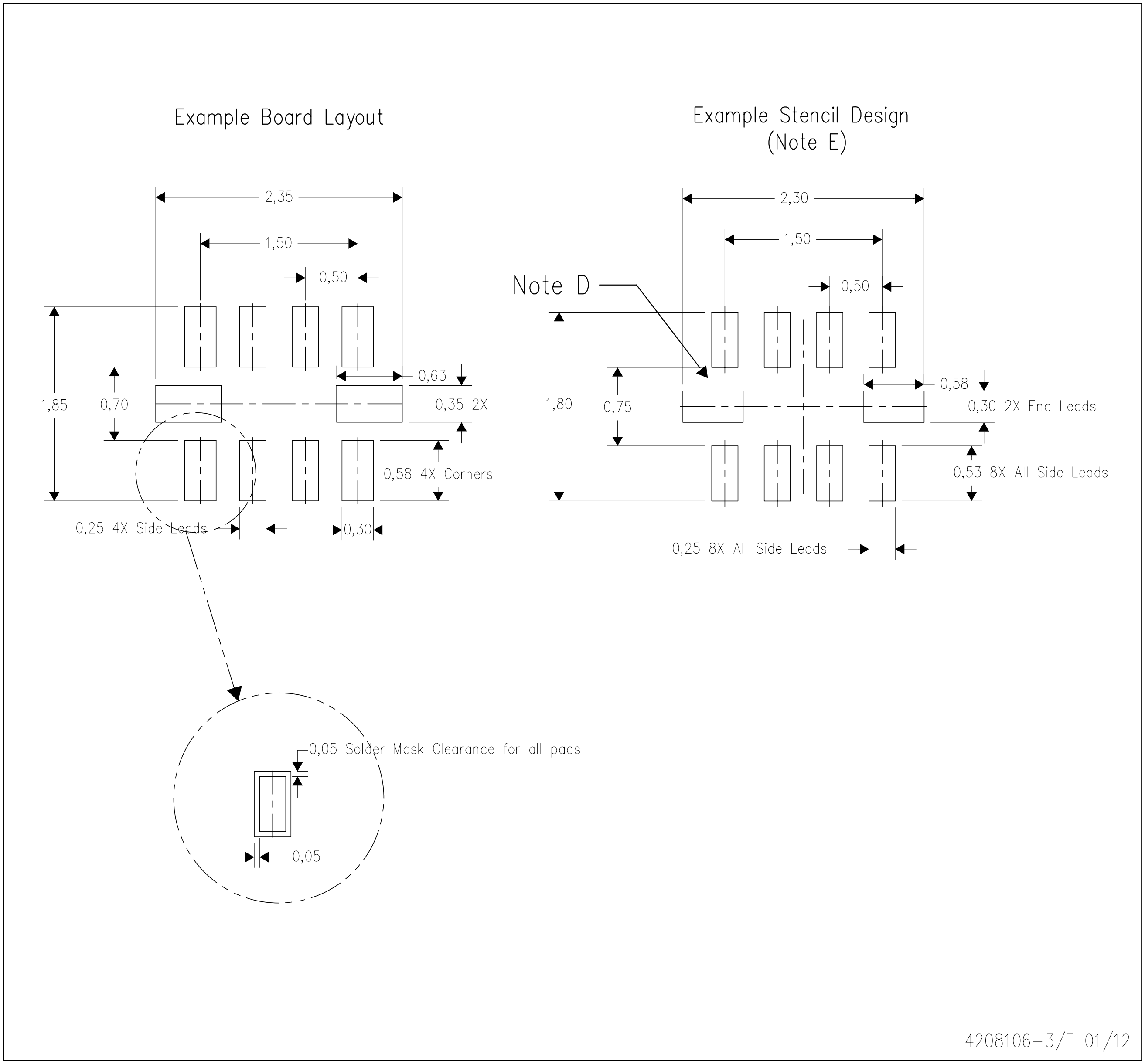


4207268–3/D 01/11

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UEFD.

RSE (R-PUQFN-N10) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
		TI E2E Community Home Page	e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265