CSD25310Q2, 20 V P-Channel NexFET™ Power MOSFETs

Check for Samples: CSD25310Q2

FEATURES

- **Ultra-Low Q_g and Q_{gd}**
- **Low On Resistance**
- **Low Thermal Resistance**
- **Pb-Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 2-mm × 2-mm Plastic Package**

APPLICATIONS

- **Battery Management**
- **Load Management**
- **Battery Protection**

DESCRIPTION

This 19.9 mΩ, –20 V P-Channel device is designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. Its low on resistance coupled with an extremely small footprint in a SON 2 mm × 2 mm plastic package make the device ideal for battery operated space constrained operations.

PRODUCT SUMMARY

V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	3.6		nC
Q_{gd}	Gate Charge Gate to Drain	0.5		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –1.8 V	59.0	mΩ
		V_{GS} = –2.5 V	27.0	mΩ
		V_{GS} = –4.5 V	19.9	mΩ
$V_{GS(th)}$	Threshold Voltage	-0.85		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD25310Q2	SON 2-mm × 2-mm Plastic Package	7-Inch Reel	3000	Tape and Reel

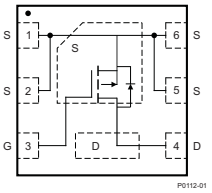
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	±8	V
I_D	Continuous Drain Current (Package Limit)	–20	A
	Continuous Drain Current(1)	–9.6	A
I_{DM}	Pulsed Drain Current(2)	48	A
P_D	Power Dissipation(1)	2.9	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C

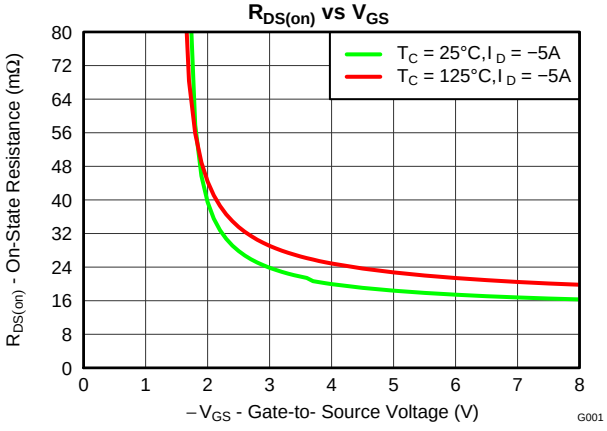
(1) $R_{\theta JA}$ = 43°C/W on 1 in² Cu (2 oz.) on .060-inch thick FR4 PCB.

(2) Pulse duration 10 µs, duty cycle ≤ 2%

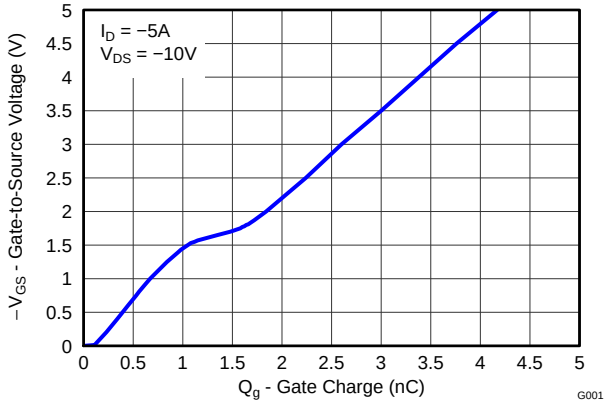
Top View



$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = –250 µA	–20			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –16 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –8 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.55	–0.85	–1.10	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –1.8 V, I_{DS} = –5 A		59.0	89.0	mΩ
		V_{GS} = –2.5 V, I_{DS} = –5 A		27.0	32.5	mΩ
		V_{GS} = –4.5 V, I_{DS} = –5 A		19.9	23.9	mΩ
g_{fs}	Transconductance	V_{DS} = –16 V, I_{DS} = –5 A		34		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		504	655	pF
C_{OSS}	Output Capacitance			281	365	pF
C_{RSS}	Reverse Transfer Capacitance			16.7	21.7	pF
R_g	Series Gate Resistance			1.9		Ω
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –5 A		3.6	4.7	nC
Q_{gd}	Gate Charge Gate to Drain			0.5		nC
Q_{gs}	Gate Charge Gate to Source			1.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.6		nC
Q_{OSS}	Output Charge	V_{DS} = –10 V, V_{GS} = 0 V		5.0		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –5 A, R_G = 2 Ω		8		ns
t_r	Rise Time			15		ns
$t_{d(off)}$	Turn Off Delay Time			15		ns
t_f	Fall Time			5		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{DS} = –5 A, V_{GS} = 0 V		–0.8	–1.0	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = –10 V, I_F = –5 A, di/dt = 200 A/µs		9.2		nC
t_{rr}	Reverse Recovery Time			13		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			4.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1)(2)			55	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

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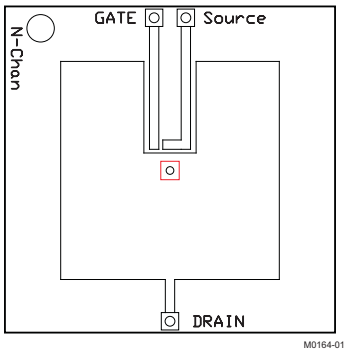
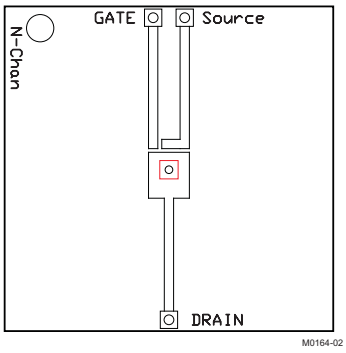


Max $R_{\theta JA}$ = 55 when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 215 when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

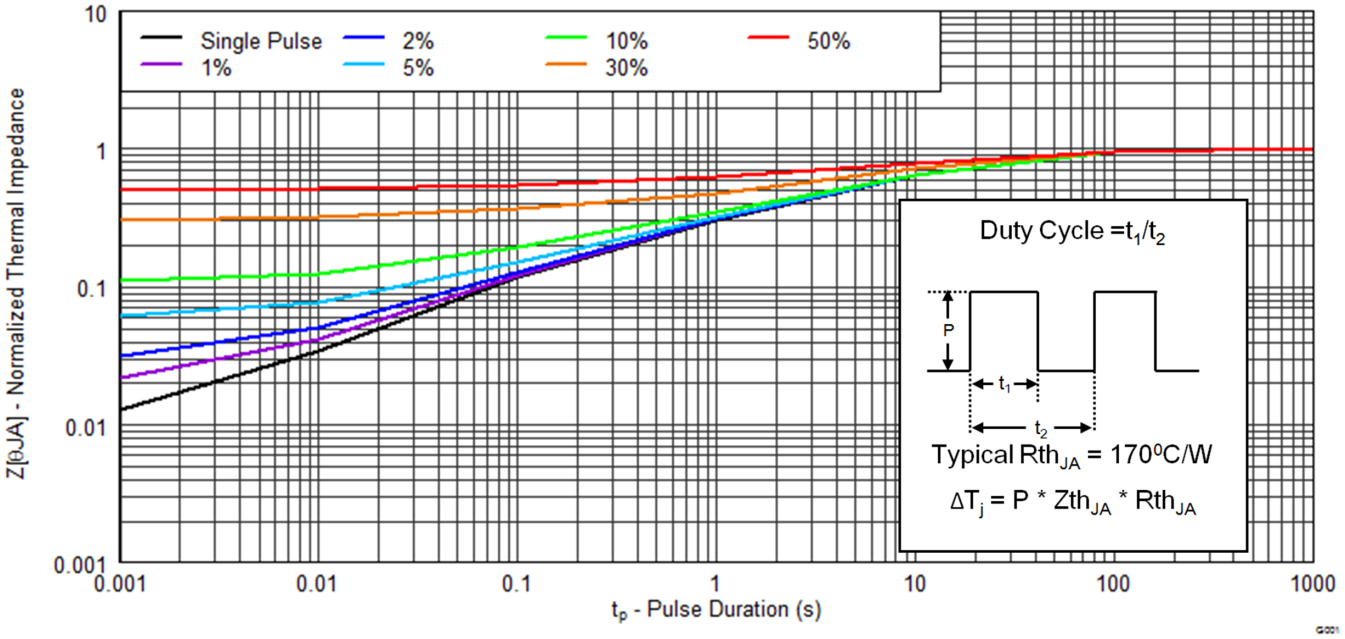


Figure 1. Transient Thermal Impedance

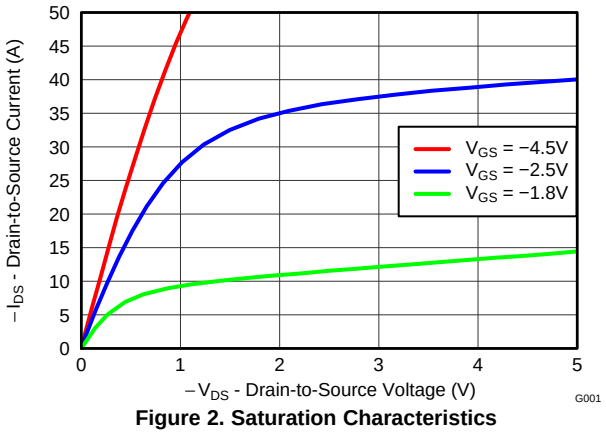


Figure 2. Saturation Characteristics

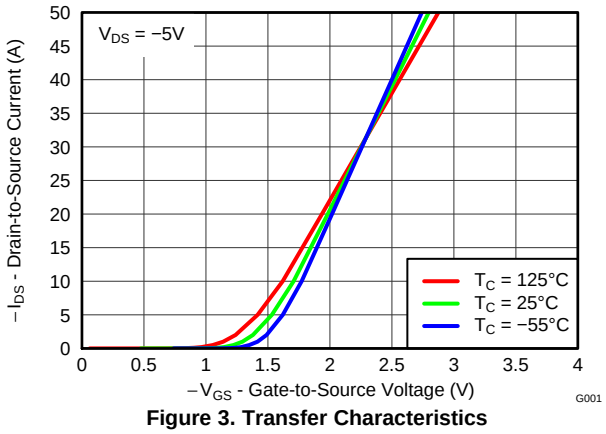


Figure 3. Transfer Characteristics

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

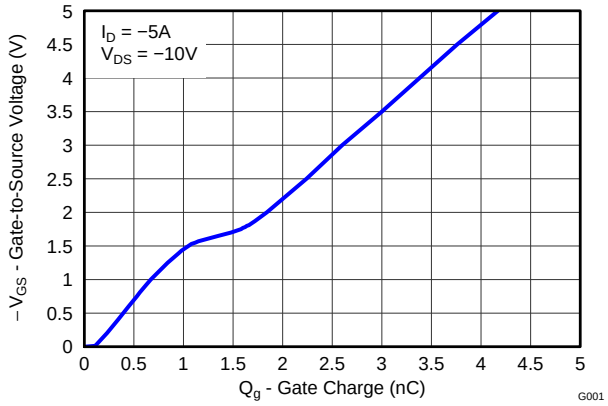

Figure 4. Gate Charge

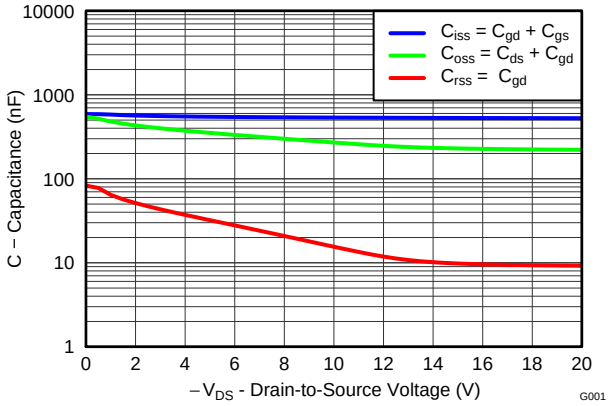

Figure 5. Capacitance

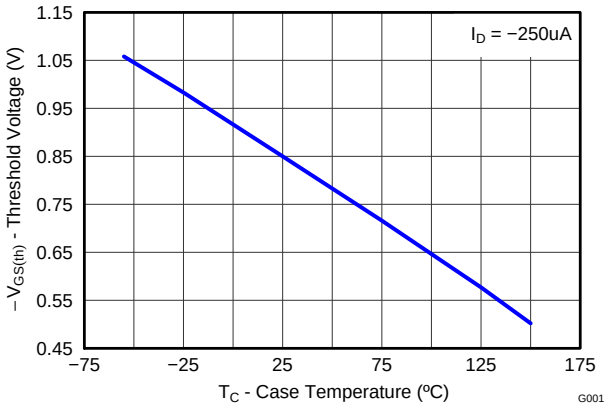

Figure 6. Threshold Voltage vs Temperature

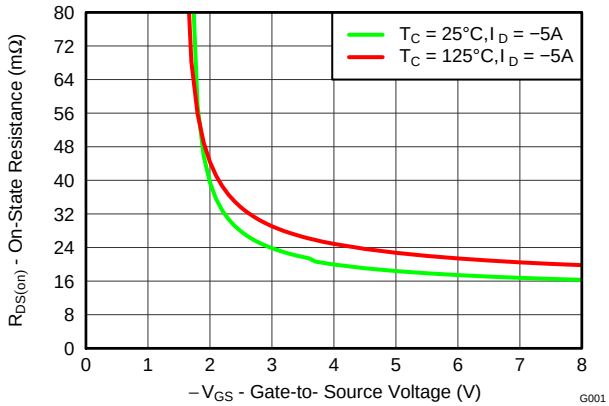

Figure 7. On-State Resistance vs Gate-to-Source Voltage

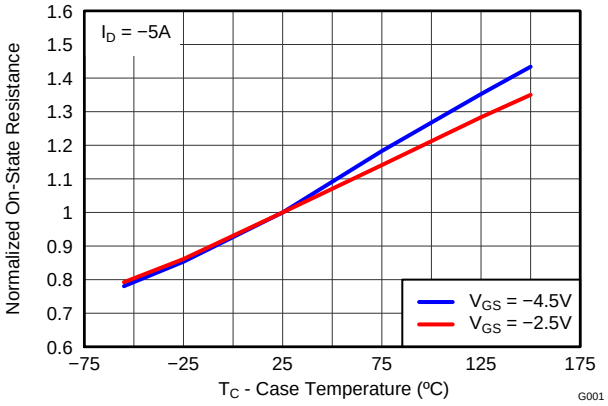

Figure 8. Normalized On-State Resistance vs Temperature

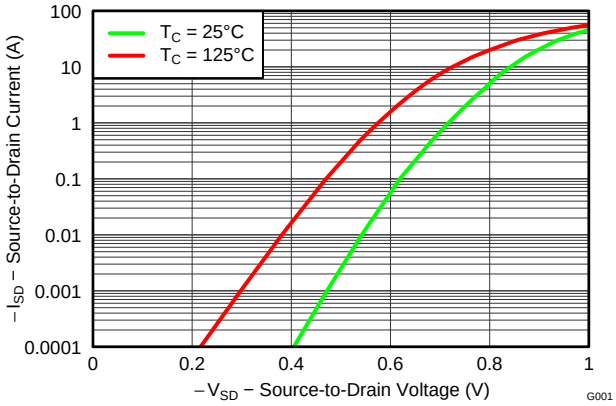

Figure 9. Typical Diode Forward Voltage

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

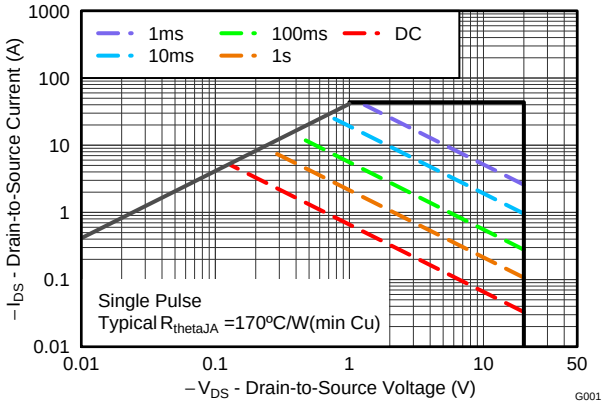


Figure 10. Maximum Safe Operating Area

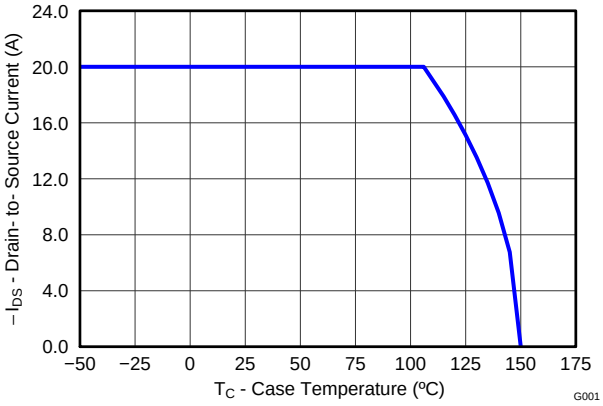
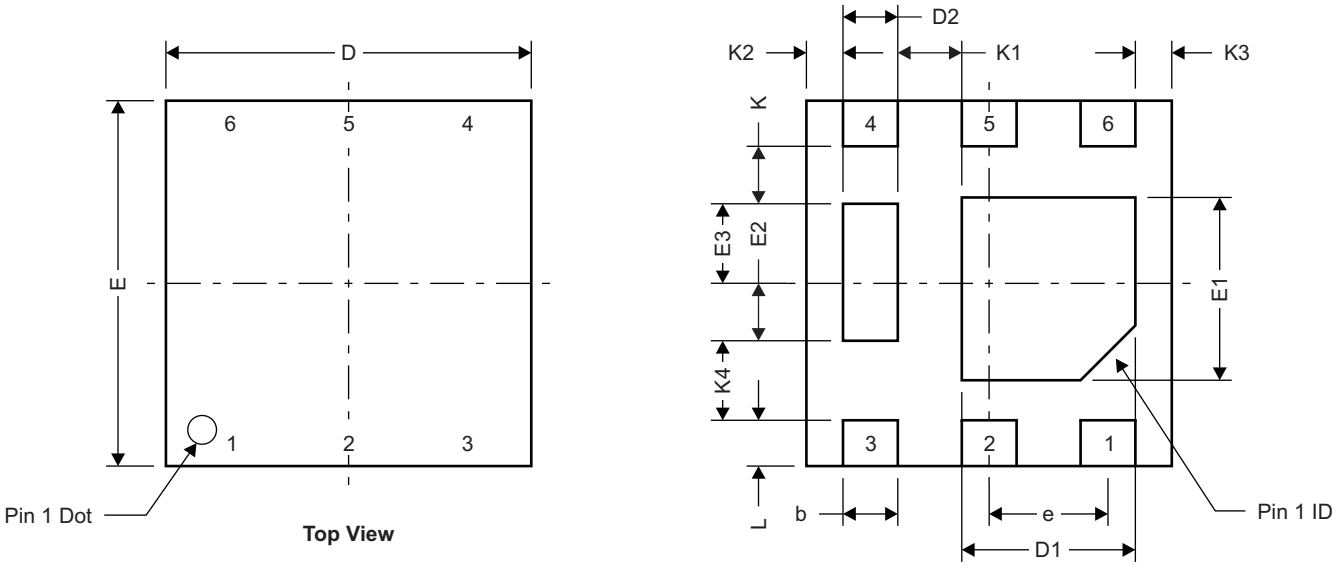


Figure 11. Maximum Drain Current vs Temperature

MECHANICAL DATA

Q2 Package Dimensions



M0165-01

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C	0.203 TYP			0.008 TYP		
D	2.000 TYP			0.080 TYP		
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2	0.300 TYP			0.012 TYP		
E	2.000 TYP			0.080 TYP		
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2	0.280 TYP			0.0112 TYP		
E3	0.470 TYP			0.0188 TYP		
e	0.650 TYP			0.026 TYP		
K	0.280 TYP			0.0112 TYP		
K1	0.350 TYP			0.014 TYP		
K2	0.200 TYP			0.008 TYP		
K3	0.200 TYP			0.008 TYP		
K4	0.470 TYP			0.0188 TYP		
L	0.200	0.25	0.300	0.008	0.010	0.012

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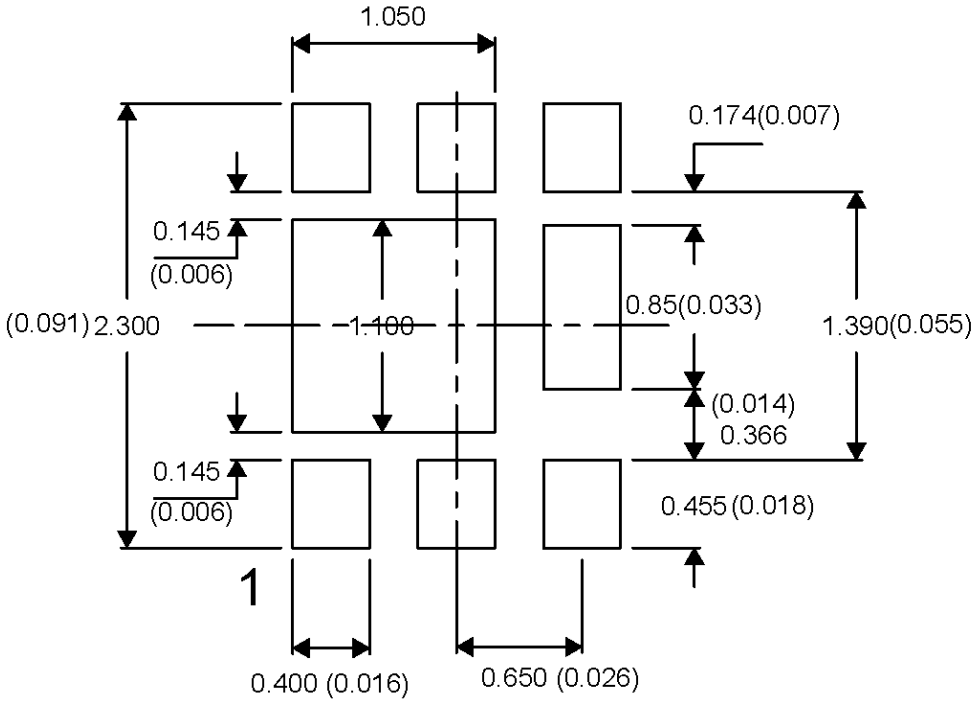
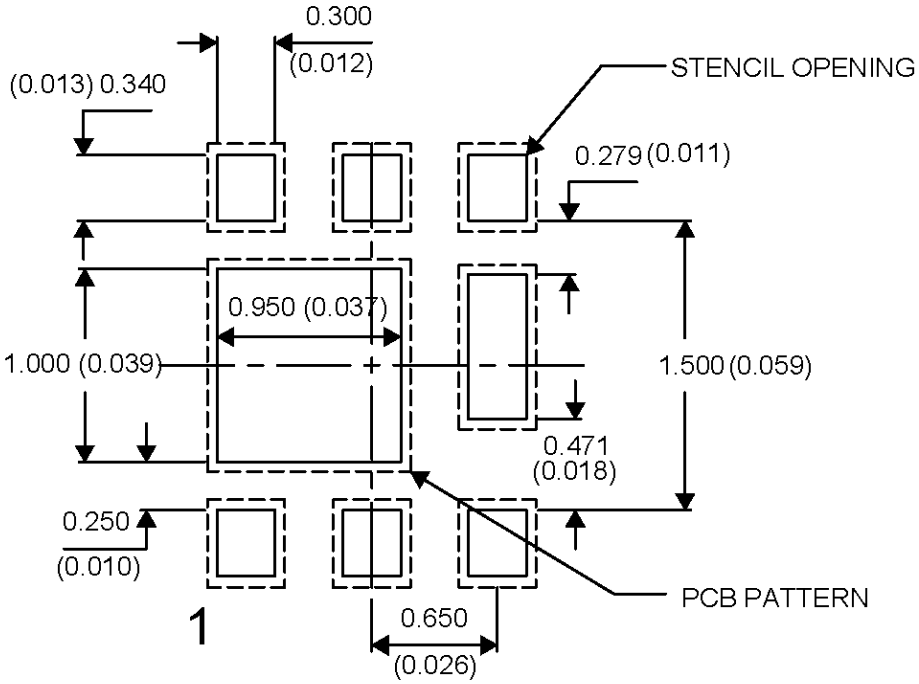
Recommended PCB Pattern



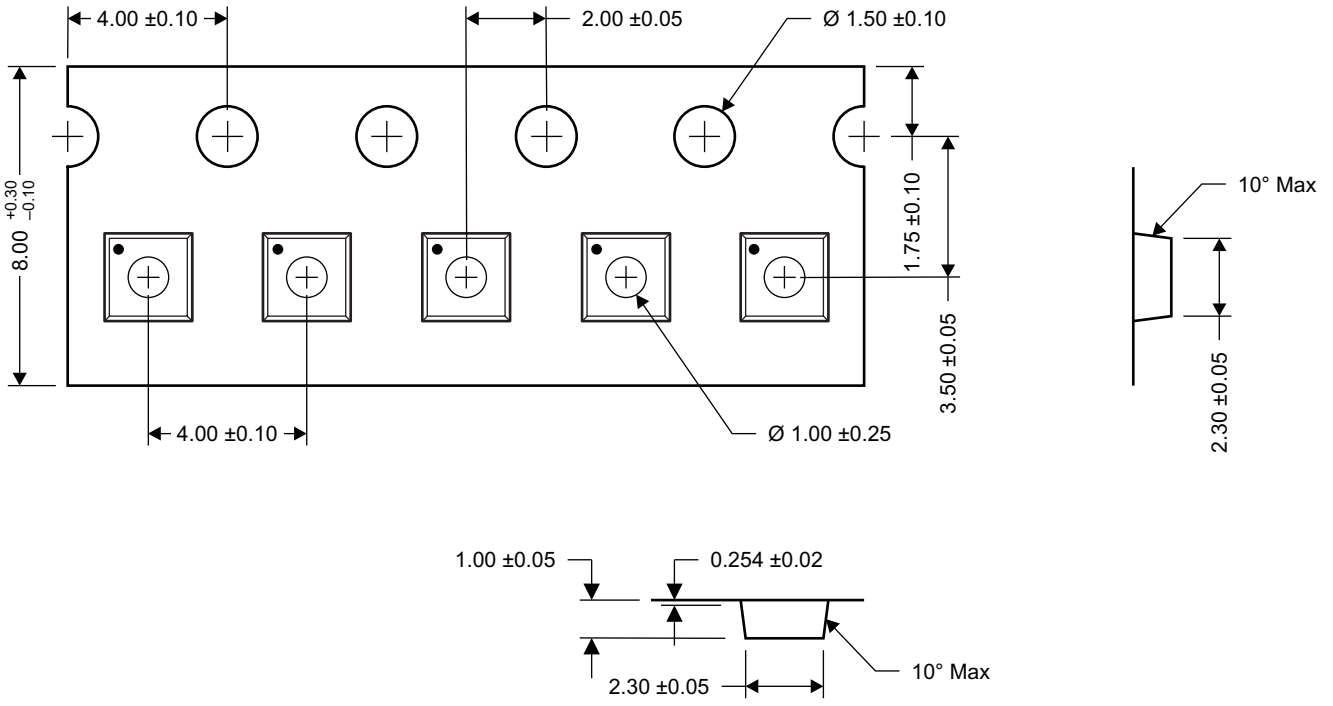
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Recommended Stencil Pattern



Note: All dimensions are in mm, unless otherwise specified.

Q2 Tape and Reel Information



Notes: 1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ±0.20
3. Other material available
4. Typical SR of form tape Max 10^9 OHM/SQ
5. All dimensions are in mm, unless otherwise specified.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25310Q2	ACTIVE	SON	DQK	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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