

## ***Using the TPS51916EVM-746 Complete DDR2, DDR3, DDR3L, and DDR4 Memory Power Solution Synchronous Buck Controller, 2-A LDO, Buffered Reference***

The TPS51916EVM-746 evaluation module (EVM) allows users to evaluate the performance of the TPS51916 low-dropout (LDO) regulator. The TPS51916 provides a complete power supply for DDR2, DDR3, DDR3L, and DDR4 memory system in the lowest total cost and minimum space. TPS51916 integrates a synchronous buck controller (VDDQ) with a 2-A sink/source tracking LDO (VTT) and buffered, low-noise reference (VTTREF).

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## 1 Description

The TPS51916EVM-746 is designed to use a regulated 12-V bus to produce a regulated 1.5-VDDQ output at up to a 20-A load current. The TPS51916EVM-746 demonstrates TPS51916 in a typical DDR3 application with D-CAP2™-mode operation. The EVM also provides test points to evaluate the performance of the TPS51916.

### 1.1 Typical Applications

- DDR2/DDR2/DDR3L/DDR4 memory power supplies
- SSTL\_18, SSTL\_15, SSTL\_135, and HSTL termination

### 1.2 Features

The TPS51916EVM-746 features:

- D-CAP2™-mode operation with all-ceramic VDDQ output capacitor
- 20-Adc steady-state VDDQ output current
- Support VDDQ prebias start-up
- SW1 and SW2 provides S3, S5 power control
- Optional external VLDOIN voltage for efficiency and flexible operation
- Convenient test points for probing critical waveforms

## 2 Electrical Performance Specifications

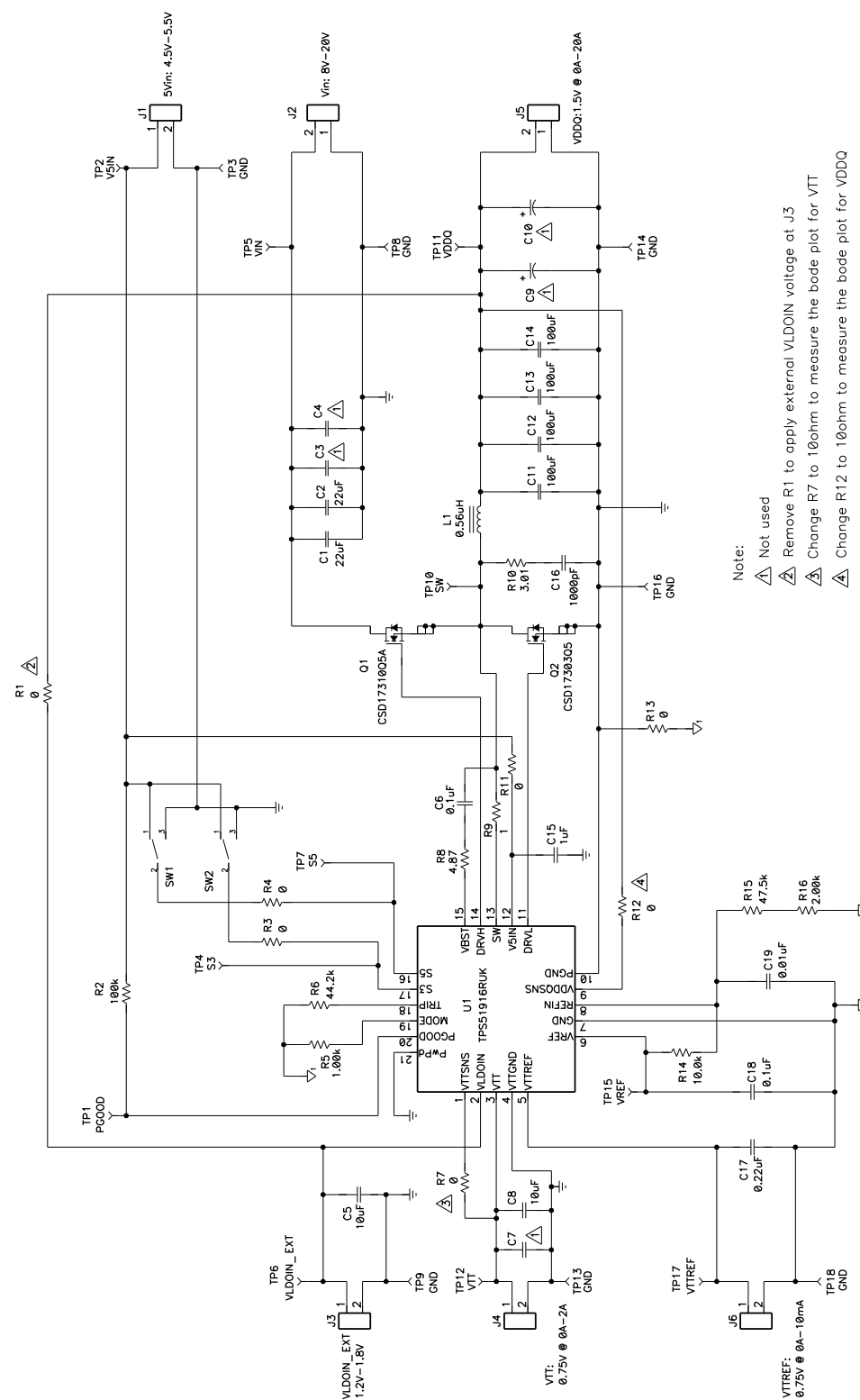
**Table 1. TPS51916EVM-746 Electrical Performance Specifications**

| Parameter                                  | Test Conditions                                                             | Min  | Typ                    | Max | Units |
|--------------------------------------------|-----------------------------------------------------------------------------|------|------------------------|-----|-------|
| <b>Input Characteristics</b>               |                                                                             |      |                        |     |       |
| Voltage range                              | VIN                                                                         | 8    | 12                     | 20  | V     |
|                                            | V5IN                                                                        | 4.5  | 5                      | 5.5 |       |
| Maximum input current                      | VIN = 8 V, I <sub>VDDQ</sub> = 20 A                                         |      | 4.21                   |     | A     |
| No-load input current                      | Vin = 20 V, I <sub>VDDQ</sub> = 0 A                                         |      | 0.1                    |     | mA    |
| <b>VDDQ Output</b>                         |                                                                             |      |                        |     |       |
| VDDQ Output voltage (VDDQ <sub>SNS</sub> ) | DDR3 (Default setting), R15 = 47.5k, R16 = 2k                               |      | 1.5                    |     | V     |
|                                            | DDR2, R15 = R16= Open                                                       |      | 1.8                    |     | V     |
|                                            | DDR3L, R15 = 28k, R16 = 2k                                                  |      | 1.35                   |     | V     |
|                                            | DDR4, R15 = 18.2k, R16 = 2k                                                 |      | 1.2                    |     | V     |
| VDDQ Output voltage regulation             | Line regulation (Vin = 8 V–20 V)                                            |      | 0.2%                   |     |       |
|                                            | Load regulation (Vin = 12 V, I <sub>VDDQ</sub> = 0 A–20 A)                  |      | 0.5%                   |     |       |
| Output voltage ripple                      | Vin = 12 V, I <sub>VDDQ</sub> = 20 A                                        |      | 20                     |     | mVpp  |
| Output load current                        |                                                                             | 0    |                        | 20  | A     |
| Output overcurrent                         |                                                                             |      | 30                     |     | A     |
| Switching frequency                        |                                                                             |      | 500                    |     | kHz   |
| Peak efficiency                            | Vin = 12 V, 1.5 VDDQ/8 A                                                    |      | 90.93%                 |     |       |
| Full-load efficiency                       | Vin = 12 V, 1.5 VDDQ/20 A                                                   |      | 87.3%                  |     |       |
| <b>VTT Output</b>                          |                                                                             |      |                        |     |       |
| VTT output voltage                         |                                                                             |      | VTTREF                 |     | V     |
| VTT output current                         | For DDR2(0.9 VTT) and DDR3(0.75 VTT)                                        | –2   |                        | 2   | A     |
|                                            | For DDR3L(0.675 VTT) and DDR4(0.6 VTT)                                      | –1.5 |                        | 1.5 | A     |
| VTT output tolerance to VTTREF             | I <sub>VTT</sub>   < 2 A, 1.4 V ≤ V <sub>VDDQ<sub>SNS</sub></sub> ≤ 1.8 V   | –40  |                        | 40  | mV    |
|                                            | I <sub>VTT</sub>   < 1.5 A, 1.2 V ≤ V <sub>VDDQ<sub>SNS</sub></sub> < 1.4 V | –40  |                        | 40  | mV    |
| <b>VTTREF Output</b>                       |                                                                             |      |                        |     |       |
| VTTREF output voltage                      |                                                                             |      | VDDQ <sub>SNS</sub> /2 |     | V     |
| VTTREF output current                      |                                                                             | –10  |                        | 10  | mA    |

**Table 1. TPS51916EVM-746 Electrical Performance Specifications (continued)**

| Parameter                          | Test Conditions                                                  | Min   | Typ | Max   | Units |
|------------------------------------|------------------------------------------------------------------|-------|-----|-------|-------|
| VTTREF output tolerance to VDDQSNS | $ I_{V_{TTREF}}  < 100 \mu A, 1.2 V \leq V_{VDDQSNS} \leq 1.8 V$ | 49.2% |     | 50.8% |       |
|                                    | $ I_{V_{TTREF}}  < 10 mA, 1.2 V \leq V_{VDDQSNS} < 1.8 V$        | 49%   |     | 51%   |       |
| Operating temperature              |                                                                  |       | 25  |       | °C    |

### 3 Schematic



### Figure 1. TPS51916EVM-746 Schematic

## 4 Test Setup

### 4.1 Test Equipment

**Voltage Source V5IN:** The input voltage source V5IN must be a 0-V to 5-V variable dc source capable of supplying 1 Adc. Connect V5IN to J1 as shown in [Figure 3](#).

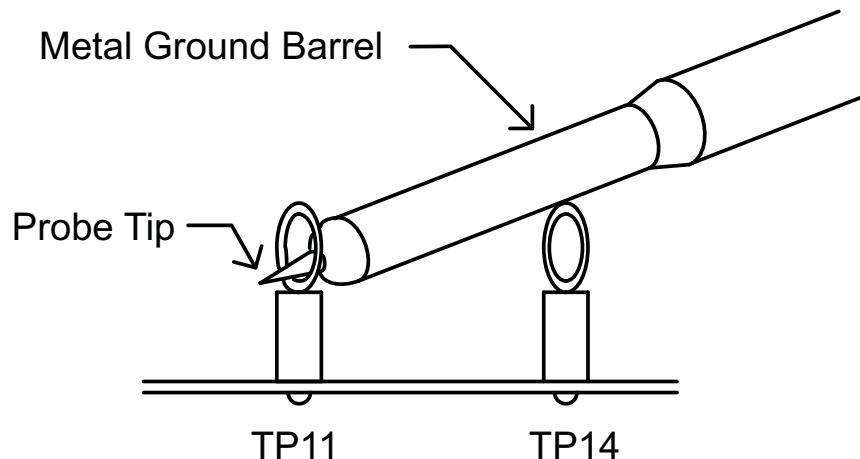
**Voltage Source VIN:** The input voltage source VIN must be a 0-V to 20-V variable dc source capable of supplying 10 Adc. Connect VIN to J2 as shown in [Figure 3](#).

**Multimeters:**

- V1: V5IN at TP2 (V5IN) and TP3 (GND).
- V2: VIN at TP5 (VIN) and TP8 (GND).
- V3: VDDQ at TP11 (VDDQ) and TP14 (GND).
- V4: VTT at TP12 (VTT) and TP13 (GND).
- V5: VTTREF at TP17 (VTTREF) and TP18 (GND).
- A1: VIN input current
- A2: V5IN input current

**Output Load:** The output load must be an electronic constant-resistance mode load capable of 0-Adc to 20 Adc at 1.5 V.

**Oscilloscope:** A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope must be set for 1-M $\Omega$  impedance, 20-MHz bandwidth, ac coupling, 2- $\mu$ s/division horizontal resolution, 20-mV/division vertical resolution. Test points TP11 and TP14 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP11 and holding the ground barrel on TP14 as shown in [Figure 2](#). Using a leaded ground connection may induce additional noise due to the large ground loop.



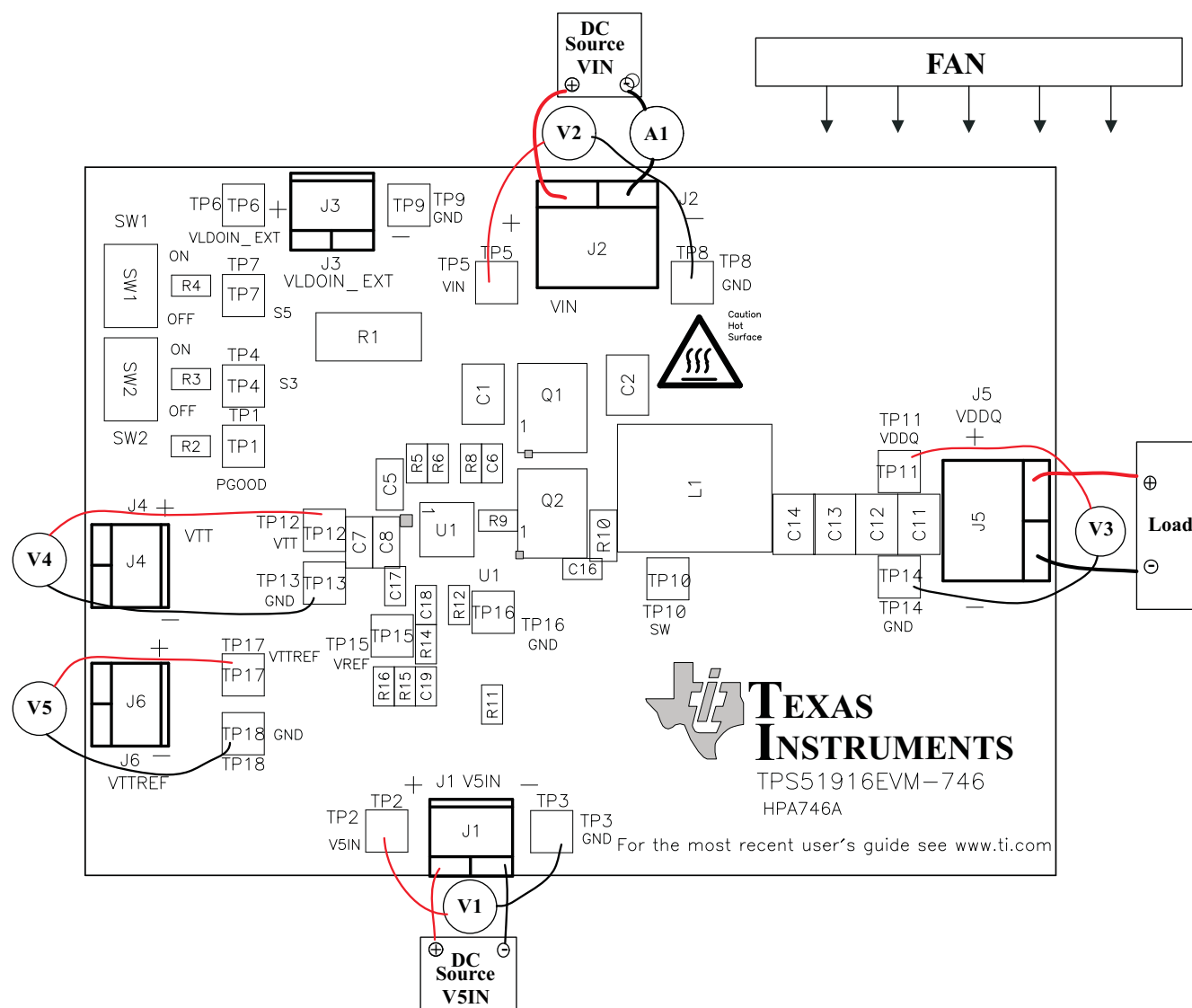
**Figure 2. Tip and Barrel Measurement for VDDQ Output Ripple**

**Fan:** Some of the components in this EVM may approach temperatures of 60°C during operation. A small fan capable of 200-400 LFM is recommended to reduce component temperatures while the EVM is operating. The EVM must not be probed if the fan is not running.

**Recommended Wire Gauge:**

1. V5IN to J1(5-V input):  
The recommended wire size is 1x AWG 18 per input connection, with the total length of wire less than 4 feet (2-foot input, 2-foot return).
2. VIN to J2(12-V input):  
The recommended wire size is 1x AWG 16 per input connection, with the total length of wire less than 4 feet (2-foot input, 2-foot return).
3. J5 to LOAD:  
The minimum recommended wire size is 2x AWG 16, with the total length of wire less than 4 feet (2-foot input, 2-foot return)

## 4.2 Recommended Test Setup



**Figure 3. TPS51916EVM-746 Recommended Test Setup**

Figure 3 is the recommended test setup to evaluate the TPS51916EVM-746. When working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM.

### Input Connections:

1. Prior to connecting the dc source V5IN, it is advisable to limit the source current from V5IN to 1 A maximum. Ensure that V5IN is initially set to 0 V and connected as shown in Figure 3.
2. Prior to connecting the dc source VIN, it is advisable to limit the source current from VIN to 10 A maximum. Ensure that VIN is initially set to 0 V and connected as shown in Figure 3.
3. Connect voltmeters V1 at TP2 (V5IN) and TP3 (GND) to measure V5IN voltage, V2 at TP5 (VIN), and TP8 (GND) to measure VIN voltage as shown in Figure 3.
4. Connect a current meter A1 between dc source VIN and J2 to measure the input current.
5. Connect a current meter A2 between dc source V5IN and J1 to measure the input current.

### Output Connections:

1. Connect the load to J5 and set the load to constant-resistance mode to sink 0 Adc before V5IN and VIN are applied.
2. Connect a voltmeter V3 at TP11 (VDDQ) and TP14 (GND) to measure VDDQ voltage, V4 at TP12 (VTT) and TP13 (GND) to measure VTT voltage and V5 at TP17 (VTTREF) and TP18 (GND) to measure VTTREF voltage.

#### Other Connections:

Place a fan as shown in [Figure 3](#) and turn it on, ensuring that air is flowing across the EVM.

## 5 Configurations

### 5.1 S3, S5 Enable Selection

The controller can be enabled and disabled by switches SW1 and SW2.

**Default setting: Push SW1 and SW2 to the bottom (OFF position) to disable the controller.**

**Table 2. S3, S5 Enable Selection**

| State | SW2 (S3) set to | SW1(S5) set to | VDDQ           | VTTREF         | VTT            |
|-------|-----------------|----------------|----------------|----------------|----------------|
| S0    | ON position     | ON position    | ON             | ON             | ON             |
| S3    | OFF position    | ON position    | ON             | ON             | OFF(High-Z)    |
| S4/S5 | OFF position    | OFF position   | OFF(Discharge) | OFF(Discharge) | OFF(Discharge) |

## 6 Test Procedure

### 6.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Set up EVM as described in [Section 4](#) and [Figure 3](#).
2. Ensure that the load is set to constant-resistance mode and to sink 0 Adc.
3. Ensure that SW1 and SW2 are in the OFF position.
4. Increase V5IN from 0 V to 5 V. Use V1 to measure V5IN input voltage.
5. Increase VIN from 0 V to 12 V. Use V2 to measure VIN input voltage.
6. Push SW1 and SW2 to ON position to enable the controller.
7. Use V3 to measure VDDQ output voltage.
8. Use V4 to measure VTT output voltage.
9. Use V5 to measure VTTREF output voltage.
10. Use A1 to measure VIN input current for efficiency.
11. Use A2 to measure V5IN input current for efficiency.
12. Vary the load from 0 Adc to 20 Adc; VDDQ must remain in load regulation.
13. Vary VIN from 8 V to 20 V; VDDQ must remain in line regulation.
14. Push SW1 and SW2 to OFF position to disable the controller.
15. Decrease the load to 0 A.
16. Decrease VIN and V5IN to 0 V.

### 6.2 List of Test Points

**Table 3. Test Point Functions**

| Test Points | Name  | Description |
|-------------|-------|-------------|
| TP1         | PGOOD | Power Good  |
| TP2         | V5IN  | 5-V input   |
| TP3         | GND   | Ground      |

**Table 3. Test Point Functions (continued)**

| Test Points | Name       | Description                      |
|-------------|------------|----------------------------------|
| TP4         | S3         | S3 signal input                  |
| TP5         | VIN        | VIN input                        |
| TP6         | VLDOIN_EXT | External input for VLDOIN        |
| TP7         | S5         | S5 signal input                  |
| TP8         | GND        | Ground                           |
| TP9         | GND        | Ground                           |
| TP10        | SW         | Switching node                   |
| TP11        | VDDQ       | VDDQ output                      |
| TP12        | VTT        | VTT output                       |
| TP13        | GND        | Ground                           |
| TP14        | GND        | Ground                           |
| TP15        | VREF       | Internal 1.8-V reference voltage |
| TP16        | GND        | Ground                           |
| TP17        | VTTREF     | Buffered VTT reference voltage   |
| TP18        | GND        | Ground                           |

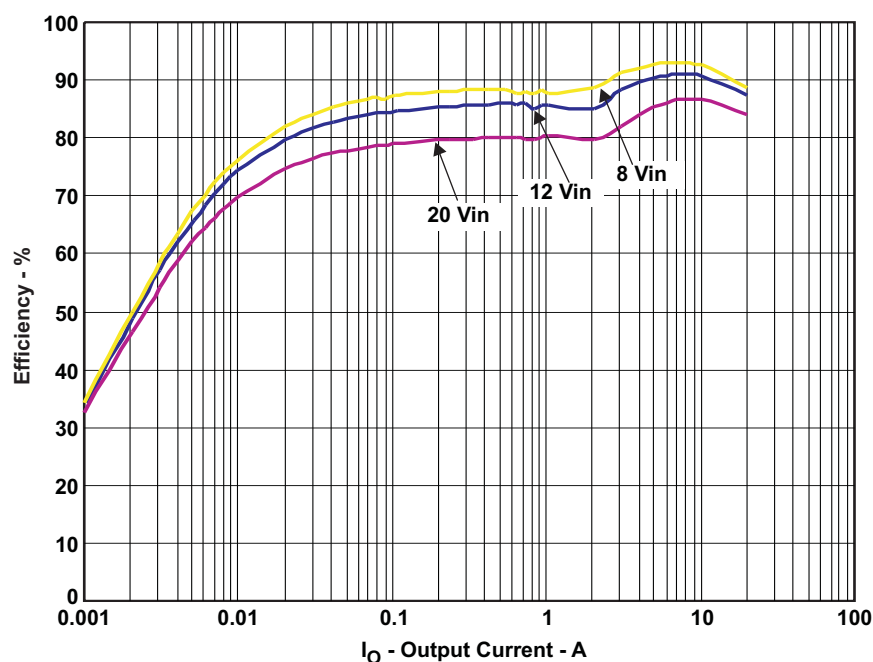
### 6.3 Equipment Shutdown

1. Shut down the load.
2. Shut down V5IN and VIN.
3. Shut down the fan.

## 7 Performance Data and Typical Characteristic Curves

Figure 4 through Figure 22 present typical performance curves for TPS51916EVM-746.

### 7.1 DDR3 VDDQ Efficiency


**Figure 4. DDR3 VDDQ Efficiency**

## 7.2 DDR3 VDDQ Load Regulation

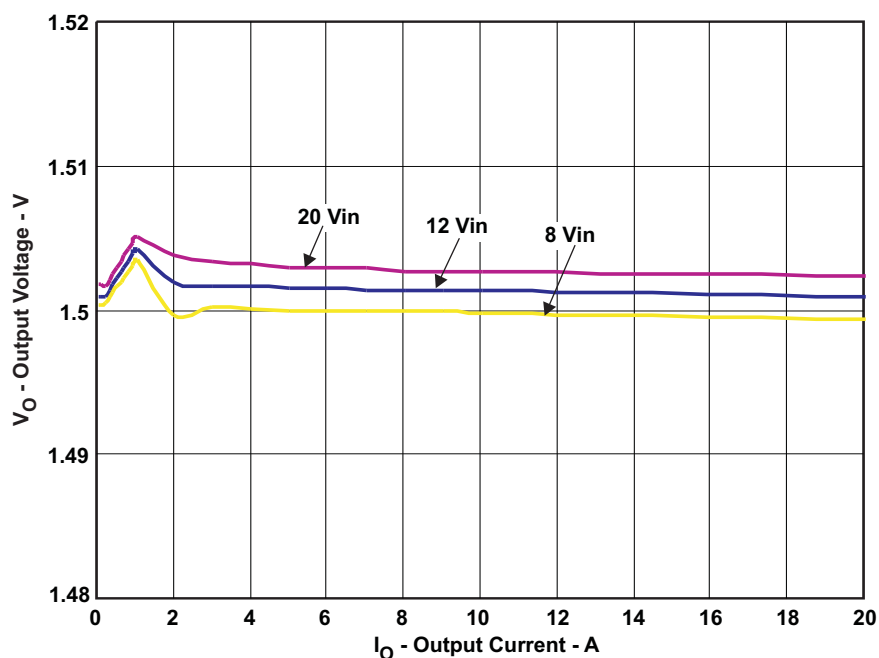


Figure 5. DDR3 VDDQ Load Regulation

## 7.3 DDR3 VDDQ Line Regulation

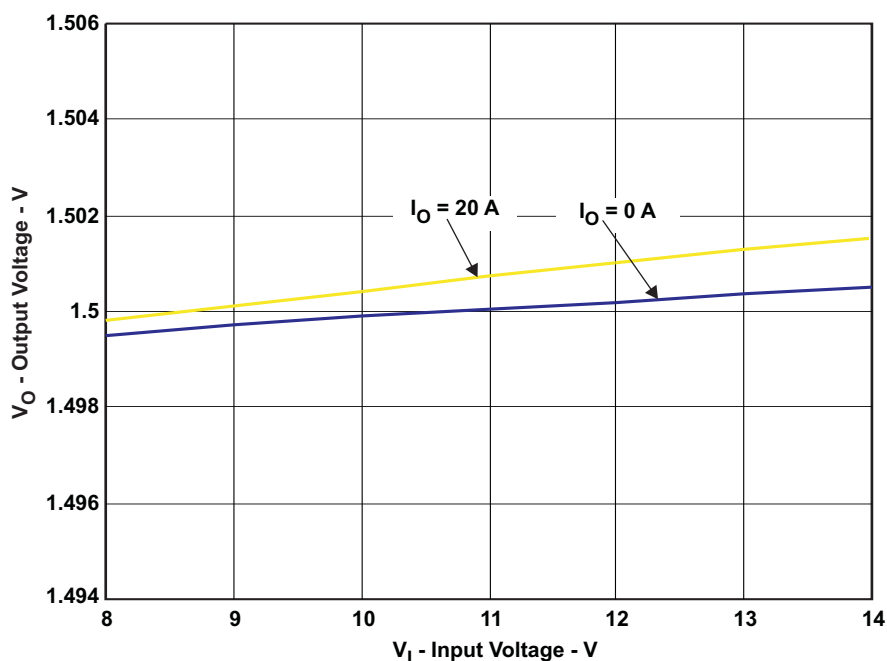


Figure 6. DDR3 VDDQ Line Regulation

## 7.4 DDR3 VTT Load Regulation

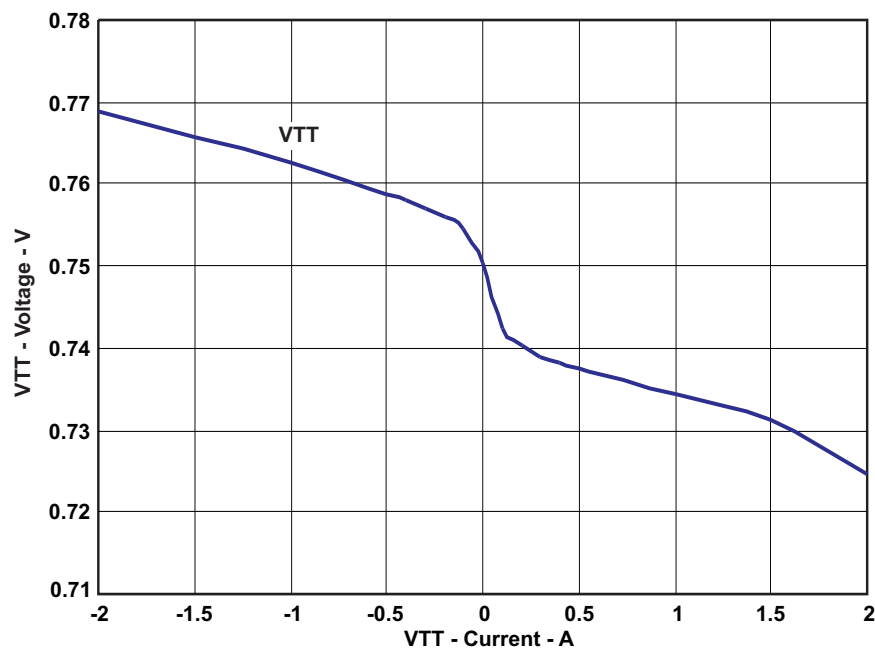


Figure 7. DDR3 VTT Load Regulation

## 7.5 DDR3 VTTREF Load Regulation

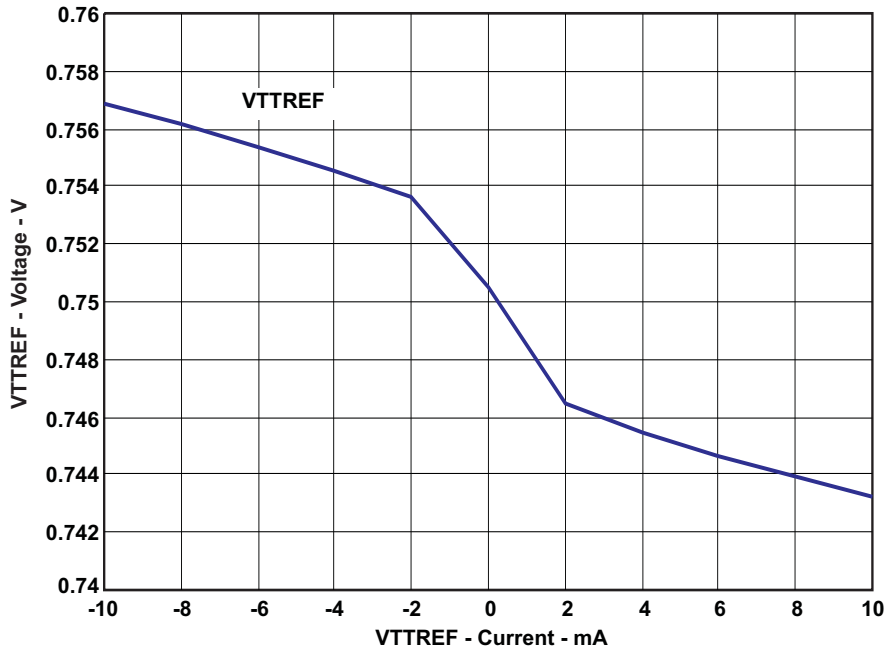


Figure 8. DDR3 VTTREF Load Regulation

## 7.6 DDR3 VTT Dropout Voltage

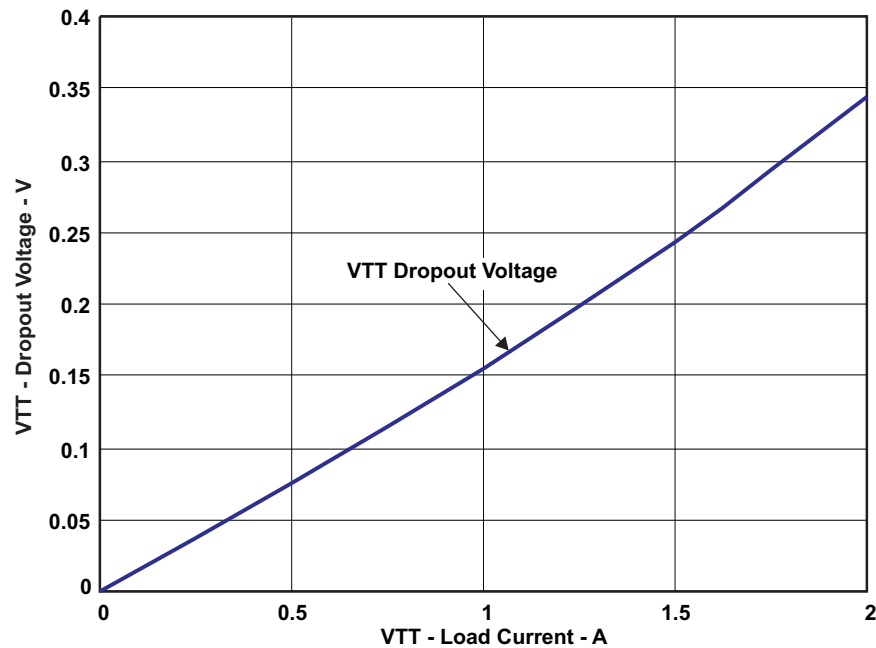


Figure 9. DDR3 VTT Dropout Voltage

## 7.7 DDR3 S5 Enable Turnon/Turnoff

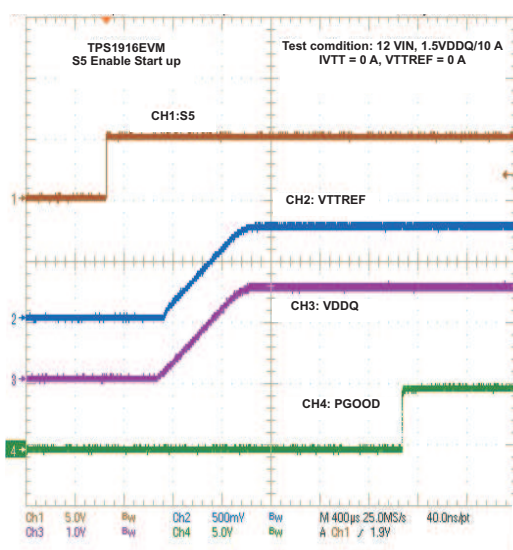


Figure 10. DDR3 S5 Enable Turnon

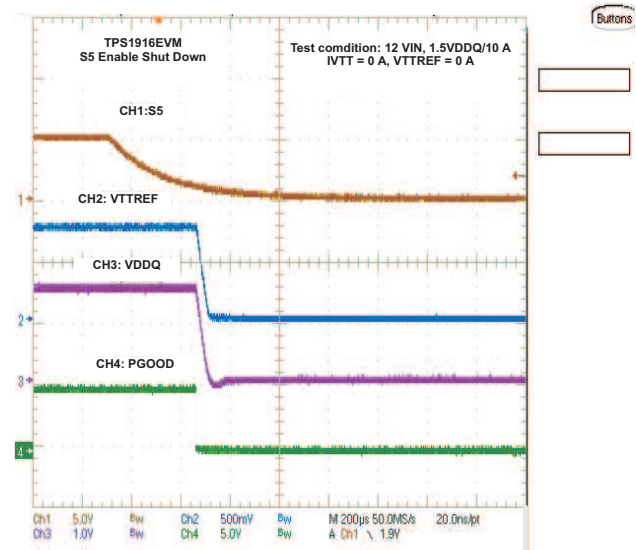


Figure 11. DDR3 S5 Enable Turnoff

## 7.8 S5 Enable Turnon with 1-V Prebias at VDDQ

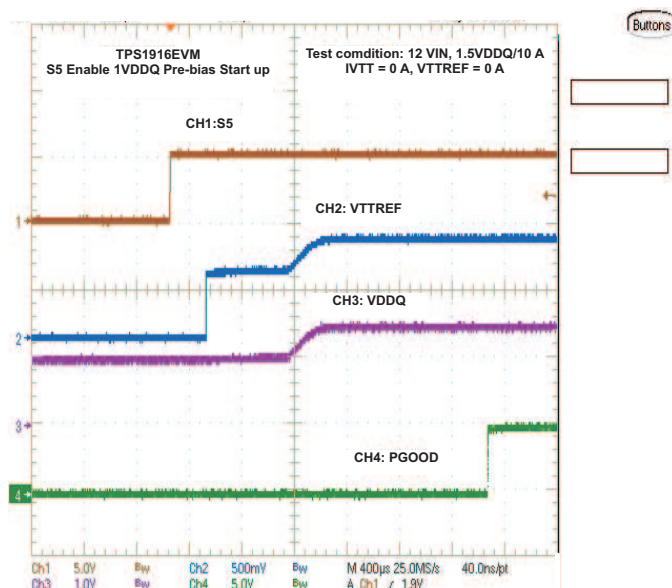


Figure 12. DDR3 S5 Enable Turnon With 1-V Prebias at VDDQ

## 7.9 DDR3 S3 Enable Turnon/ Turnoff (S5 is ON)

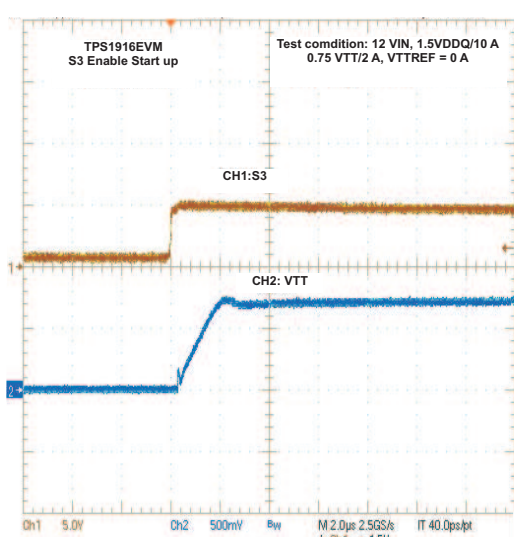


Figure 13. DDR3 S3 Enable Turnon

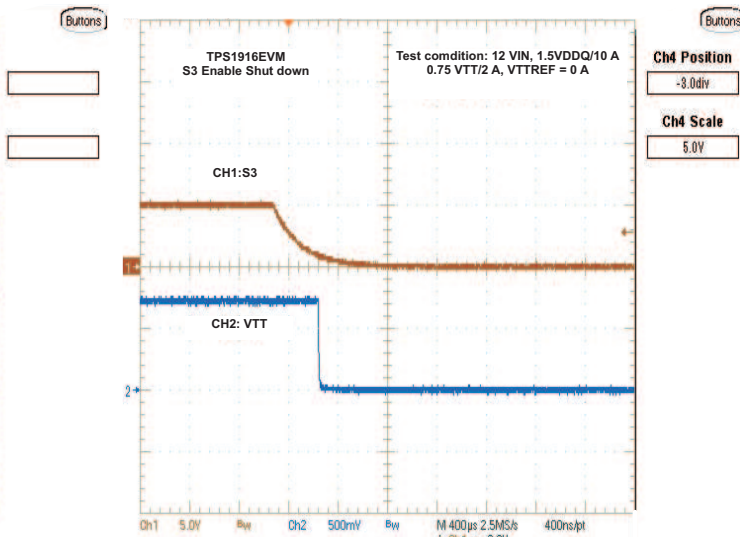


Figure 14. DDR3 S3 Enable Turnoff

## 7.10 DDR3 VDDQ Output Ripple

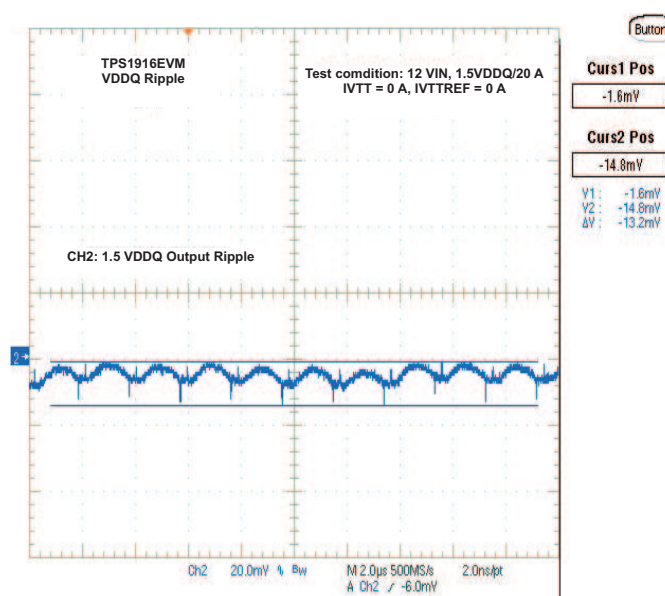


Figure 15. DDR3 VDDQ Output Ripple

## 7.11 DDR3 VDDQ Switching Node

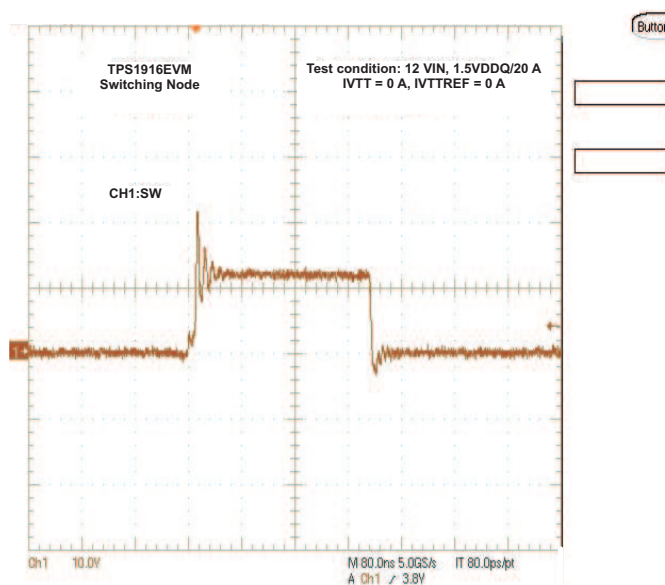


Figure 16. DDR3 VDDQ Switching Node

## 7.12 DDR3 VDDQ Output Transient

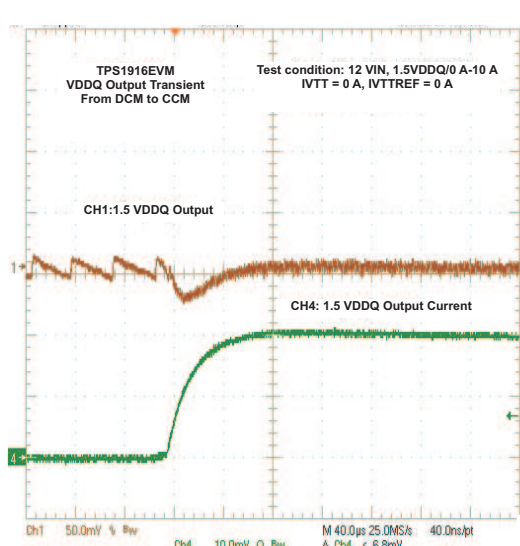


Figure 17. VDDQ Output Transient From DCM to CCM

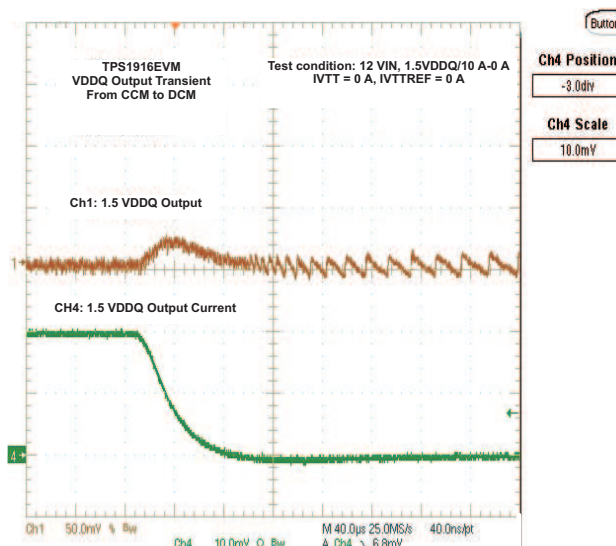


Figure 18. VDDQ Output Transient From CCM to DCM

## 7.13 DDR3 VTT Transient With 1.5-A Sinking and Sourcing Current

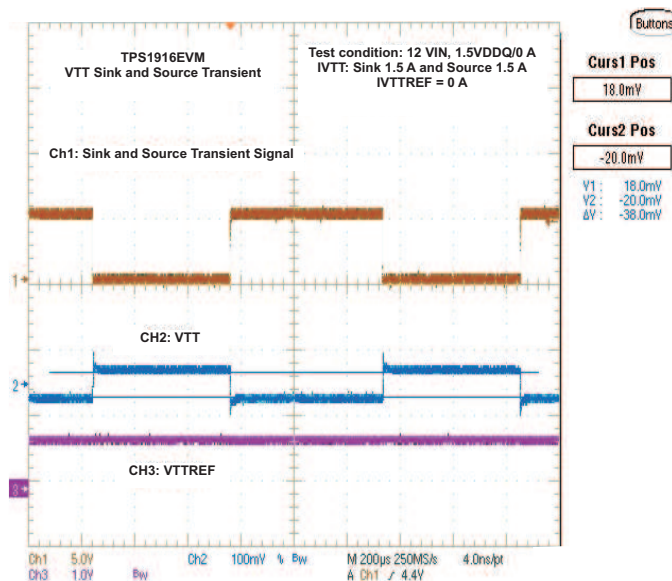


Figure 19. DDR3 VTT Transient With 1.5-A Sinking and Sourcing Current

## 7.14 Thermal Image

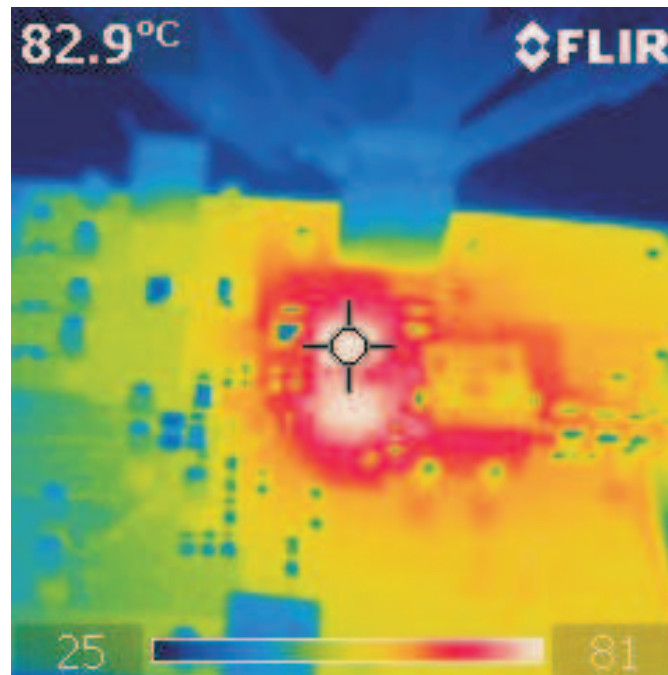


Figure 20. Top Board at 12 Vin, 1.5 VDDQ/20 A, No Load at VTT, 25°C Ambient Without Airflow

## 7.15 DDR3 VDDQ Bode Plot



Figure 21. DDR3 VDDQ Bode Plot at 12 Vin, 1.5 VDDQ/10 A

## 7.16 DDR3 VTT Bode Plot



Figure 22. DDR3 VTT Bode Plot at 12 Vin, 1.5 VDDQ/0 A and VTT 1-A Sourcing

## 8 EVM Assembly Drawing and PCB Layout

The following figures (Figure 23 through Figure 28) show the design of the TPS51916EVM-746 printed-circuit board (PCB). The EVM has been designed using a 4-layer, 2-oz copper circuit board.

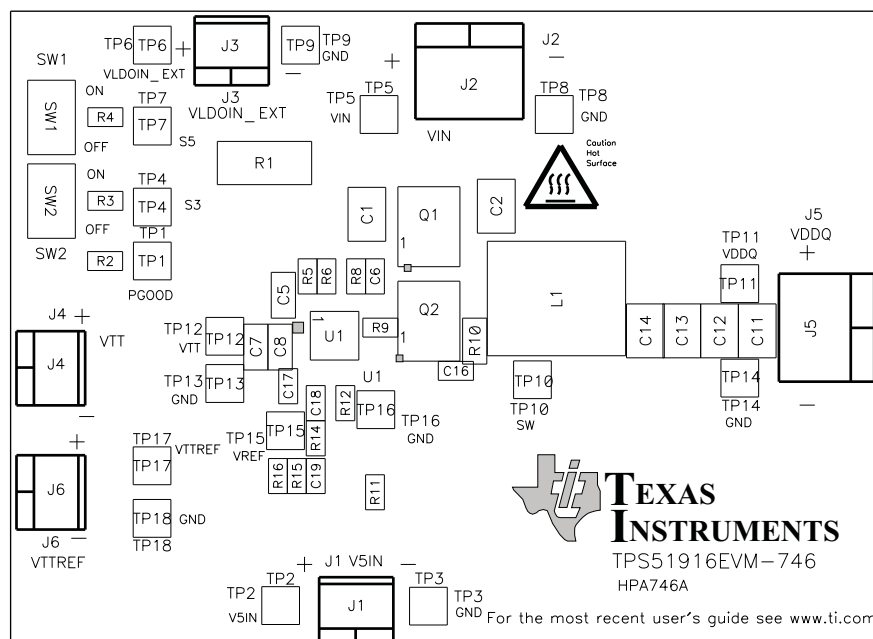


Figure 23. TPS51916EVM-746 Top Layer Assembly Drawing

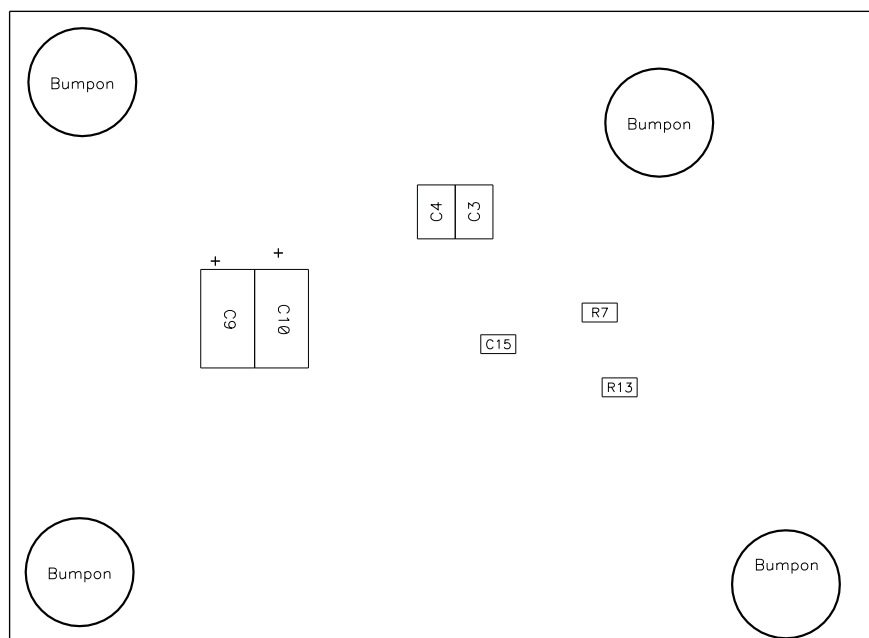


Figure 24. TPS51916EVM-746 Bottom Assembly Drawing

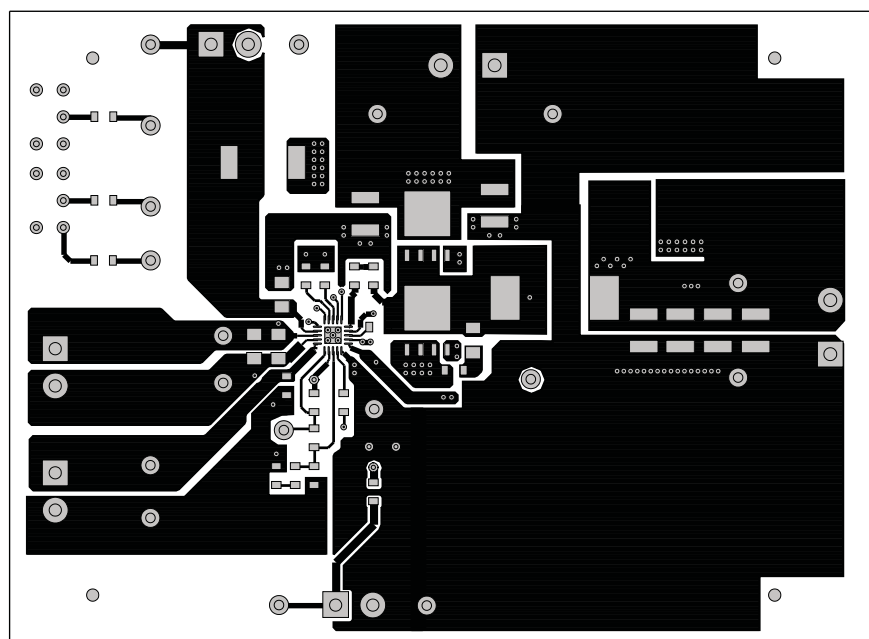
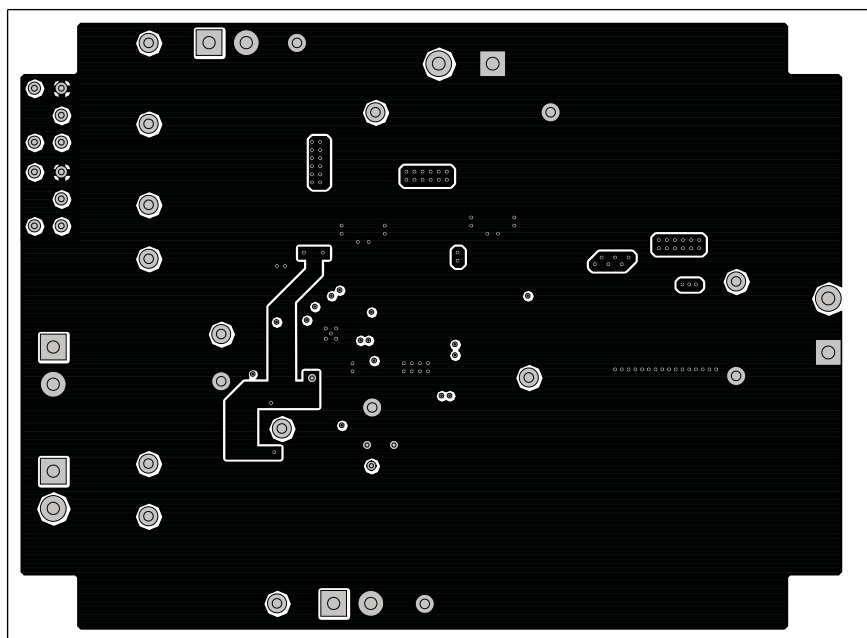
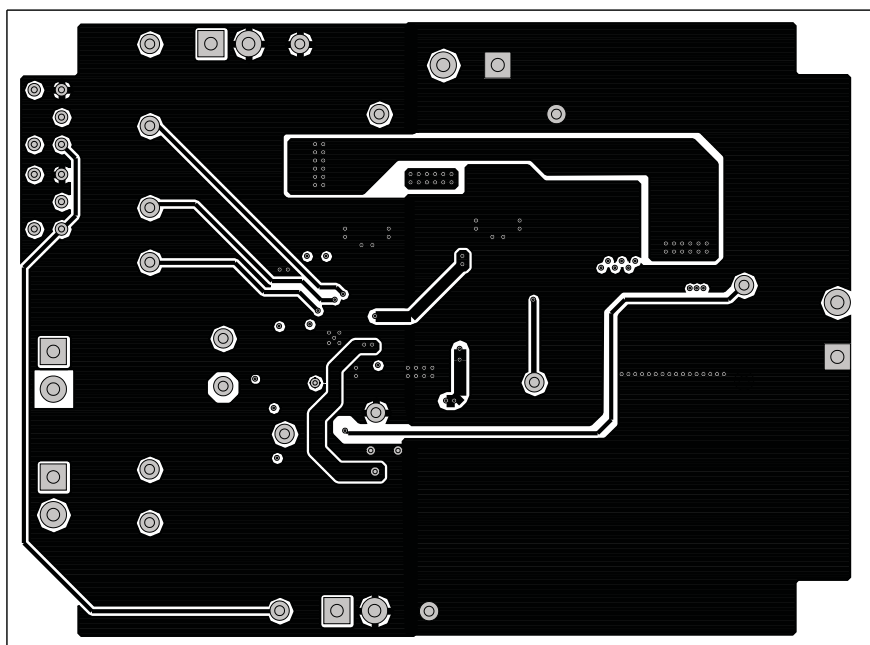


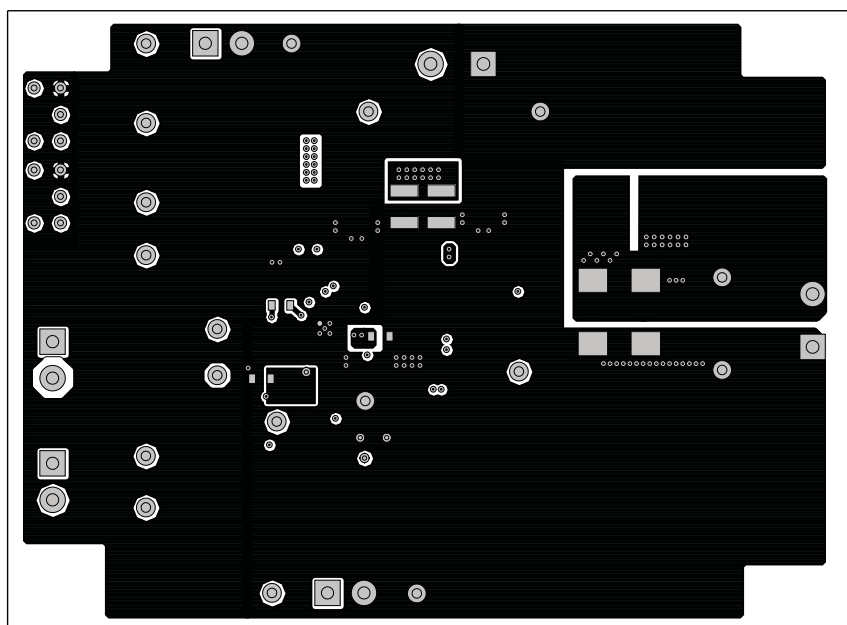
Figure 25. TPS51916EVM-746 Top Copper



**Figure 26. TPS51916EVM-746 Layer-2 Copper**



**Figure 27. TPS51916EVM-746 Layer-3 Copper**



**Figure 28. TPS51916EVM-746 Bottom Copper**

## 9 Bill of Materials

**Table 4. TPS51916EVM-746 Bill of Materials**

| QTY | REFDES                    | DESCRIPTION                                                       | MFR       | PART NUMBER        |
|-----|---------------------------|-------------------------------------------------------------------|-----------|--------------------|
| 2   | C1, C2                    | Capacitor, Ceramic, 22 $\mu$ F, 25V, X5R, 20%, 1210               | MURATA    | GRM32ER61C226KE20L |
| 4   | C11, C12, C13, C14        | Capacitor, Ceramic, 100 $\mu$ F, 6.3V, X5R, 20%, 1210             | MURATA    | GRM32ER60J107ME20L |
| 1   | C15                       | Capacitor, Ceramic, 1 $\mu$ F, 25V, X7R, 20%, 0603                | STD       | STD                |
| 1   | C16                       | Capacitor, Ceramic, 1000 pF, 50V, X7R, 20%, 0603                  | STD       | STD                |
| 1   | C17                       | Capacitor, Ceramic, 0.22 $\mu$ F, 25V, X7R, 20%, 0603             | STD       | STD                |
| 1   | C19                       | Capacitor, Ceramic, 0.01 $\mu$ F, 25V, X7R, 20%, 0603             | STD       | STD                |
| 2   | C5, C8                    | Capacitor, Ceramic, 10 $\mu$ F, 10V, X5R, 20%, 0805               | STD       | STD                |
| 2   | C6, C18                   | Capacitor, Ceramic, 0.1 $\mu$ F, 50V, X7R, 20%, 0603              | STD       | STD                |
| 1   | Q1                        | MOSFET, N-ch, 30V, 21A, 4.5 m $\Omega$                            | TI        | CSD17310Q5A        |
| 1   | Q2                        | MOSFET, N-ch, 30V, 32A, 2.0 m $\Omega$                            | TI        | CSD17303Q5         |
| 1   | L1                        | Inductor, SMT, 0.56 $\mu$ H, 21A, 1.56 m $\Omega$ , 0.510"x0.520" | Panasonic | ETQP4LR56WFC       |
| 1   | R1                        | Resistor, Chip, 0, 1W, 1%, 2512                                   | STD       | STD                |
| 1   | R10                       | Resistor, Chip, 3.01, 1/16W, 1%, 0805                             | STD       | STD                |
| 1   | R14                       | Resistor, Chip, 10.0k, 1/16W, 1%, 0603                            | STD       | STD                |
| 1   | R15                       | Resistor, Chip, 47.5k, 1/16W, 1%, 0603                            | STD       | STD                |
| 1   | R16                       | Resistor, Chip, 2.00k, 1/16W, 1%, 0603                            | STD       | STD                |
| 1   | R2                        | Resistor, Chip, 100k, 1/16W, 1%, 0603                             | STD       | STD                |
| 1   | R5                        | Resistor, Chip, 1.00k, 1/16W, 1%, 0603                            | STD       | STD                |
| 1   | R6                        | Resistor, Chip, 44.2k, 1/16W, 1%, 0603                            | STD       | STD                |
| 1   | R8                        | Resistor, Chip, 4.87, 1/16W, 1%, 0603                             | STD       | STD                |
| 1   | R9                        | Resistor, Chip, 1, 1/16W, 1%, 0603                                | STD       | STD                |
| 6   | R3, R4, R7, R11, R12, R13 | Resistor, Chip, 0, 1/16W, 1%, 0603                                | STD       | STD                |
| 1   | U1                        | IC, Complete DDR2, DDR3 and DDR3L Memory Power Solution, RUK-20   | TI        | TPS51916RUK        |

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 80°C. The EVM is designed to operate properly with certain components above 80°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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