

## FEATURES

- Power-Supply Voltage Range: 2.2 V to 5 V
- Low Supply Current: 930  $\mu$ A/Amplifier at 2.2 V
- High Unity-Gain Bandwidth: 10 MHz
- Rail-to-Rail Output Swing
  - 600- $\Omega$  Load: 120 mV From Either Rail at 2.2 V
  - 2-k $\Omega$  Load: 50 mV From Either Rail at 2.2 V
- Input Common-Mode Voltage Range Includes Ground
- Input Voltage Noise: 9 nV/ $\sqrt{\text{Hz}}$  at f = 1 kHz

## APPLICATIONS

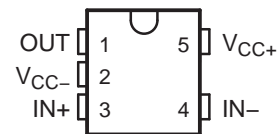
- Cellular and Cordless Phones
- Active Filter and Buffers
- Laptops and PDAs
- Battery Powered Electronics

## DESCRIPTION/ORDERING INFORMATION

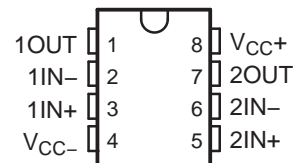
The LMV721 (single) and LMV722 (dual) are low-noise low-voltage low-power operational amplifiers that can be designed into a wide range of applications. The LMV721 and LMV722 have a unity-gain bandwidth of 10 MHz, a slew rate of 5 V/ $\mu$ s, and a quiescent current of 930  $\mu$ A/amplifier at 2.2 V.

The LMV721 and LMV722 are designed to provide optimal performance in low-voltage and low-noise systems. They provide rail-to-rail output swing into heavy loads. The input common-mode voltage range includes ground, and the maximum input offset voltage are 3.5 mV (over recommended temperature range) for the devices. Their capacitive load capability is also good at low supply voltages. The operating range is from 2.2 V to 5.5 V.

LMV721...DBV or DCK PACKAGE  
(TOP VIEW)



LMV722...D, DGK, OR DRG PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>	
–40°C to 85°C	Single	SC-70 – DCK	Reel of 3000	LMV721IDCKR	RK_
			Reel of 250	LMV721IDCKT	
		SOT-23 – DBV	Reel of 3000	LMV721IDBVR	RBF_
	Dual	SOIC – D	Reel of 2500	LMV722IDR	MV722I
			Tube of 75	LMV722ID	
		VSSOP – DGK	Reel of 2500	LMV722IDGKR	R6_
	QFN – DRG	Reel of 2500	LMV722IDRGR	ZYY	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DBV/DCK/DGK: The actual top-side marking has one additional character that designates the assembly/test site.



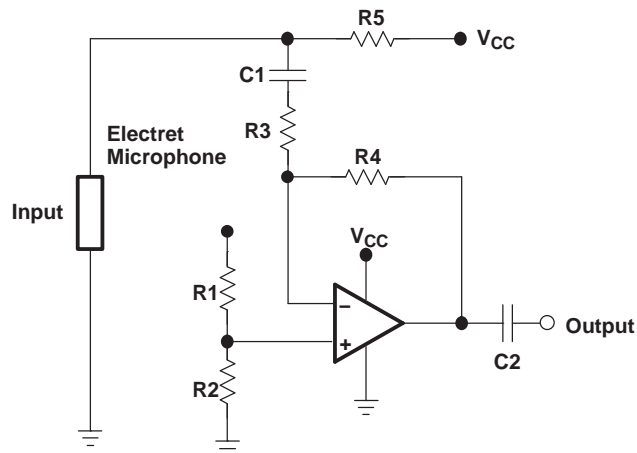
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# LMV721, LMV722

## 10-MHz LOW-NOISE LOW-VOLTAGE LOW-POWER OPERATIONAL AMPLIFIERS

SLOS470A–JUNE 2005–REVISED AUGUST 2006

### Typical Application



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage <sup>(2)</sup>		5.5	V
$V_{ID}$	Differential input voltage <sup>(3)</sup>	±Supply voltage		V
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	D package <sup>(5)</sup>	97	°C/W
		DBV package <sup>(5)</sup>	206	
		DCK package <sup>(5)</sup>	252	
		DGK package <sup>(5)</sup>	172	
		DRG package <sup>(6)</sup>	50.7	
$T_J$	Operating virtual-junction temperature		150	°C
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and  $V_{CC}$  specified for the measurement of  $I_{OS}$ ) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.
- (6) The package thermal impedance is calculated in accordance with JESD 51-5.

### Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage	2.2	5	V
$T_J$	Operating virtual-junction temperature	-40	85	°C

### ESD Protection

		TYP	UNIT
Human-Body Model		2000	V
Machine Model		100	V

**Electrical Characteristics**
 $V_{CC+} = 2.2\text{ V}$ ,  $V_{CC-} = \text{GND}$ ,  $V_{ICR} = V_{CC+}/2$ ,  $V_O = V_{CC+}/2$ , and  $R_L > 1\text{ M}\Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_J$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage		25°C		0.02	3	mV
			–40°C to 85°C			3.5	
$TCV_{IO}$	Input offset voltage average drift		25°C		0.6		$\mu\text{V}/^\circ\text{C}$
$I_{IB}$	Input bias current		25°C		260		nA
$I_{IO}$	Input offset current		25°C		25		nA
CMMR	Common-mode rejection ratio	$V_{ICR} = 0\text{ V to }1.3\text{ V}$	25°C	70	88		dB
			–40°C to 85°C	64			
PSRR	Power-supply rejection ratio	$V_{CC+} = 2.2\text{ V to }5\text{ V}$ , $V_O = 0$ , $V_{ICR} = 0$	25°C	80	90		dB
			–40°C to 85°C	70			
$V_{ICR}$	Input common-mode voltage	CMRR $\geq 50\text{ dB}$	25°C		–0.3		V
						0.3	
$A_{VD}$	Large-signal voltage gain	$R_L = 600\ \Omega$ , $V_O = 0.75\text{ V to }2\text{ V}$	25°C	75	81		dB
			–40°C to 85°C	70			
		$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V to }2.1\text{ V}$	25°C	75	84		
			–40°C to 85°C	70			
$V_O$	Output swing	$R_L = 600\ \Omega\text{ to }V_{CC+}/2$	25°C	2.090	2.125		V
			–40°C to 85°C	2.065			
			25°C		0.071	0.120	
			–40°C to 85°C			0.145	
		$R_L = 2\text{ k}\Omega\text{ to }V_{CC+}/2$	25°C	2.150	2.177		
			–40°C to 85°C	2.125			
$I_O$	Output current	Sourcing, $V_O = 0\text{ V}$ , $V_{IN(\text{diff})} = \pm 0.5\text{ V}$	25°C	10	14.9		mA
			–40°C to 85°C	5			
		Sinking, $V_O = 2.2\text{ V}$ , $V_{IN(\text{diff})} = \pm 0.5\text{ V}$	25°C	10	17.6		
			–40°C to 85°C	5			
$I_{CC}$	Supply current	LMV721	25°C		0.93	1.3	mA
			–40°C to 85°C			1.5	
		LMV722	25°C		1.81	2.4	
			–40°C to 85°C			2.6	
SR	Slew rate <sup>(1)</sup>		25°C		4.9		V/ $\mu\text{s}$
GBW	Gain bandwidth product		25°C		10		MHz
$\Phi_m$	Phase margin		25°C		67.4		°
$G_m$	Gain margin		25°C		–9.8		dB
$V_n$	Input-referred voltage noise	$f = 1\text{ kHz}$	25°C		9		$\text{nV}/\sqrt{\text{Hz}}$
$I_n$	Input-referred current noise	$f = 1\text{ kHz}$	25°C		0.3		$\text{pA}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$f = 1\text{ kHz}$ , $A_V = 1$ , $R_L = 600\ \Omega$ , $V_O = 500\text{ mV}_{pp}$	25°C		0.004		%

(1) Connected as voltage follower with 1-V step input. Number specified is the slower of the positive and negative slew rate.

# LMV721, LMV722

## 10-MHz LOW-NOISE LOW-VOLTAGE LOW-POWER OPERATIONAL AMPLIFIERS

SLOS470A–JUNE 2005–REVISED AUGUST 2006

### Electrical Characteristics

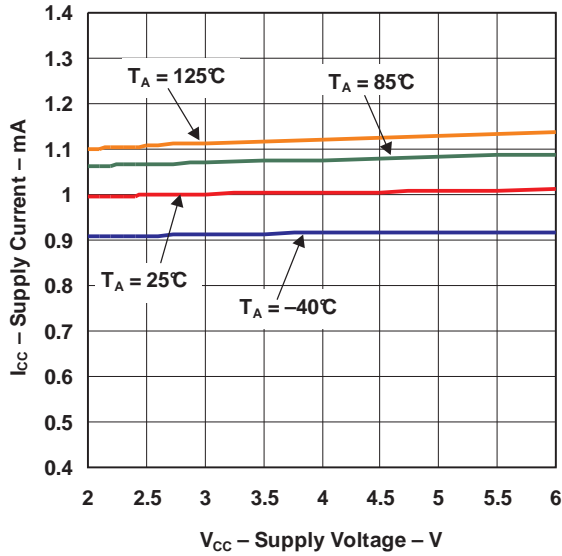
$V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = \text{GND}$ ,  $V_{ICR} = V_{CC+}/2$ ,  $V_O = V_{CC+}/2$ , and  $R_L > 1\text{ M}\Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_J$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage		25°C	-0.08	3		mV
			-40°C to 85°C		3.5		
$TCV_{IO}$	Input offset voltage average drift		25°C		0.6		$\mu\text{V}/^\circ\text{C}$
$I_{IB}$	Input bias current		25°C		260		nA
$I_{IO}$	Input offset current		25°C		25		nA
CMMR	Common-mode rejection ratio	$V_{ICR} = 0\text{ V to }1.3\text{ V}$	25°C	80	89		dB
			-40°C to 85°C	75			
PSRR	Power-supply rejection ratio	$V_{CC+} = 2.2\text{ V to }5\text{ V}$ , $V_O = 0$ , $V_{ICR} = 0$	25°C	70	90		dB
			-40°C to 85°C	64			
$V_{ICR}$	Input common-mode voltage	CMRR $\geq 50\text{ dB}$	25°C		-0.3		V
					4.1		
$A_{VD}$	Large-signal voltage gain	$R_L = 600\ \Omega$ , $V_O = 0.75\text{ V to }4.8\text{ V}$	25°C	80	87		dB
			-40°C to 85°C	70			
		$R_L = 2\text{ k}\Omega$ , $V_O = 0.7\text{ V to }4.9\text{ V}$	25°C	80	94		
			-40°C to 85°C	70			
$V_O$	Output swing	$R_L = 600\ \Omega\text{ to }V_{CC+}/2$	25°C	4.84	4.882		V
			-40°C to 85°C	4.815			
			25°C		0.134	0.19	
			-40°C to 85°C			0.215	
		$R_L = 2\text{ k}\Omega\text{ to }V_{CC+}/2$	25°C	4.93	4.952		
			-40°C to 85°C	4.905			
$I_O$	Output current	Sourcing, $V_O = 0\text{ V}$ , $V_{IN(\text{diff})} = \pm 0.5\text{ V}$	25°C	20	52.6		mA
			-40°C to 85°C	12			
		Sinking, $V_O = 2.2\text{ V}$ , $V_{IN(\text{diff})} = \pm 0.5\text{ V}$	25°C	15	23.7		
			-40°C to 85°C	8.5			
$I_{CC}$	Supply current	LMV721	25°C		1.03	1.4	mA
			-40°C to 85°C			1.7	
		LMV722	25°C		2.01	2.4	
			-40°C to 85°C			2.8	
SR	Slew rate <sup>(1)</sup>		25°C		5.25		V/ $\mu\text{s}$
GBW	Gain bandwidth product		25°C		10		MHz
$\Phi_m$	Phase margin		25°C		72		°
$G_m$	Gain margin		25°C		-11		dB
$V_n$	Input-referred voltage noise	$f = 1\text{ kHz}$	25°C		8.5		$\text{nV}/\sqrt{\text{Hz}}$
$I_n$	Input-referred current noise	$f = 1\text{ kHz}$	25°C		0.2		$\text{pA}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$f = 1\text{ kHz}$ , $AV = 1$ , $R_L = 600\ \Omega$ , $V_O = 500\text{ mV}_{pp}$	25°C		0.001		%

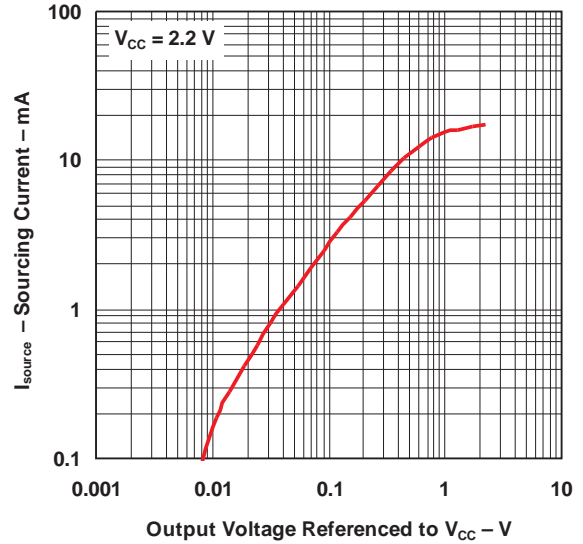
(1) Connected as voltage follower with 1-V step input. Number specified is the slower of the positive and negative slew rate.

**TYPICAL CHARACTERISTICS**

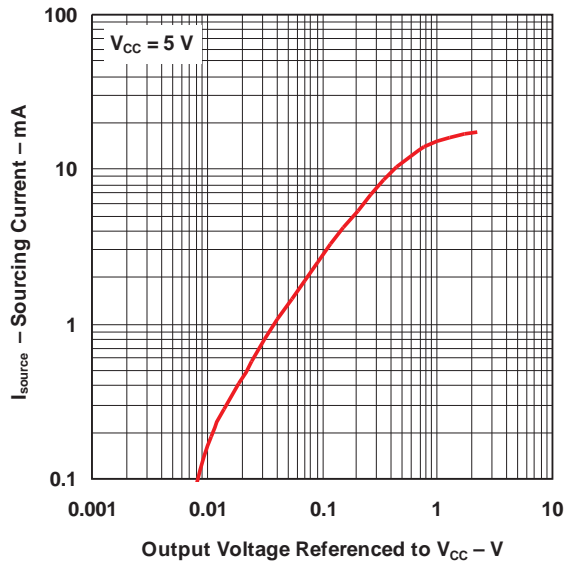
**SUPPLY CURRENT  
VS  
SUPPLY VOLTAGE**



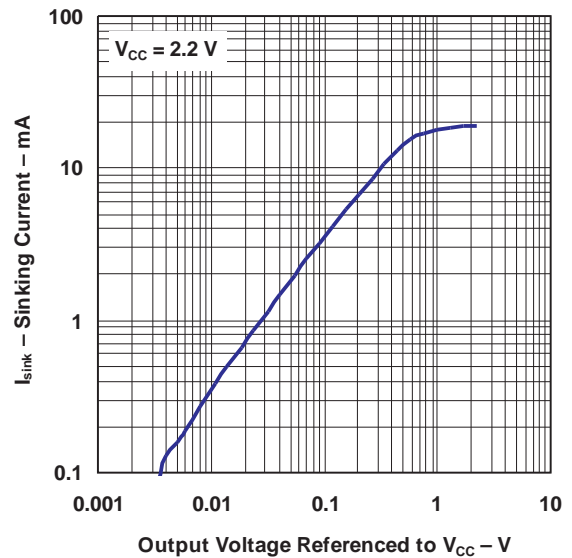
**SOURCING CURRENT  
VS  
OUTPUT VOLTAGE**



**SOURCING CURRENT  
VS  
OUTPUT VOLTAGE**

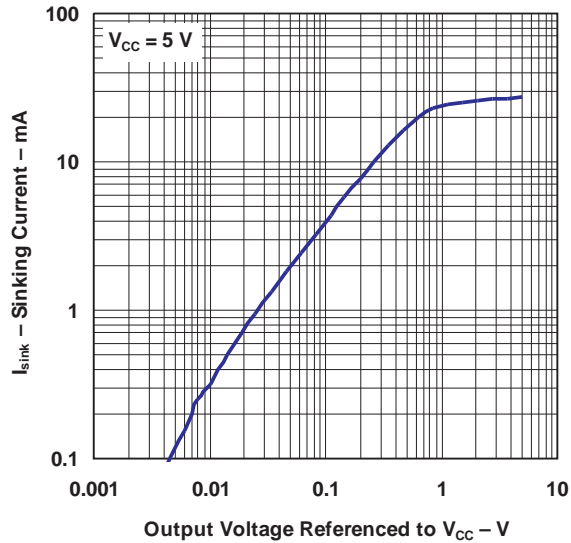


**SINKING CURRENT  
VS  
OUTPUT VOLTAGE**

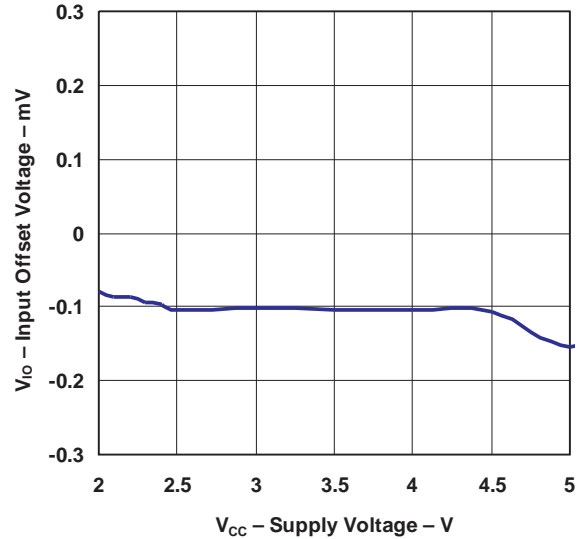


TYPICAL CHARACTERISTICS (continued)

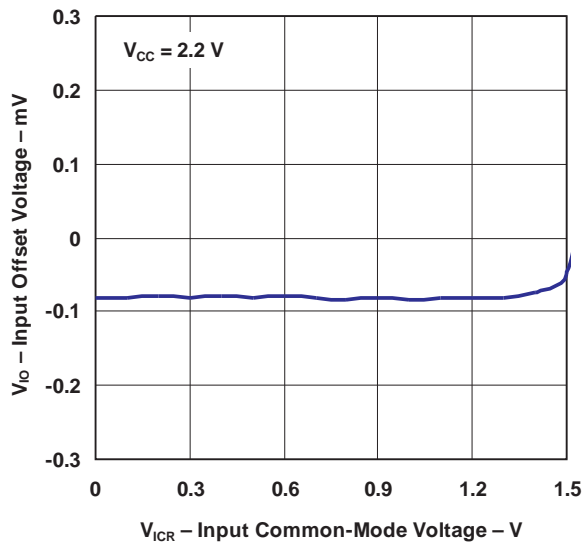
SINKING CURRENT  
 VS  
 OUTPUT VOLTAGE



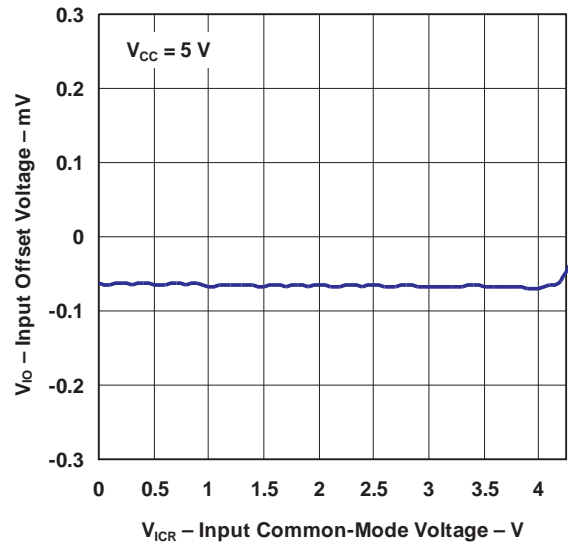
OUTPUT VOLTAGE SWING  
 VS  
 SUPPLY VOLTAGE



INPUT OFFSET VOLTAGE  
 VS  
 INPUT COMMON-MODE VOLTAGE

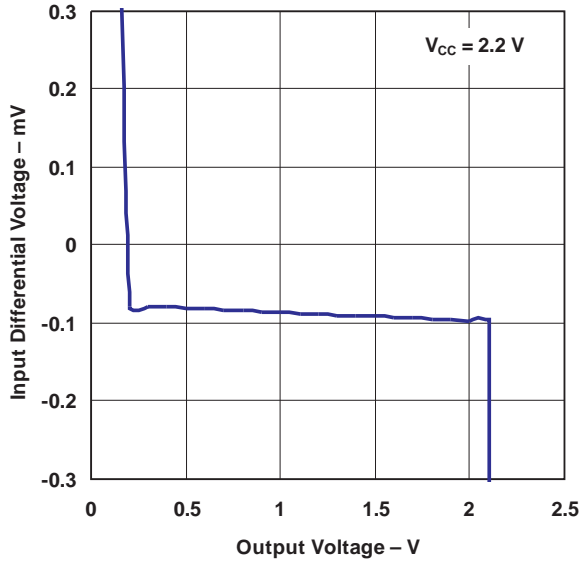


INPUT OFFSET VOLTAGE  
 VS  
 INPUT COMMON-MODE VOLTAGE

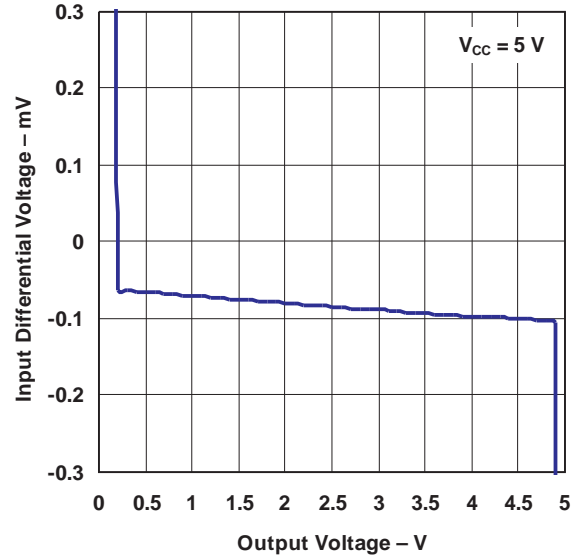


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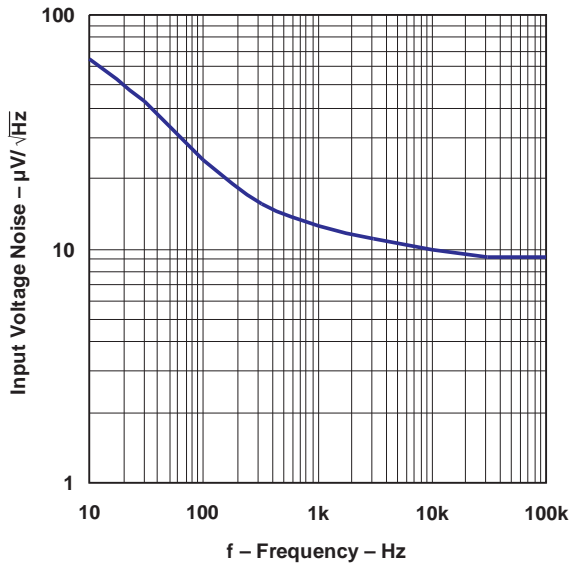
**INPUT VOLTAGE**  
**vs**  
**OUTPUT VOLTAGE**



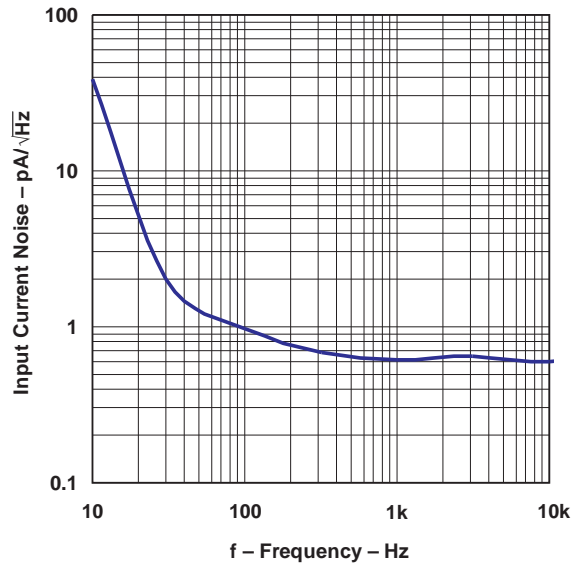
**INPUT VOLTAGE**  
**vs**  
**OUTPUT VOLTAGE**



**INPUT VOLTAGE NOISE**  
**vs**  
**FREQUENCY**

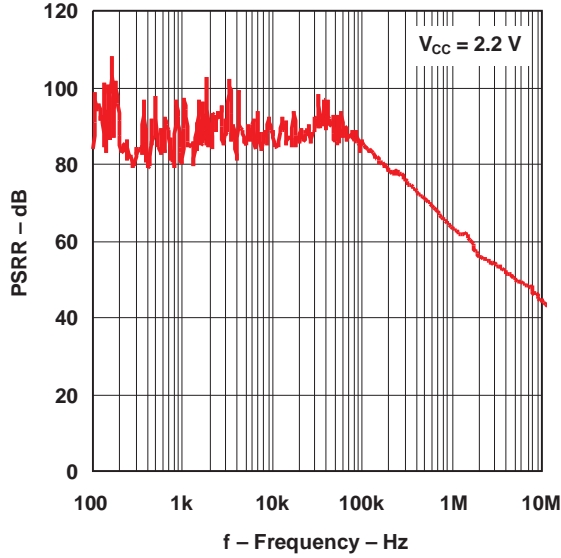


**INPUT CURRENT NOISE**  
**vs**  
**FREQUENCY**

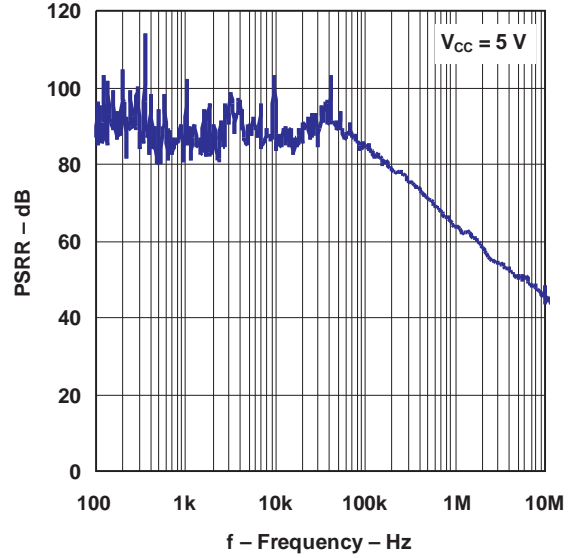


TYPICAL CHARACTERISTICS (continued)

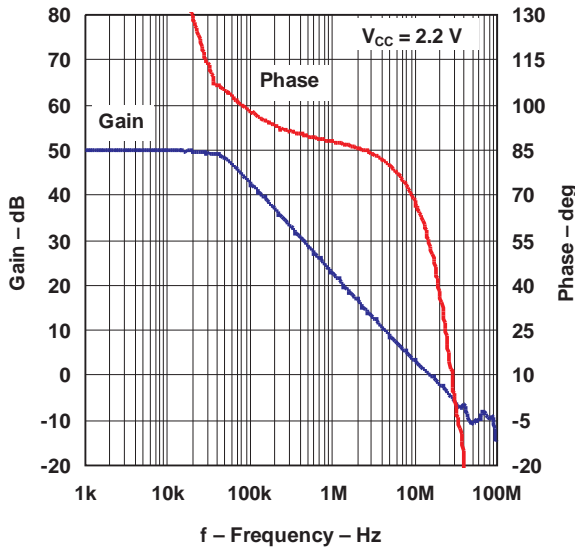
PSRR  
 VS  
 FREQUENCY



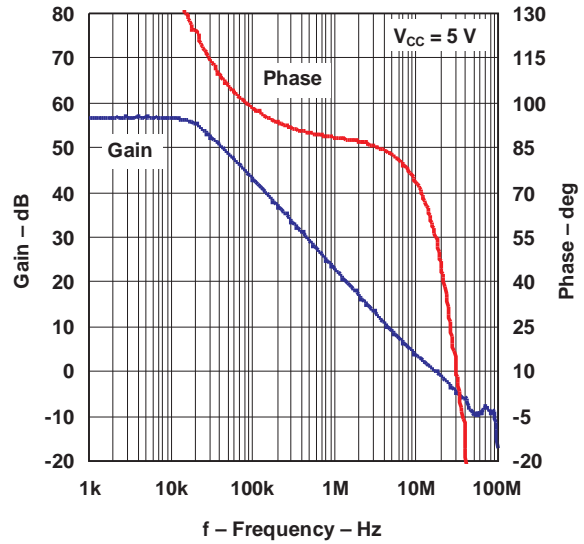
PSRR  
 VS  
 FREQUENCY



GAIN AND PHASE  
 VS  
 FREQUENCY



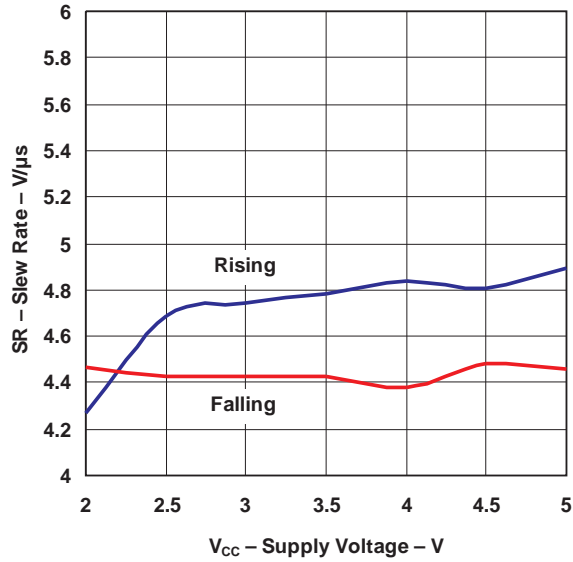
GAIN AND PHASE  
 VS  
 FREQUENCY



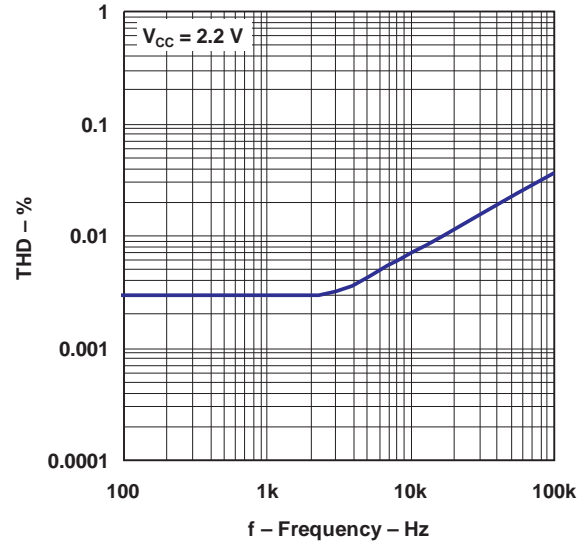


**TYPICAL CHARACTERISTICS (continued)**

**SLEW RATE  
VS  
SUPPLY VOLTAGE**

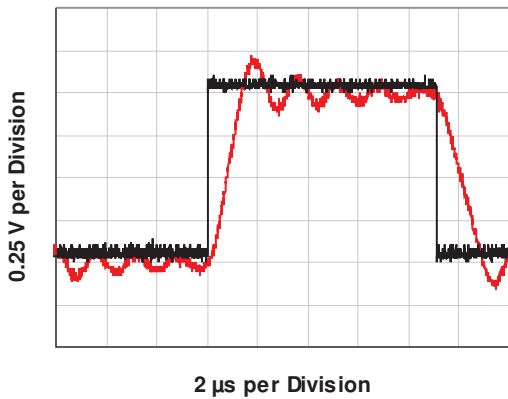


**THD  
VS  
FREQUENCY**



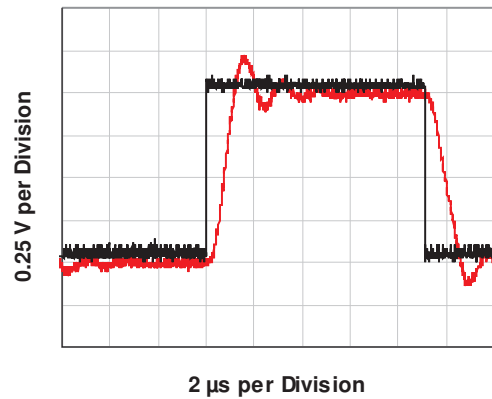
**PULSE RESPONSE**

$V_{CC} = 5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ ,  $C_L = 21.2\text{ nF}$ ,  $R_o = 0\ \Omega$



**PULSE RESPONSE**

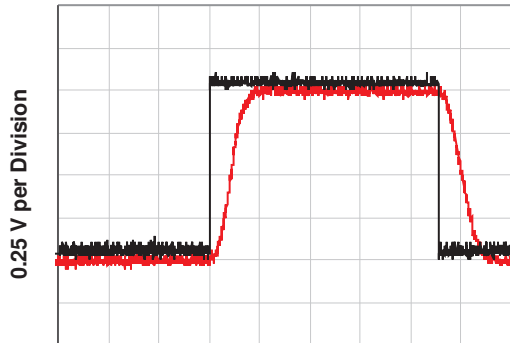
$V_{CC} = 5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ ,  $C_L = 21.2\text{ nF}$ ,  $R_o = 2.1\ \Omega$



TYPICAL CHARACTERISTICS (continued)

PULSE RESPONSE

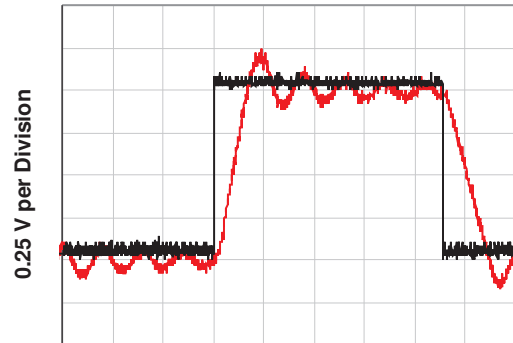
$V_{cc} = 5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ ,  $C_L = 21.2\text{ nF}$ ,  $R_o = 9.5\ \Omega$



2  $\mu\text{s}$  per Division

PULSE RESPONSE

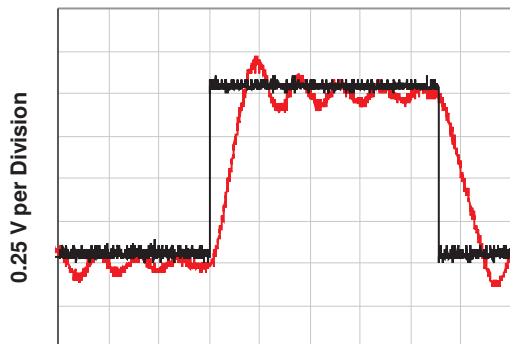
$V_{cc} = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 21.2\text{ nF}$ ,  $R_o = 0\ \Omega$



2  $\mu\text{s}$  per Division

PULSE RESPONSE

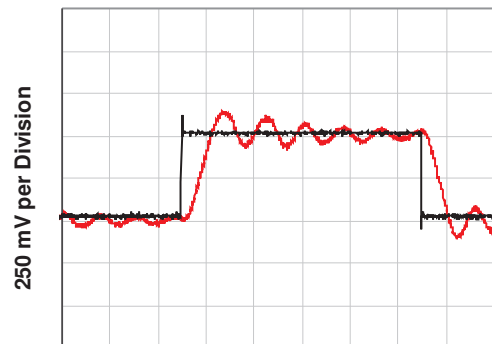
$V_{cc} = 5\text{ V}$ ,  $R_L = 600\ \Omega$ ,  $C_L = 21.2\text{ nF}$ ,  $R_o = 0\ \Omega$



2  $\mu\text{s}$  per Division

PULSE RESPONSE

$V_{cc} = 2.2\text{ V}$ ,  $R_L = 2\ \Omega$ ,  $C_L = 2.12\text{ nF}$ ,  $R_o = 0\ \Omega$

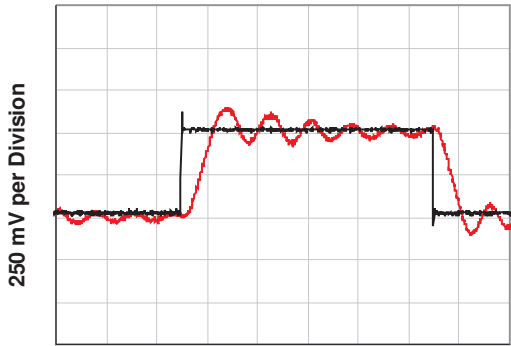


1  $\mu\text{s}$  per Division

**TYPICAL CHARACTERISTICS (continued)**

**PULSE RESPONSE**

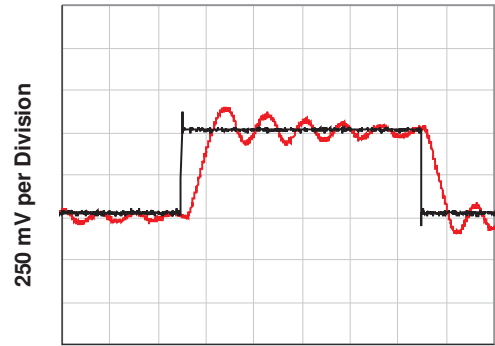
$V_{CC} = 2.2\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ ,  $C_L = 2.12\text{ nF}$ ,  $R_o = 0\ \Omega$



1  $\mu\text{s}$  per Division

**PULSE RESPONSE**

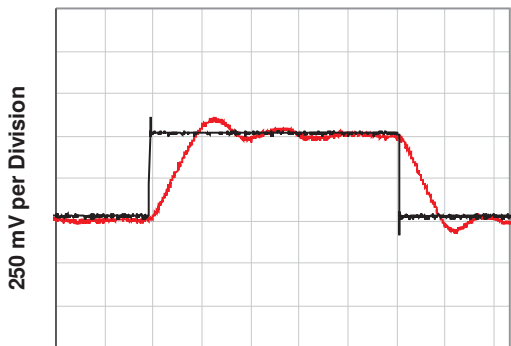
$V_{CC} = 2.2\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 2.12\text{ nF}$ ,  $R_o = 0\ \Omega$



1  $\mu\text{s}$  per Division

**PULSE RESPONSE**

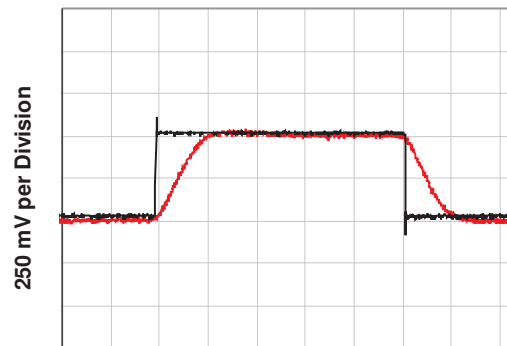
$V_{CC} = 2.2\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 2.12\text{ nF}$ ,  $R_o = 2.2\ \Omega$



1  $\mu\text{s}$  per Division

**PULSE RESPONSE**

$V_{CC} = 2.2\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 2.12\text{ nF}$ ,  $R_o = 11.5\ \Omega$

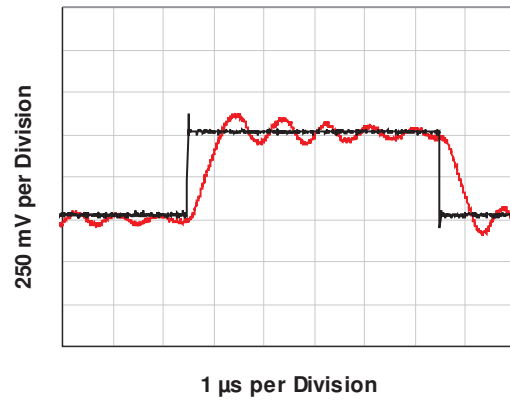


1  $\mu\text{s}$  per Division

TYPICAL CHARACTERISTICS (continued)

PULSE RESPONSE

$$V_{CC} = 2.2 \text{ V}, R_L = 600 \ \Omega, C_L = 1.89 \text{ nF}, R_o = 0 \ \Omega$$



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
LMV721IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV721IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV721IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV721IDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV721IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV721IDCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV722ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV722IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV722IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV722IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV722IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV722IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

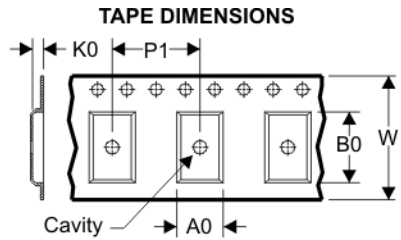
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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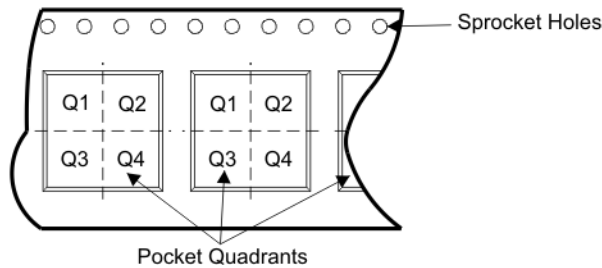
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**TAPE AND REEL BOX INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV721IDBVR	DBV	5	SITE 35	180	9	3.23	3.17	1.37	4	8	Q3
LMV721IDBVR	DBV	5	SITE 45	0	0	3.23	3.17	1.37	4	8	Q3
LMV721IDCKR	DCK	5	SITE 35	180	9	2.24	2.34	1.22	4	8	Q3
LMV721IDCKR	DCK	5	SITE 45	0	0	2.4	2.5	1.2	4	8	Q3
LMV721IDCKT	DCK	5	SITE 35	180	9	2.24	2.34	1.22	4	8	Q3
LMV721IDCKT	DCK	5	SITE 45	0	0	2.4	2.5	1.2	4	8	Q3
LMV722IDGKR	DGK	8	SITE 47	330	12	5.3	3.3	1.3	8	12	Q1
LMV722IDR	D	8	SITE 27	330	12	6.4	5.2	2.1	8	12	Q1

**TAPE AND REEL BOX DIMENSIONS**

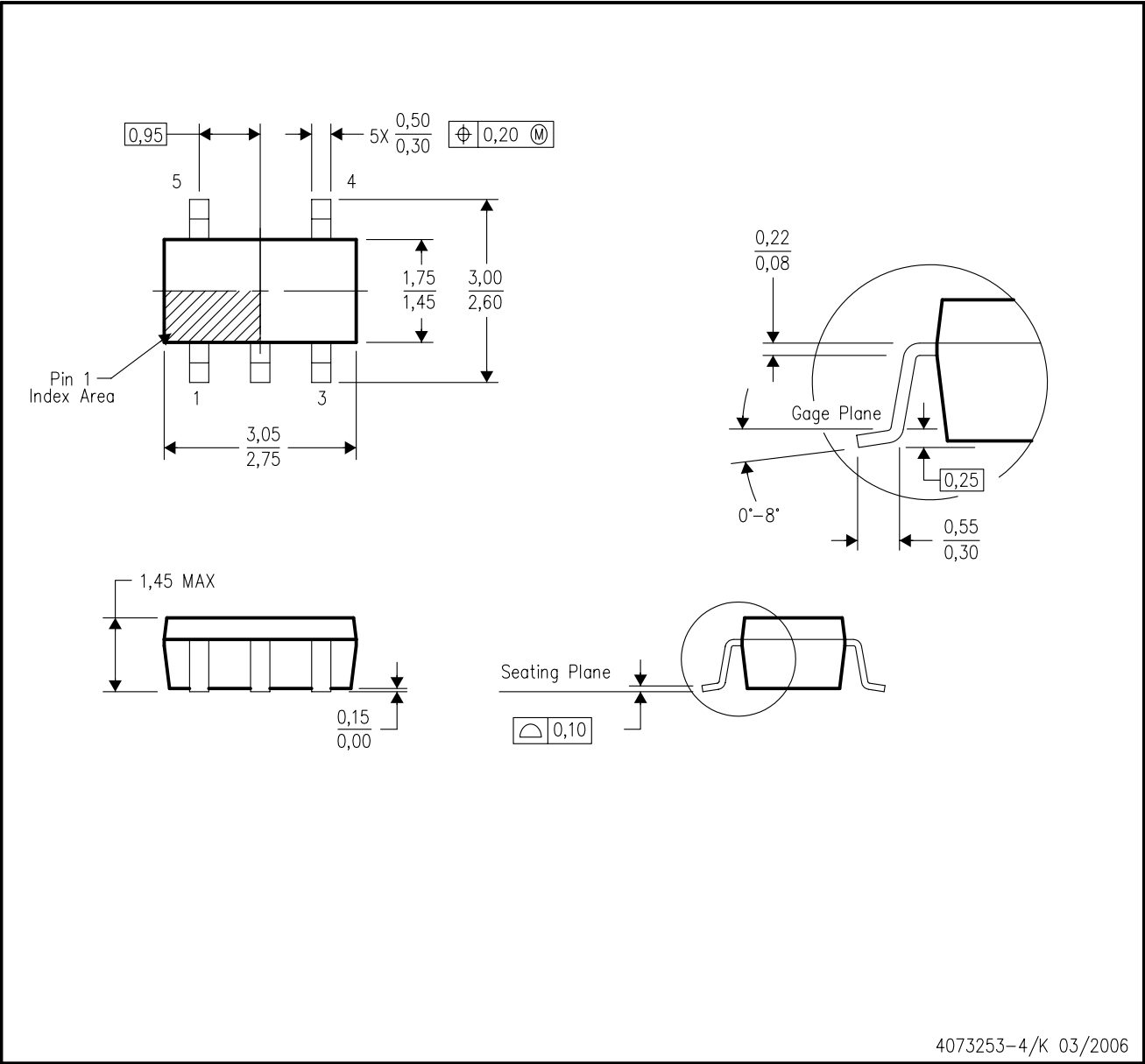


Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
LMV721IDBVR	DBV	5	SITE 35	202.0	201.0	28.0
LMV721IDBVR	DBV	5	SITE 45	0.0	185.0	220.0
LMV721IDCKR	DCK	5	SITE 35	202.0	201.0	28.0
LMV721IDCKR	DCK	5	SITE 45	0.0	185.0	220.0
LMV721IDCKT	DCK	5	SITE 35	202.0	201.0	28.0
LMV721IDCKT	DCK	5	SITE 45	0.0	185.0	220.0
LMV722IDGKR	DGK	8	SITE 47	370.0	355.0	55.0
LMV722IDR	D	8	SITE 27	342.9	338.1	20.64



DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DGK (S-PDSO-G8)

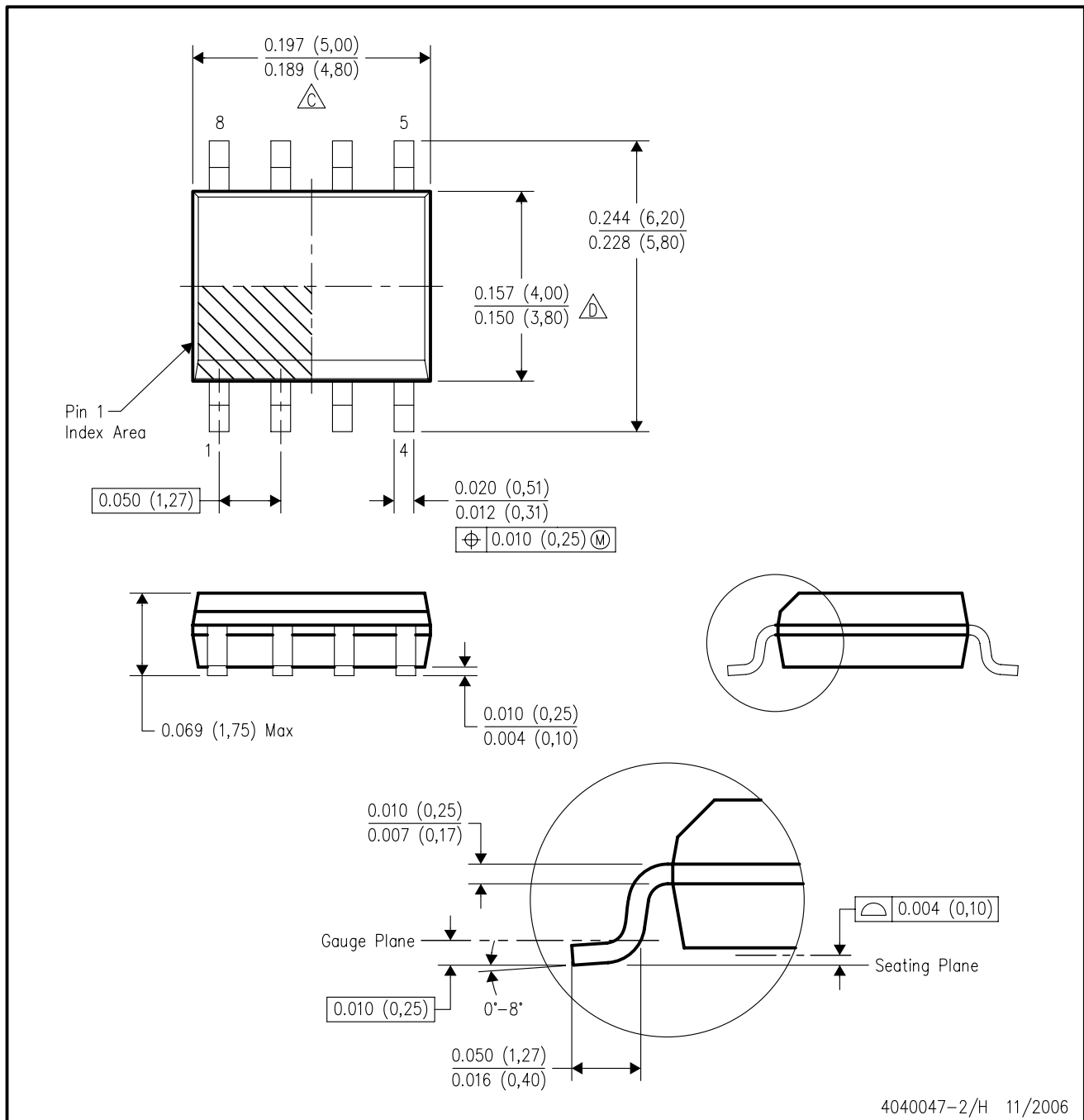
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AA.

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