Low-Power, Low-Noise, 16-Bit, Analog-to-Digital Converter for Small-Signal Sensors

Check for Samples: ADS1120

FEATURES

- **Low Current Consumption: As Low as 120 µA (typ) in Duty-Cycle Mode**
- **Wide Supply Range: 2.3 V to 5.5 V**
- **Programmable Gain: 1 V/V to 128 V/V**
- **Programmable Data Rates: Up to 2 kSPS**
- **16-Bit Noise-Free Resolution at 20 SPS**
- **Simultaneous 50-Hz and 60-Hz Rejection at 20 SPS with Single-Cycle Settling Digital Filter**
- **Dual-Matched Programmable Current Sources: 50 µA to 1500 µA**
- **Internal 2.048-V Reference: 5 ppm/°C (typ) Drift**
- **Internal 2% Accurate Oscillator**
- **Internal Temperature Sensor: 0.5°C (typ) Accuracy**
- **Two Differential or Four Single-Ended Inputs**
- **SPI™-Compatible Interface**
- **Package: 3,5-mm × 3,5-mm × 0,9-mm QFN**

APPLICATIONS

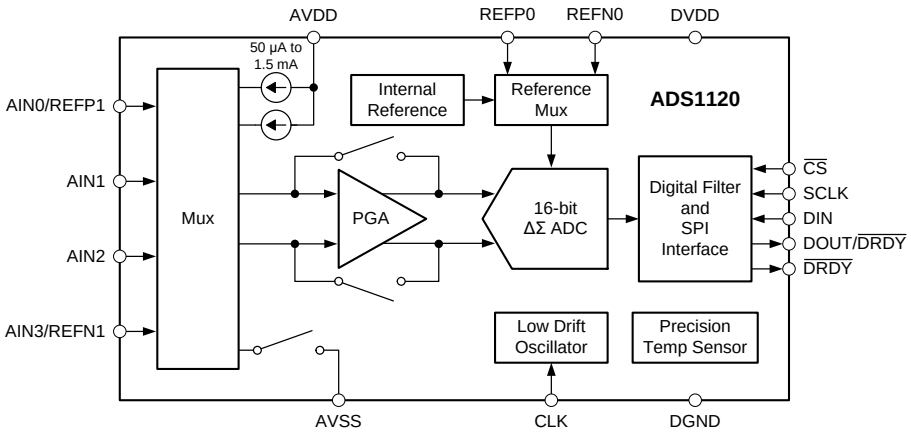
- **Temperature Sensors:**
  - **Thermocouples**
  - **Resistance Temperature Detectors (RTDs) 2-, 3-, or 4-Wire Types**
- **Bridge Sensors**
- **Portable Instrumentation**
- **Factory Automation and Process Controls**

DESCRIPTION

The ADS1120 is a precision, 16-bit, analog-to-digital converter (ADC) that offers many integrated features to reduce system cost and component count in applications measuring small sensor signals. The device features two differential or four single-ended inputs through a flexible input multiplexer (mux), a low-noise, programmable gain amplifier (PGA), two programmable excitation current sources, a voltage reference, an oscillator, a low-side switch, and a precision temperature sensor.

The device can perform conversions at data rates up to 2000 samples-per-second (SPS) with single-cycle settling. At 20 SPS, the digital filter offers simultaneous 50-Hz and 60-Hz rejection for noisy industrial applications. The internal PGA offers gains up to 128 V/V. This PGA makes the ADS1120 ideally-suited for applications measuring small sensor signals, such as resistance temperature detectors (RTDs), thermocouples, thermistors, and bridge sensors. The device supports measurements of pseudo- or fully-differential signals when using the PGA. Alternatively, the device can be configured to bypass the internal PGA while still providing high input impedance and gains up to 4 V/V, allowing for single-ended measurements.

The power consumption is as low as 120 µA when operating in duty-cycle mode with the PGA disabled. Communication to the device is established through a mode 1 SPI-compatible interface. The ADS1120 is offered in a leadless QFN-16 or a TSSOP-16 package and is specified over a temperature range of –40°C to +125°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Ordering Information

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

Product Family

DEVICE	RESOLUTION (Bits)	MAXIMUM GAIN	MAXIMUM SAMPLE RATE (SPS)	PACKAGE DESIGNATOR
ADS1120	16	128	2000	QFN-16
				TSSOP-16
ADS1220	24	128	2000	QFN-16
				TSSOP-16

Absolute Maximum Ratings(1)

		VALUE		UNIT
		MIN	MAX	
AVDD to AVSS		–0.3	+7	V
DVDD to DGND		–0.3	+7	V
AVSS to DGND		–2.8	+0.3	V
Analog input voltage	AIN0/REFP1, AIN1, AIN2, AIN3/REFN1, REFP0, REFN0	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	$\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, $\overline{DRDY}$, CLK	DGND – 0.3	DVDD + 0.3	V
Analog input current	Continuous	–10	+10	mA
Temperature	Maximum junction, T_{JMax}		+150	°C
	Storage, T_{STG}	–60	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	–2000	+2000	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	–500	+500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Thermal Information

THERMAL METRIC(1)		ADS1120		UNITS
		QFN (RVA)	TSSOP (PW)	
		16 PINS	16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	43.4	99.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	47.3	35.2	
θ_{JB}	Junction-to-board thermal resistance	18.4	44.3	
ψ_{JT}	Junction-to-top characterization parameter	0.6	2.4	
ψ_{JB}	Junction-to-board characterization parameter	18.4	43.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.0	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Electrical Characteristics

Minimum and maximum specifications are at T_A = –40°C to +125°C. Typical specifications are at T_A = +25°C. All specifications are at AVDD = 3.3 V, AVSS = 0 V, DVDD = 3.3 V, PGA enabled, DR = 20 SPS, and external V_{REF} = 2.5 V, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Full-scale differential input voltage range	$V_{IN} = (V_{AINP} – V_{AINN})$		$\pm V_{REF}$ / gain(2)		V
	Absolute input voltage range	PGA disabled, gain = 1 to 4	AVSS – 0.1		AVDD + 0.1	V
		Gain = 1 to 128	See the *Low-Noise PGA* section			V
V_{CM}	Common-mode input voltage range [$V_{CM} = (V_{AINP} + V_{AINN}) / 2$]	PGA disabled, gain = 1 to 4	AVSS – 0.1		AVDD + 0.1	V
		Gain = 1 to 128	See the *Low-Noise PGA* section			
	Absolute input current		See the Typical Characteristics			
	Differential input current		See the Typical Characteristics			
SYSTEM PERFORMANCE						
	Resolution (no missing codes)		16			Bits
DR	Data rate	Normal mode	20, 45, 90, 175, 330, 600, 1000			SPS
		Duty-cycle mode	5, 11.25, 22.5, 44, 82.5, 150, 250			SPS
		Turbo mode	40, 90, 180, 350, 660, 1200, 2000			SPS
	Noise (input-referred)		See the *Noise Performance* section			
INL	Integral nonlinearity	Gain = 1 to 128, V_{CM} = 0.5 AVDD, best fit(3)		8	20	ppm
V_{IO}	Offset voltage (input-referred)	PGA disabled, gain = 1 to 4, T_A = +25°C, differential inputs		±4		µV
		Gain = 1 to 128, T_A = +25°C, differential inputs		±4		µV
	Offset drift	PGA disabled, gain = 1 to 4		0.25		µV/°C
		Gain = 1 to 128, T_A = –40°C to +85°C(3)		0.08	0.3	µV/°C
		Gain = 1 to 128		0.25		µV/°C
GE	Gain error	PGA disabled, gain = 1 to 4, T_A = +25°C		±0.015%		
		Gain = 1 to 128, T_A = +25°C	–0.1%	±0.015%	0.1%	
	Gain drift	PGA disabled, gain = 1 to 4		1		ppm/°C
		Gain = 1 to 128(3)		1	4	ppm/°C
NMRR	Normal-mode rejection ratio(3)	50 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 10	105			dB
		60 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 11	105			dB
		50 Hz or 60 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 01	90			dB
CMRR	Common-mode rejection ratio	At dc and gain = 1	90	105		dB
		f_{CM} = 50 Hz, DR = 2000 SPS(3)	95	115		dB
		f_{CM} = 60 Hz, DR = 2000 SPS(3)	95	115		dB
PSRR	Power-supply rejection ratio	AVDD at dc, V_{CM} = 0.5 AVDD, gain = 1	80	105		dB
		DVDD at dc, V_{CM} = 0.5 AVDD, gain = 1(3)	100	115		dB
INTERNAL VOLTAGE REFERENCE						
	Initial accuracy	T_A = +25°C	2.045	2.048	2.051	V
	Reference drift(3)			5	40	ppm/°C
	Long-term drift	1000 hours		110		ppm
VOLTAGE REFERENCE INPUT						
V_{REF}	Reference input range	$V_{REF} = V_{REFPx} – V_{REFNx}$	0.75	2.5	AVDD	V
	Negative reference absolute input	REFNx to AVSS	AVSS – 0.1		V_{REFPx} – 0.75	V
	Positive reference absolute input	REFPx to AVSS	V_{REFNx} + 0.75		AVDD + 0.1	V
	Reference input current	REFN0 = AVSS, REFP0 = V_{REF}		±10		nA

(1) *PGA disabled* means the low-noise PGA is powered down and bypassed. Gains of 1, 2, and 4 are still possible in this case. See the *Bypassing the PGA* section for more information.
(2) Limited to [(AVDD – AVSS) – 0.4 V] / gain, when the PGA is enabled.
(3) Minimum and maximum values are ensured by design and characterization data.

Electrical Characteristics (continued)

Minimum and maximum specifications are at T_A = –40°C to +125°C. Typical specifications are at T_A = +25°C.
All specifications are at AVDD = 3.3 V, AVSS = 0 V, DVDD = 3.3 V, PGA enabled, DR = 20 SPS, and external V_{REF} = 2.5 V, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXCITATION CURRENT SOURCES (IDACs)						
	Current settings			50, 100, 250, 500, 1000, 1500		µA
	Compliance voltage	All current settings			AVDD – 0.9	V
	Accuracy	All current settings, each IDAC	–6%	±1%	6%	
	Current match	Between IDACs		±0.3%		
	Temperature drift	Each IDAC		50		ppm/°C
	Temperature drift matching	Between IDACs		10		ppm/°C
CLOCK SOURCES						
	Internal oscillator accuracy	Normal mode	–2%	±1%	2%	
	External clock	Frequency range	0.5	4.096	4.5	MHz
		Duty cycle	40%		60%	
TEMPERATURE SENSOR						
	Temperature sensor resolution	Conversion resolution		14		Bits
		Temperature resolution		0.03125		°C
	Temperature sensor accuracy	T_A = 0°C to +75°C		±0.25		°C
		T_A = –40°C to +125°C		±0.5		°C
		vs analog supply voltage		0.0625	0.25	°C/V
LOW-SIDE POWER SWITCH						
R_{ON}	On resistance			3.5		Ω
	Current through switch				30	mA
DIGITAL INPUT/OUTPUT						
V_{IH}	High-level input voltage		0.7 DVDD		DVDD	V
V_{IL}	Low-level input voltage		DGND		0.3 DVDD	V
V_{OH}	High-level output voltage	I_{OH} = 3 mA	0.8 DVDD			V
V_{OL}	Low-level output voltage	I_{OL} = 3 mA			0.2 DVDD	V
I_H	Input leakage, high	V_{IH} = 5.5 V	–10		10	µA
I_L	Input leakage, low	V_{IL} = DGND	–10		10	µA

Electrical Characteristics (continued)

Minimum and maximum specifications are at T_A = –40°C to +125°C. Typical specifications are at T_A = +25°C.
All specifications are at AVDD = 3.3 V, AVSS = 0 V, DVDD = 3.3 V, PGA enabled, DR = 20 SPS, and external V_{REF} = 2.5 V, unless otherwise noted.(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY REQUIREMENTS							
V_{DD}	Supply voltage	Digital	DVDD to DGND	2.3		5.5	V
		Analog, unipolar	AVDD to AVSS, AVSS = DGND	2.3		5.5	V
		Analog, bipolar	AVDD to DGND	2.3		2.75	V
			AVSS to DGND	–2.75		–2.3	V
I_{CC}	Supply current(4)	I_{AVDD}	Power-down mode		0.1	3	µA
			Duty-cycle mode, PGA disabled		65		µA
			Normal mode, PGA disabled		240		µA
			Normal mode, gain = 1 to 16		340	490	µA
			Normal mode, gain = 32		425		µA
			Normal mode, gain = 64, 128		510		µA
			Turbo mode, gain = 1 to 16		540		µA
		I_{DVDD}	Power-down mode		0.3	5	µA
			Duty-cycle mode		55		µA
			Normal mode		75	110	µA
			Turbo mode		95		µA
P_D	Power dissipation(4)		Duty-cycle mode, PGA disabled		0.4		mW
			Normal mode, gain = 1 to 16		1.4		mW
			Turbo mode, gain = 1 to 16		2.1		mW
TEMPERATURE RANGE							
T_{STG}	Storage temperature			–60		+150	°C
T_A	Specified ambient temperature			–40		+125	°C

(4) Internal voltage reference selected, internal oscillator enabled, both IDACs turned off.

SPI Timing Characteristics

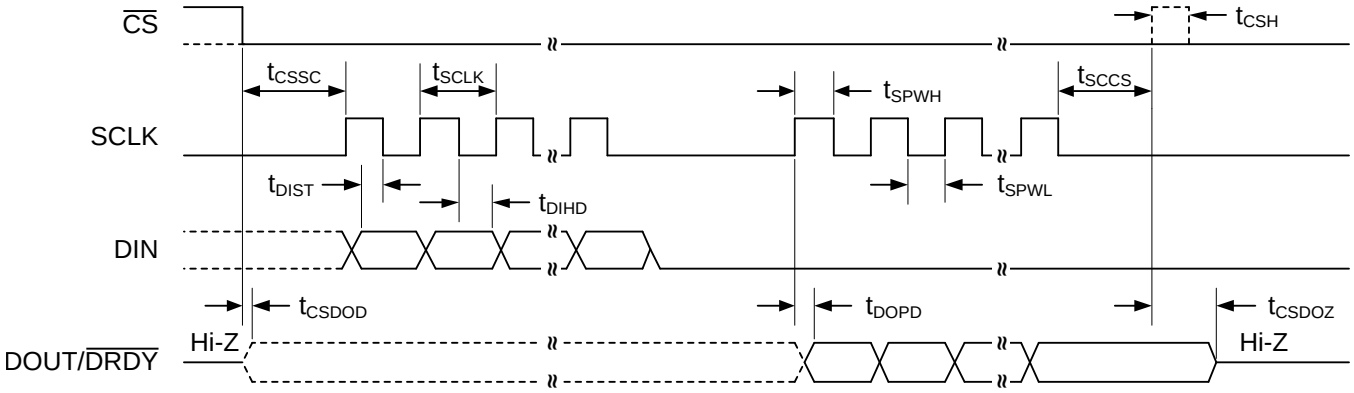


Figure 1. Serial Interface Timing

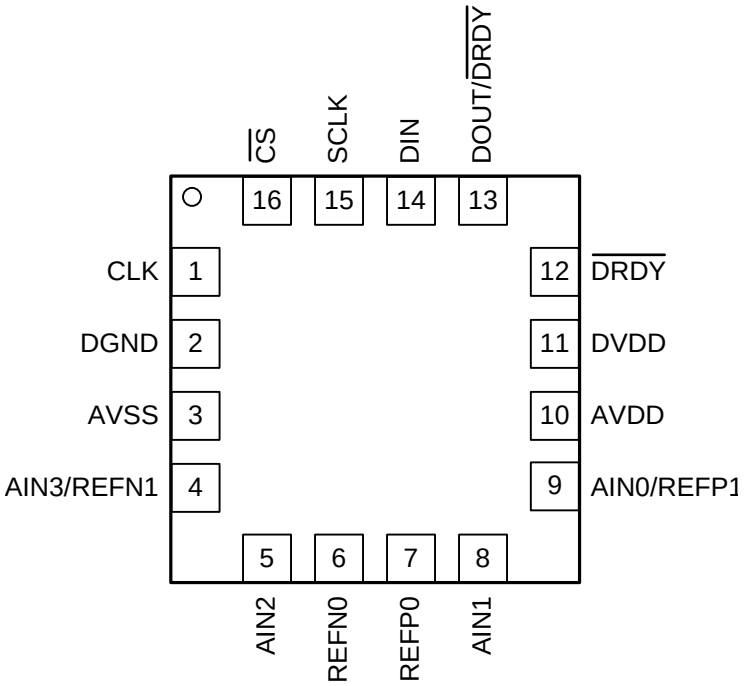
SPI Timing Characteristics(1)

PARAMETER		MIN	MAX	UNIT
t_{CSSC}	$\overline{CS}$ low to first SCLK high: setup time	50		ns
t_{SCCS}	Final SCLK falling edge to $\overline{CS}$ high	25		ns
t_{DIST}	DIN setup time	50		ns
t_{DIHD}	DIN hold time	25		ns
t_{DOPD}	SCLK rising edge to new data valid: propagation delay	0	50	ns
t_{SCLK}	SCLK period(2)	150		ns
t_{SPWH}	SCLK pulse width: high(2)	60		ns
t_{SPWL}	SCLK pulse width: low(2)	60		ns
t_{CSDOZ}	$\overline{CS}$ high to DOUT high impedance: propagation delay		50	ns
t_{CSDOD}	$\overline{CS}$ low to DOUT driven: propagation delay		50	ns
t_{CSH}	$\overline{CS}$ high pulse width	50		ns

(1) At T_A = –40°C to +125°C, DVDD = 2.3 V to 5.5 V, and DOUT load = 20 pF || 10 kΩ to DGND, unless otherwise noted.
(2) If a complete command is not sent within 13955 · t_{MOD} (normal mode, duty-cycle mode) or 27910 · t_{MOD} (turbo mode), the serial interface resets and the next SCLK pulse starts a new communication cycle.
t_{MOD} = 1 / f_{MOD}. Modulator frequency (f_{MOD}) is 256 kHz in normal and duty-cycle mode and 512 kHz in turbo mode, when using the internal oscillator or an external 4.096-MHz clock.

PIN CONFIGURATIONS

RVA PACKAGE
QFN-16
(TOP VIEW)

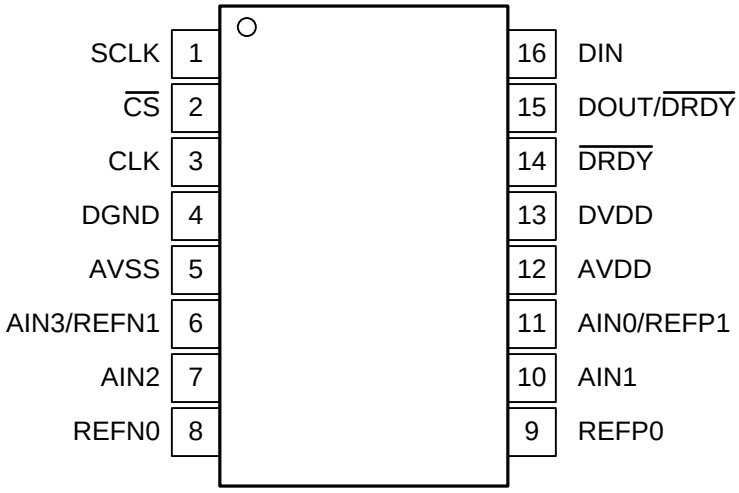


Pin Descriptions (QFN Package)

NAME	PIN NO.	ANALOG OR DIGITAL INPUT/OUTPUT	DESCRIPTION
CLK	1	Digital input	External clock source pin; connect to DGND if not used
DGND	2	Digital	Digital ground
AVSS	3	Analog	Negative analog power supply
AIN3/REFN1	4	Analog input	Differential or single-ended input; negative reference input(1)
AIN2	5	Analog input	Differential or single-ended input(1)
REFN0	6	Analog input	Negative reference input
REFP0	7	Analog input	Positive reference input
AIN1	8	Analog input	Differential or single-ended input(1)
AIN0/REFP1	9	Analog input	Differential or single-ended input; positive reference input(1)
AVDD	10	Analog	Positive analog power supply
DVDD	11	Digital	Positive digital power supply
$\overline{\text{DRDY}}$	12	Digital output	Data ready; active low
DOUT/$\overline{\text{DRDY}}$	13	Digital output	Serial data output combined with data ready; active low
DIN	14	Digital input	Serial data input
SCLK	15	Digital input	Serial clock input
$\overline{\text{CS}}$	16	Digital input	Chip select; active low
Thermal pad		—	Thermal power pad. Do not connect or only connect to AVSS.

(1) Unused analog inputs can be left unconnected or tied to AVDD.

PW PACKAGE
TSSOP-16
(TOP VIEW)



Pin Descriptions (TSSOP Package)

NAME	PIN NO.	ANALOG OR DIGITAL INPUT/OUTPUT	DESCRIPTION
SCLK	1	Digital input	Serial clock input
$\overline{CS}$	2	Digital input	Chip select; active low
CLK	3	Digital input	External clock source pin; connect to DGND if not used
DGND	4	Digital	Digital ground
AVSS	5	Analog	Negative analog power supply
AIN3/REFN1	6	Analog input	Differential or single-ended input; negative reference input(1)
AIN2	7	Analog input	Differential or single-ended input(1)
REFN0	8	Analog input	Negative reference input
REFP0	9	Analog input	Positive reference input
AIN1	10	Analog input	Differential or single-ended input(1)
AIN0/REFP1	11	Analog input	Differential or single-ended input; positive reference input(1)
AVDD	12	Analog	Positive analog power supply
DVDD	13	Digital	Positive digital power supply
$\overline{DRDY}$	14	Digital output	Data ready; active low
DOUT/$\overline{DRDY}$	15	Digital output	Serial data output combined with data ready; active low
DIN	16	Digital input	Serial data input

(1) Unused analog inputs can be left unconnected or tied to AVDD.

Typical Characteristics

At T_A = +25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{REF} = 2.5 V, unless otherwise noted.

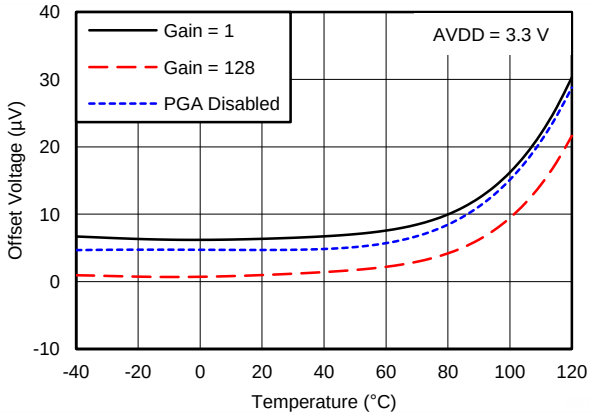


Figure 2. Input-Referred Offset Voltage vs Temperature (AVDD = 3.3 V)

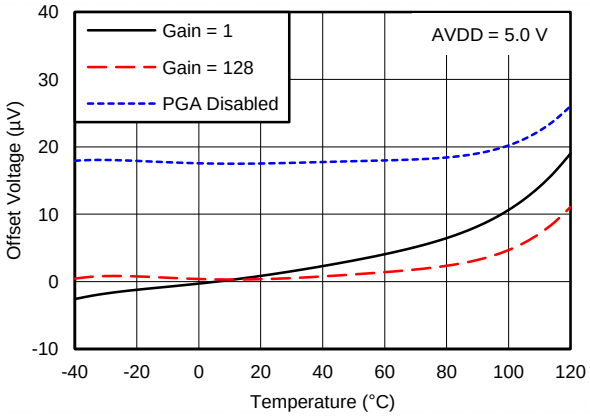


Figure 3. Input-Referred Offset Voltage vs Temperature (AVDD = 5.0 V)

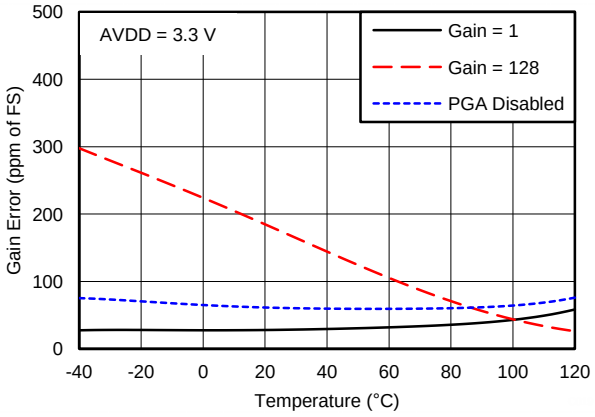


Figure 4. Gain Error vs Temperature (AVDD = 3.3 V)

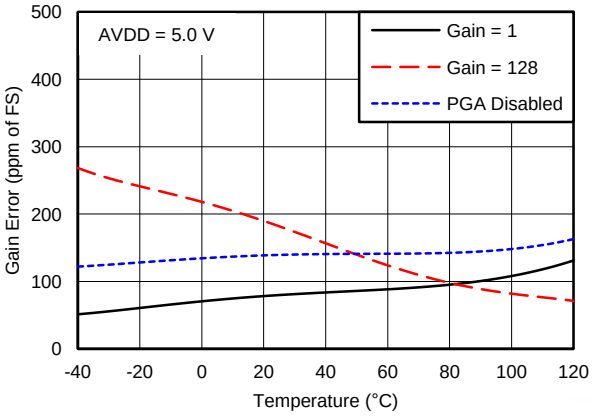


Figure 5. Gain Error vs Temperature (AVDD = 5.0 V)

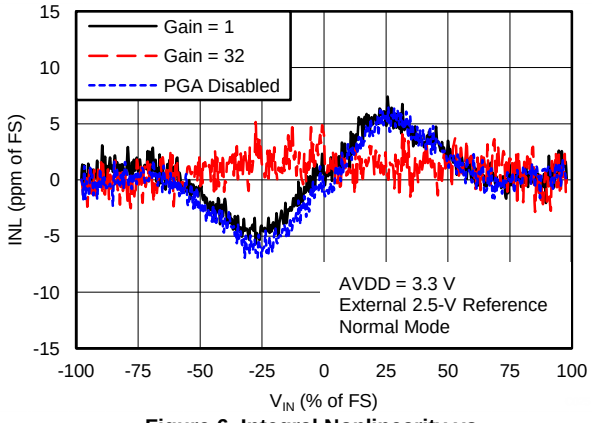


Figure 6. Integral Nonlinearity vs Differential Input Signal (AVDD = 3.3 V, External Reference)

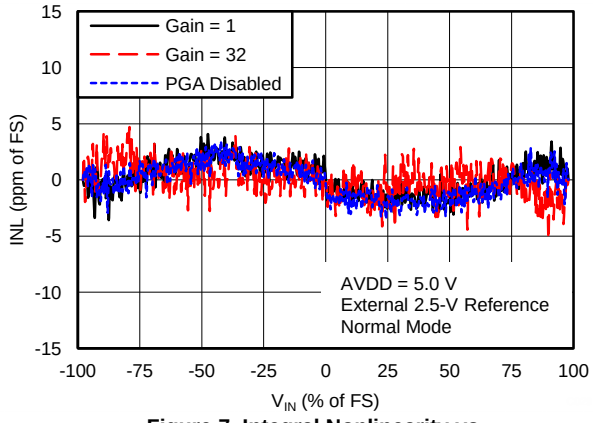


Figure 7. Integral Nonlinearity vs Differential Input Signal (AVDD = 5.0 V, External Reference)

Typical Characteristics (continued)

At T_A = +25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{REF} = 2.5 V, unless otherwise noted.

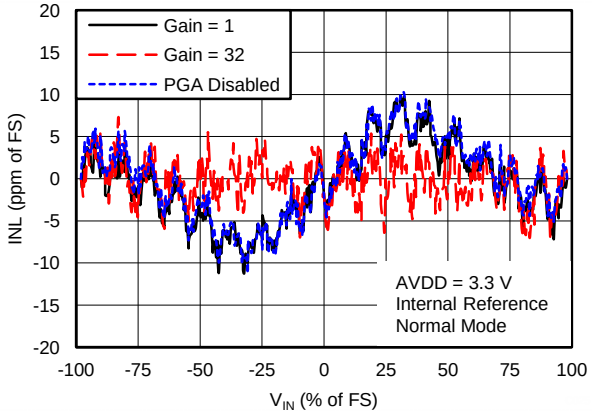


Figure 8. Integral Nonlinearity vs Differential Input Signal (AVDD = 3.3 V, Internal Reference)

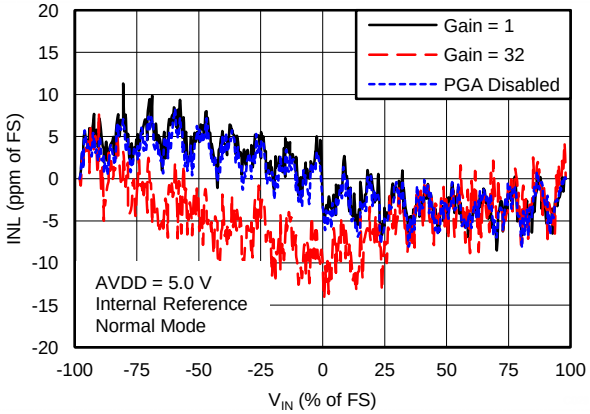


Figure 9. Integral Nonlinearity vs Differential Input Signal (AVDD = 5.0 V, Internal Reference)

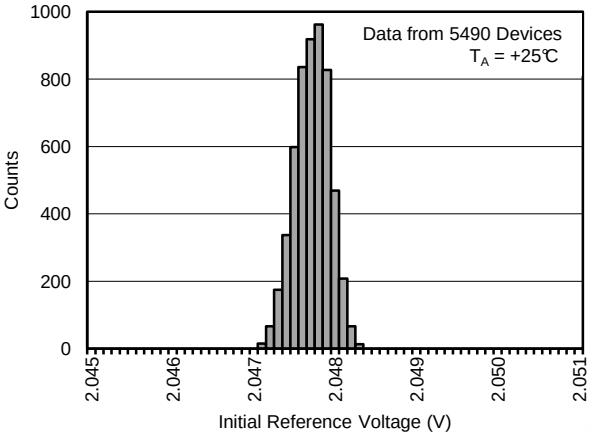


Figure 10. Internal Reference Voltage Histogram

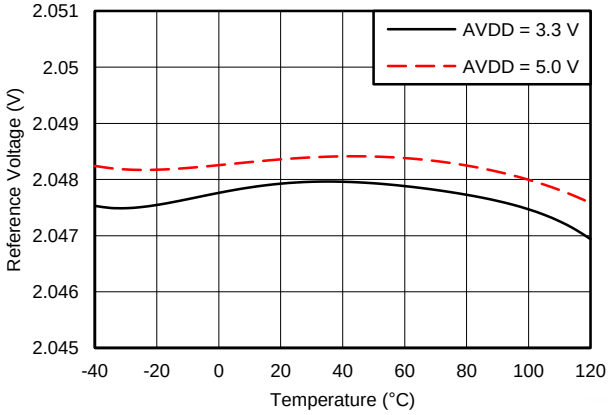


Figure 11. Internal Reference Voltage vs Temperature

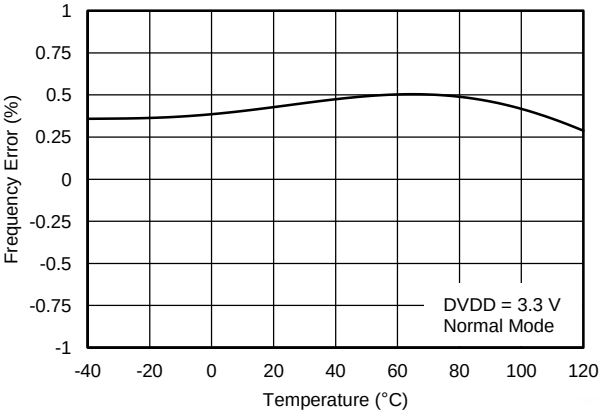


Figure 12. Internal Oscillator Accuracy vs Temperature

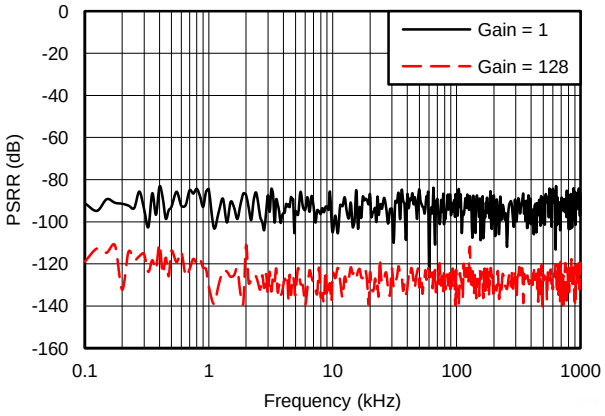


Figure 13. AVDD Power-Supply Rejection Ratio vs Frequency

Typical Characteristics (continued)

At T_A = +25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{REF} = 2.5 V, unless otherwise noted.

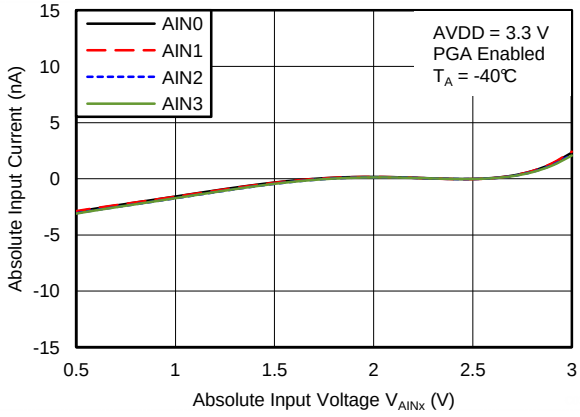


Figure 14. Absolute Input Current vs Absolute Input Voltage (PGA Enabled, T_A = –40°C)

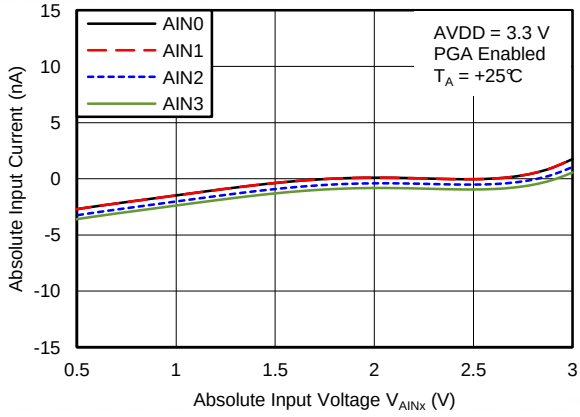


Figure 15. Absolute Input Current vs Absolute Input Voltage (PGA Enabled, T_A = +25°C)

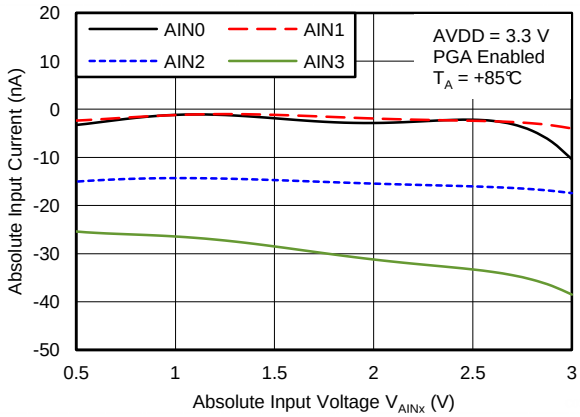


Figure 16. Absolute Input Current vs Absolute Input Voltage (PGA Enabled, T_A = +85°C)

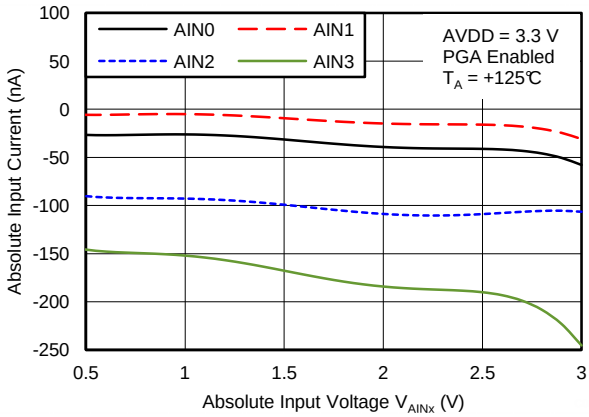


Figure 17. Absolute Input Current vs Absolute Input Voltage (PGA Enabled, T_A = +125°C)

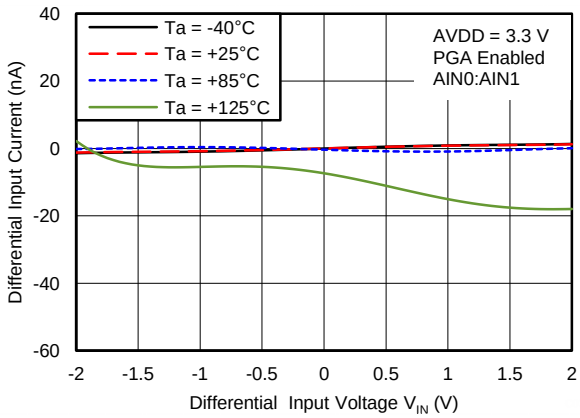


Figure 18. Differential Input Current vs Differential Input Voltage (PGA Enabled, AIN_P = AIN0, AIN_N = AIN1)

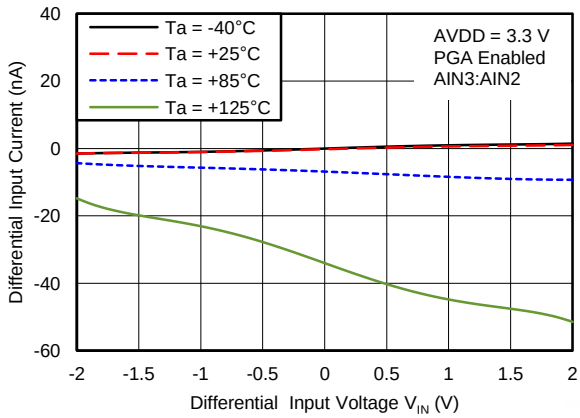


Figure 19. Differential Input Current vs Differential Input Voltage (PGA Enabled, AIN_P = AIN3, AIN_N = AIN2)

Typical Characteristics (continued)

At T_A = +25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{REF} = 2.5 V, unless otherwise noted.

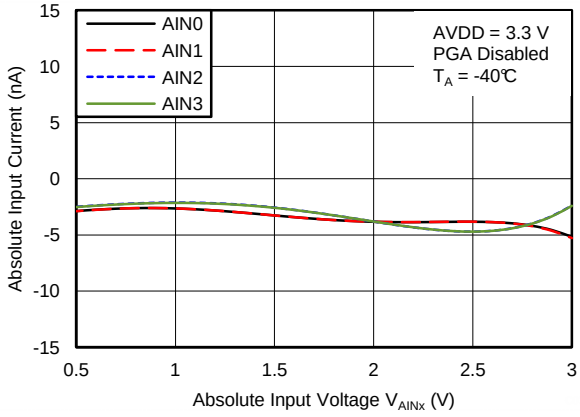


Figure 20. Absolute Input Current vs Absolute Input Voltage (PGA Disabled, T_A = –40°C)

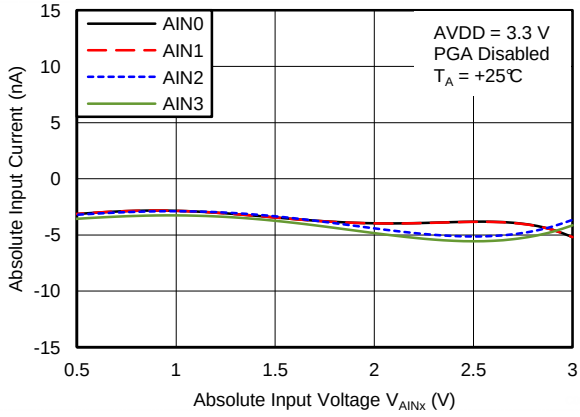


Figure 21. Absolute Input Current vs Absolute Input Voltage (PGA Disabled, T_A = +25°C)

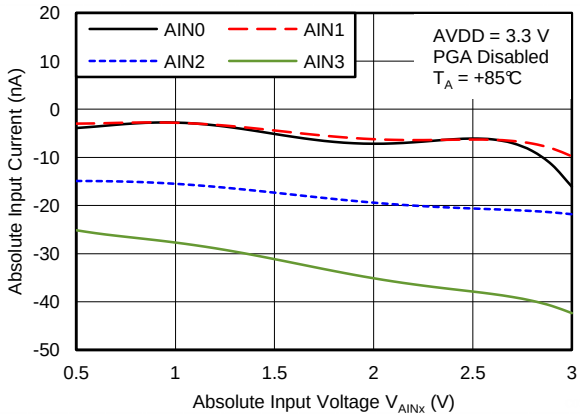


Figure 22. Absolute Input Current vs Absolute Input Voltage (PGA Disabled, T_A = +85°C)

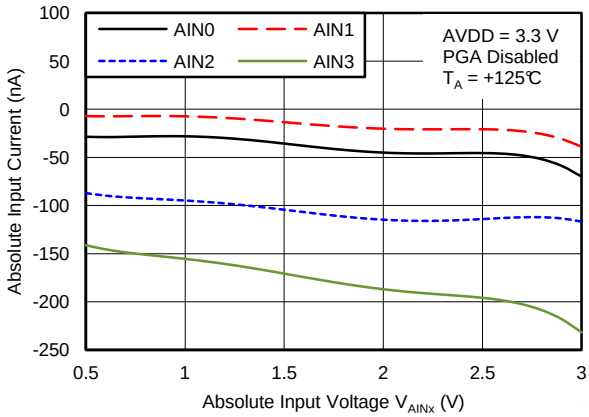


Figure 23. Absolute Input Current vs Absolute Input Voltage (PGA Disabled, T_A = +125°C)

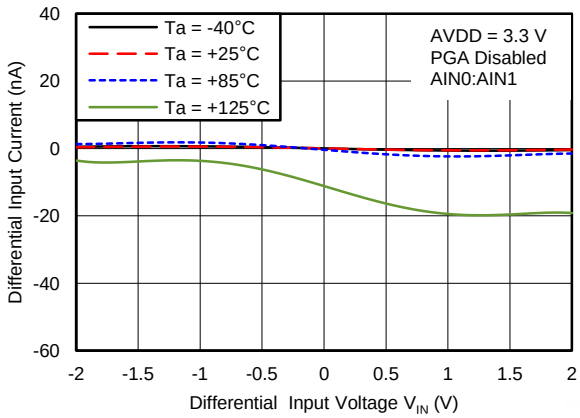


Figure 24. Differential Input Current vs Differential Input Voltage (PGA Disabled, AIN_P = AIN0, AIN_N = AIN1)

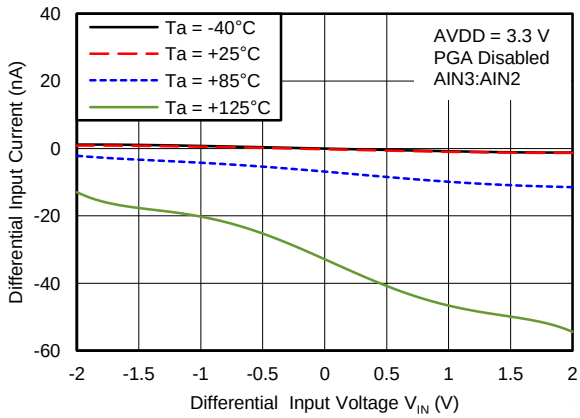


Figure 25. Differential Input Current vs Differential Input Voltage (PGA Disabled, AIN_P = AIN3, AIN_N = AIN2)

Typical Characteristics (continued)

At T_A = +25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{REF} = 2.5 V, unless otherwise noted.

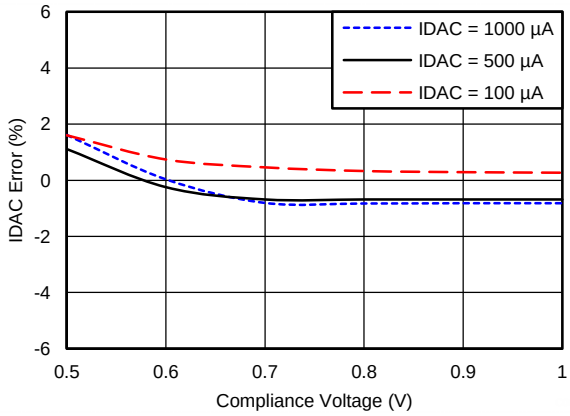


Figure 26. IDAC Accuracy vs Compliance Voltage

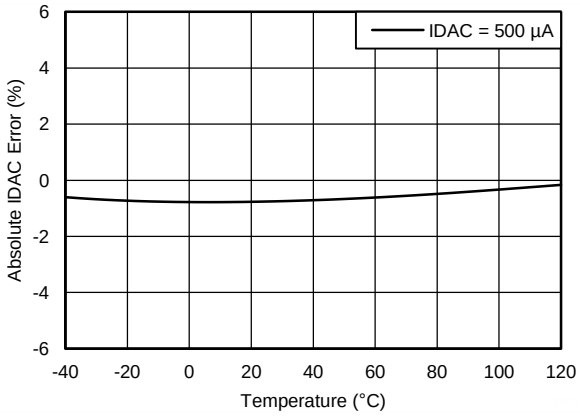


Figure 27. IDAC Accuracy vs Temperature

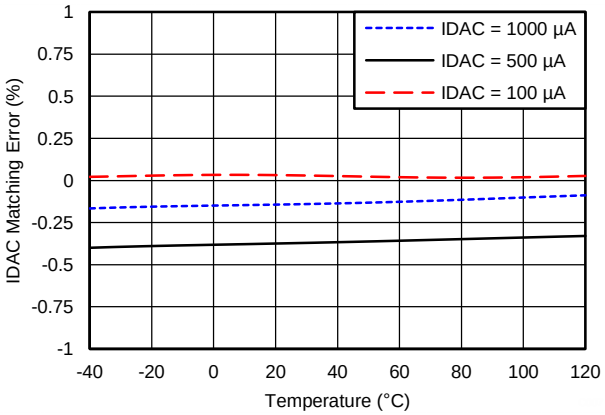


Figure 28. IDAC Matching vs Temperature

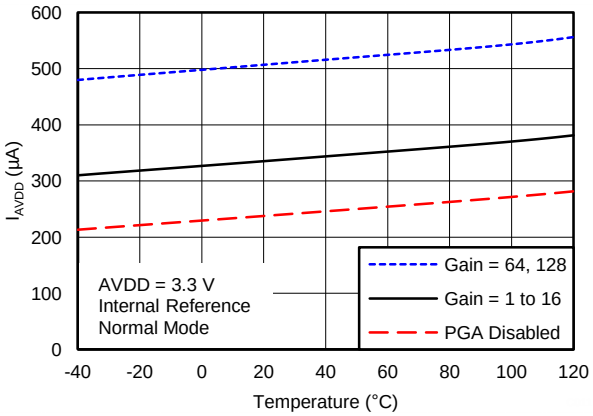


Figure 29. I_{AVDD} vs Temperature (Normal Mode)

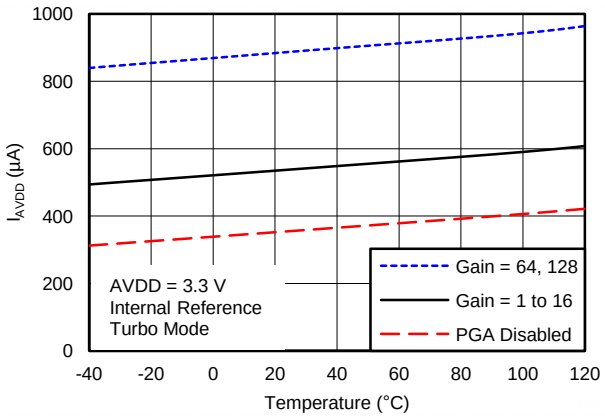


Figure 30. I_{AVDD} vs Temperature (Turbo Mode)

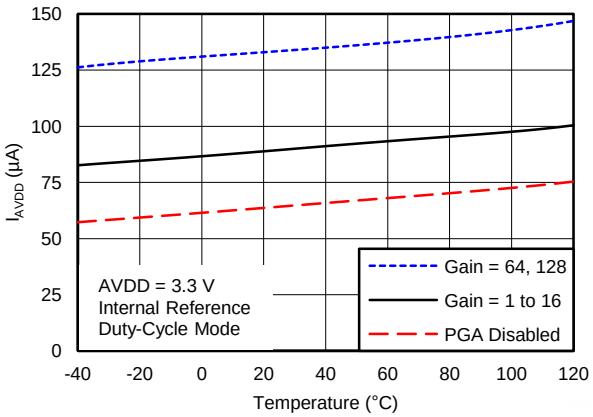


Figure 31. I_{AVDD} vs Temperature (Duty-Cycle Mode)

Typical Characteristics (continued)

At T_A = +25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{REF} = 2.5 V, unless otherwise noted.

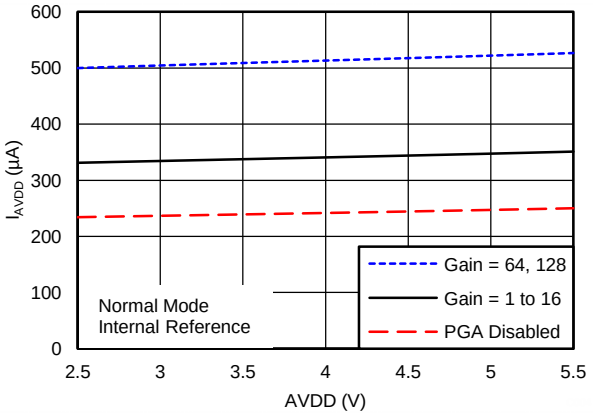


Figure 32. I_{AVDD} vs AVDD

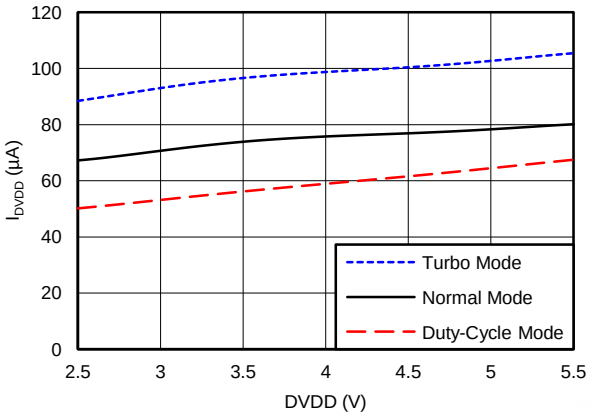


Figure 33. I_{DVDD} vs DVDD

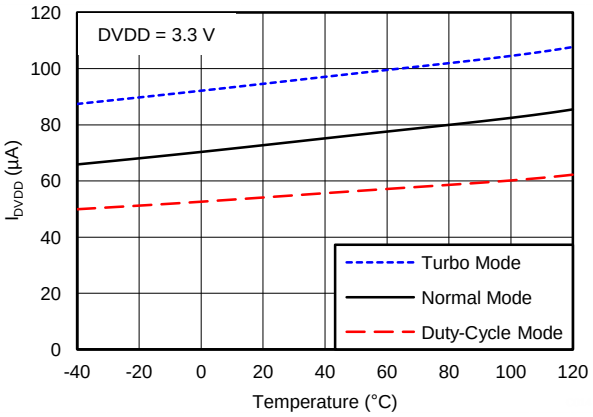


Figure 34. I_{DVDD} vs Temperature

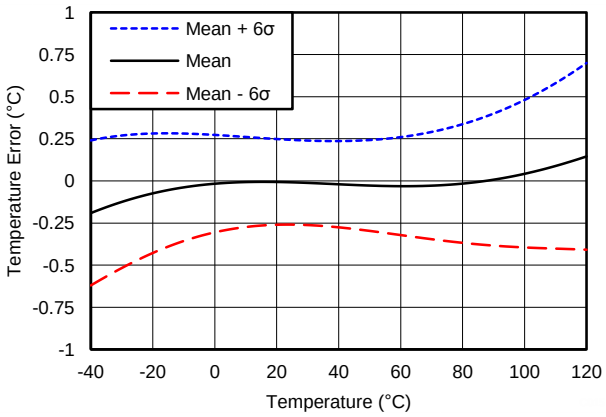


Figure 35. Internal Temperature Sensor Accuracy vs Temperature

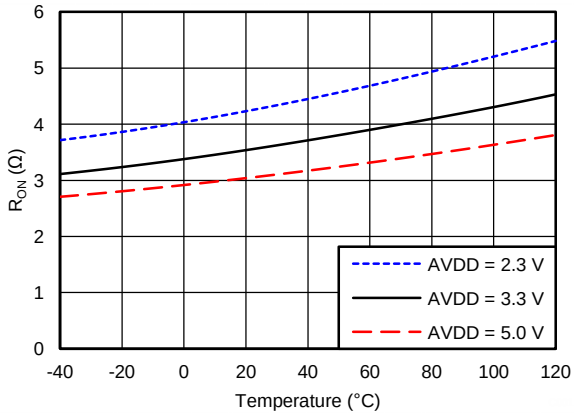


Figure 36. Low-Side Power Switch R_{ON} vs Temperature

Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called *oversampling ratio*, OSR. By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Table 1 to Table 4 summarize the device noise performance. Data are representative of typical noise performance at T_A = +25°C using the internal 2.048-V reference. Data shown are the result of averaging readings from a single device over a time period of approximately 0.75 seconds and are measured with the inputs internally shorted together. Table 1 and Table 3 list the input-referred noise in units of μV_{RMS} for the conditions shown. Note that μV_{PP} values are shown in parenthesis. Table 2 and Table 4 list the corresponding data in effective number of bits (ENOB) calculated from μV_{RMS} values using Equation 1. Note that noise-free bits calculated from peak-to-peak noise values are shown in parenthesis.

The input-referred noise (Table 1 and Table 3) only changes marginally when using an external low-noise reference, such as the REF5020. To calculate ENOB numbers and noise-free bits when using a reference voltage other than 2.048 V, use Equation 1 to Equation 3:

$$\text{ENOB} = \ln(\text{Full-Scale Range} / V_{\text{RMS-Noise}}) / \ln(2) \quad (1)$$

$$\text{Noise-Free Bits} = \ln(\text{Full-Scale Range} / V_{\text{PP-Noise}}) / \ln(2) \quad (2)$$

$$\text{Full-Scale Range} = 2 \cdot V_{REF} / \text{Gain} \quad (3)$$

Table 1. Noise in μV_{RMS} (μV_{PP}) at AVDD = 3.3 V, AVSS = 0 V, and Internal Reference = 2.048 V

DATA RATE (SPS)	GAIN (PGA ENABLED)							
	1	2	4	8	16	32	64	128
20	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)	7.81 (7.81)	3.91 (3.91)	1.95 (1.95)	0.98 (0.98)	0.49 (0.49)
45	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)	7.81 (7.81)	3.91 (3.91)	1.95 (1.95)	0.98 (0.98)	0.49 (0.51)
90	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)	7.81 (7.81)	3.91 (3.91)	1.95 (2.14)	0.98 (1.22)	0.49 (0.85)
175	62.50 (63.72)	31.25 (34.06)	15.63 (17.76)	7.81 (11.20)	3.91 (5.13)	1.95 (3.09)	0.98 (2.14)	0.49 (1.60)
330	62.50 (106.93)	31.25 (50.78)	15.63 (26.25)	7.81 (14.13)	3.91 (7.52)	1.95 (4.66)	0.98 (2.69)	0.49 (1.99)
600	62.50 (151.61)	31.25 (72.27)	15.63 (39.43)	7.81 (19.26)	3.91 (12.77)	1.95 (6.87)	0.98 (4.76)	0.55 (3.34)
1000	62.50 (227.29)	31.25 (122.68)	15.63 (58.53)	7.81 (31.52)	3.91 (18.08)	1.95 (10.71)	1.03 (6.52)	0.70 (4.01)
2000	62.50 (265.14)	31.25 (127.32)	15.63 (65.43)	7.81 (37.02)	3.91 (18.89)	1.95 (12.00)	1.13 (7.60)	0.82 (5.81)

Table 2. ENOB from RMS Noise (Peak-to-Peak Noise) at AVDD = 3.3 V, AVSS = 0 V, and Internal Reference = 2.048 V

DATA RATE (SPS)	GAIN (PGA ENABLED)							
	1	2	4	8	16	32	64	128
20	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
45	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.49)
90	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.87)	16 (15.67)	16 (15.20)
175	16 (15.97)	16 (15.88)	16 (15.82)	16 (15.48)	16 (15.61)	16 (15.34)	16 (14.87)	16 (14.29)
330	16 (15.23)	16 (15.30)	16 (15.25)	16 (15.15)	16 (15.05)	16 (14.74)	16 (14.54)	16 (13.97)
600	16 (14.72)	16 (14.79)	16 (14.66)	16 (14.70)	16 (14.29)	16 (14.18)	16 (13.72)	15.83 (13.23)
1000	16 (14.14)	16 (14.03)	16 (14.09)	16 (13.99)	16 (13.79)	16 (13.54)	15.92 (13.26)	15.49 (12.96)
2000	16 (13.92)	16 (13.97)	16 (13.93)	16 (13.76)	16 (13.73)	16 (13.38)	15.79 (13.04)	15.25 (12.43)

Table 3. Noise in μV_{RMS} (μV_{PP}) with PGA Disabled at AVDD = 3.3 V, AVSS = 0 V, and Internal Reference = 2.048 V

DATA RATE (SPS)	GAIN (PGA DISABLED)		
	1	2	4
20	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)
45	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)
90	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)
175	62.50 (65.92)	31.25 (35.40)	15.63 (18.92)
330	62.50 (94.24)	31.25 (50.17)	15.63 (28.75)
600	62.50 (138.67)	31.25 (78.13)	15.63 (39.79)
1000	62.50 (260.50)	31.25 (120.97)	15.63 (63.72)
2000	62.50 (250.98)	31.25 (131.35)	15.63 (68.18)

Table 4. ENOB from RMS Noise (Peak-to-Peak Noise) with PGA Disabled at AVDD = 3.3 V, AVSS = 0 V, and Internal Reference = 2.048 V

DATA RATE (SPS)	GAIN (PGA DISABLED)		
	1	2	4
20	16 (16)	16 (16)	16 (16)
45	16 (16)	16 (16)	16 (16)
90	16 (16)	16 (16)	16 (16)
175	16 (15.92)	16 (15.82)	16 (15.72)
330	16 (15.41)	16 (15.32)	16 (15.12)
600	16 (14.85)	16 (14.68)	16 (14.65)
1000	16 (13.94)	16 (14.05)	16 (13.97)
2000	16 (13.99)	16 (13.93)	16 (13.87)

Overview

The ADS1120 is a small, low-power, 16-bit, ΔΣ ADC that offers many integrated features that reduce system cost and component count in applications measuring small sensor signals.

In addition to the ΔΣ ADC core and single-cycle settling digital filter, the device offers a low-noise, high input impedance, programmable gain amplifier (PGA), an internal voltage reference, and a clock oscillator. The device also integrates a highly linear and accurate temperature sensor as well as two matched programmable current sources (IDACs) for sensor excitation. All of these features are intended to reduce the required external circuitry in typical sensor applications and improve overall system performance. An additional low-side power switch eases the design of low-power bridge sensor applications. The device is fully configured through four registers and controlled by six commands through a mode 1 SPI-compatible interface. Figure 37 shows the device functional block diagram.

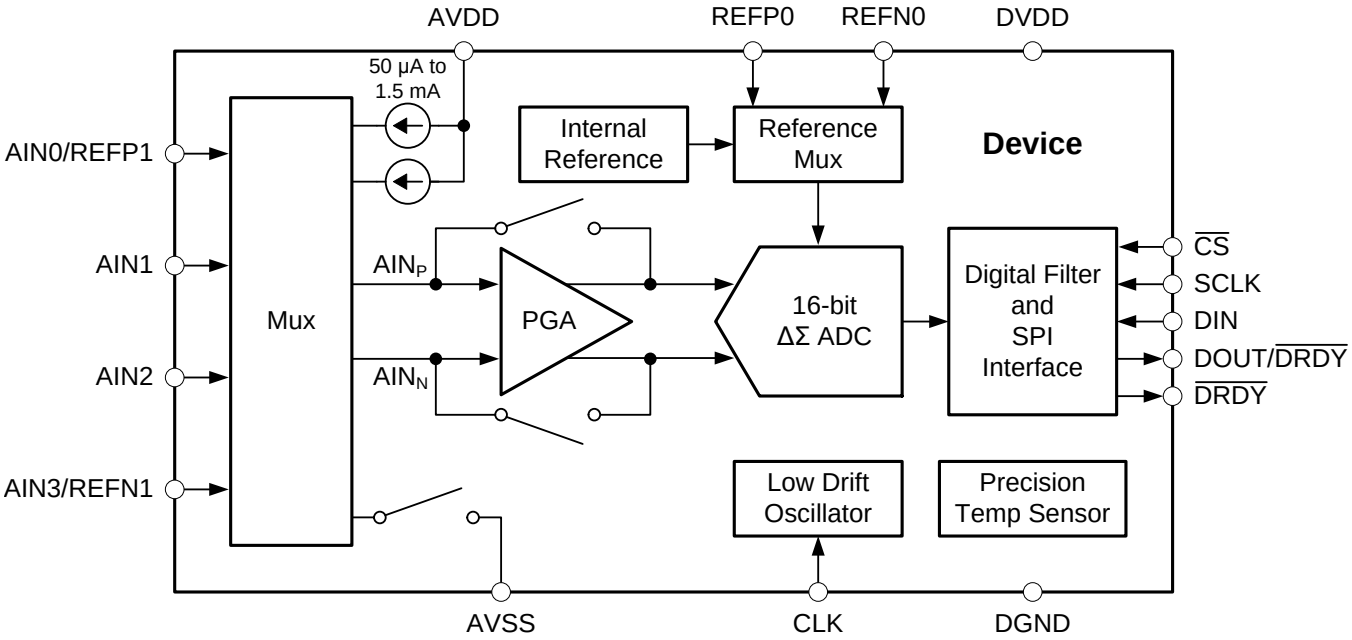


Figure 37. Functional Block Diagram

The ADS1120 ADC measures a differential signal, V_{IN}, which is the difference in voltage between nodes AIN_P and AIN_N. The converter core consists of a differential, switched-capacitor, ΔΣ modulator followed by a digital filter. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage. This architecture results in a very strong attenuation in any common-mode signal.

The device has two available conversion modes: single-shot and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value in an internal data buffer. The device then enters a low-power state to save power. Single-shot mode is intended to provide significant power savings in systems that require only periodic conversions, or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. New data are available at the programmed data rate. Data can be read at any time without concern of data corruption and always reflect the most recently completed conversion.

Multiplexer

The device contains a very flexible input multiplexer, as shown in Figure 38. Either four single-ended signals, two differential signals, or a combination of two single-ended signals and one differential signal can be measured. The multiplexer is configured by four bits (MUX[3:0]) in the configuration register. When single-ended signals are measured, the negative ADC input (AIN_N) is internally connected to AVSS by a switch within the multiplexer. For system-monitoring purposes, the analog supply (AVDD – AVSS) / 4 or the currently-selected external reference voltage ($V_{REFPx} – V_{REFNx}$) / 4 can be selected as inputs to the ADC. The multiplexer also offers the possibility to route any of the two programmable current sources to any analog input (AINx) or to any dedicated reference pin (REFP0, REFN0).

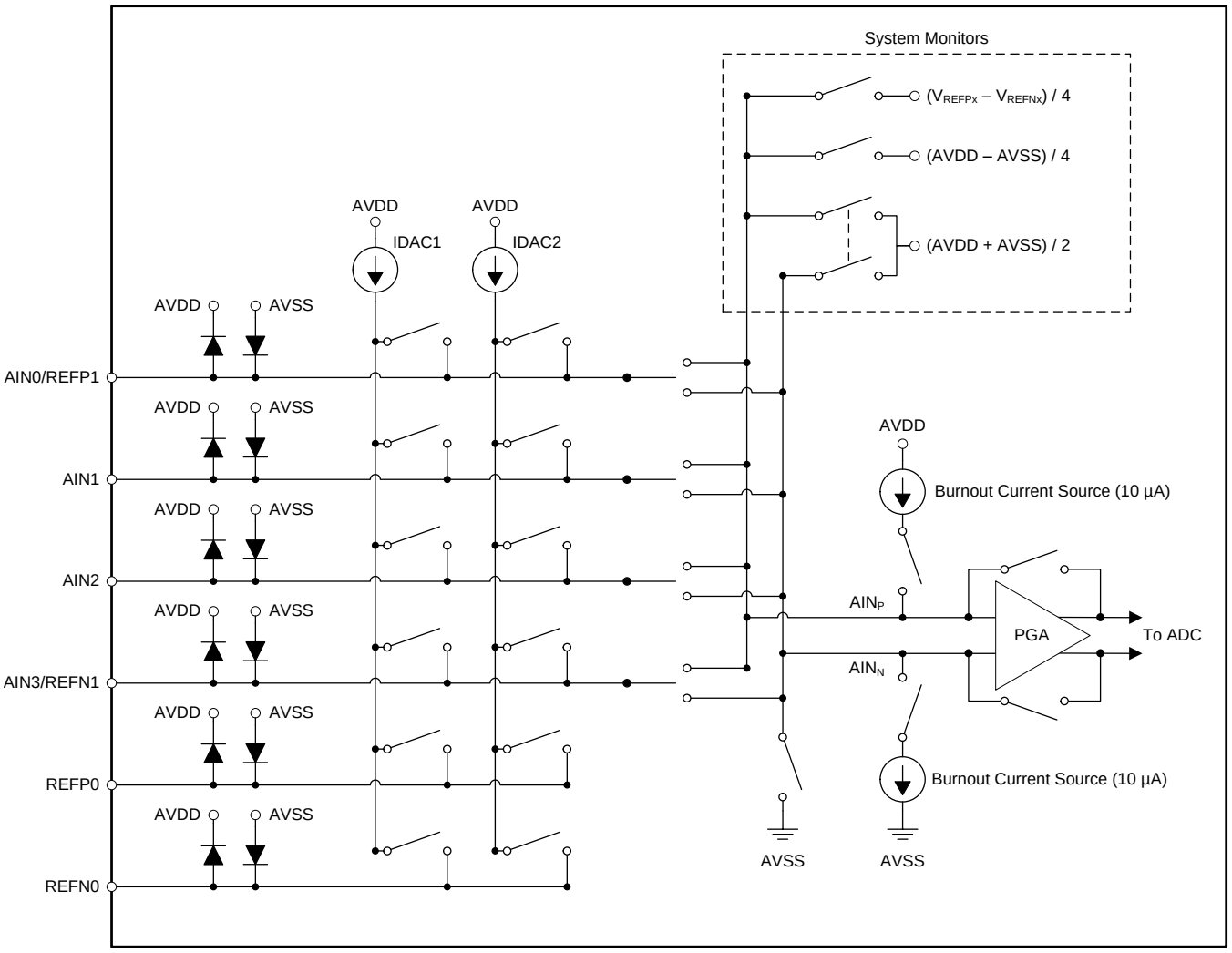


Figure 38. Analog Input Multiplexer

Electrostatic discharge (ESD) diodes to AVDD and AVSS protect the inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range of Equation 4:

$$AVSS – 0.3\ V < V_{AINx} < AVDD + 0.3\ V \quad (4)$$

If the voltages on the input pins have any potential to violate these conditions, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings table). Overdriving an unused input on the device may affect conversions taking place on other input pins. If any overdrive on unused inputs is possible, TI recommends clamping the signal with external Schottky diodes.

Low-Noise PGA

The device features a low-noise, low-drift, high input impedance, programmable gain amplifier (PGA). The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Three bits (GAIN[2:0]) in the configuration register are used to configure the gain. A simplified diagram of the PGA is shown in Figure 39. The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the PGA gain. The PGA input is equipped with an electromagnetic interference (EMI) filter.

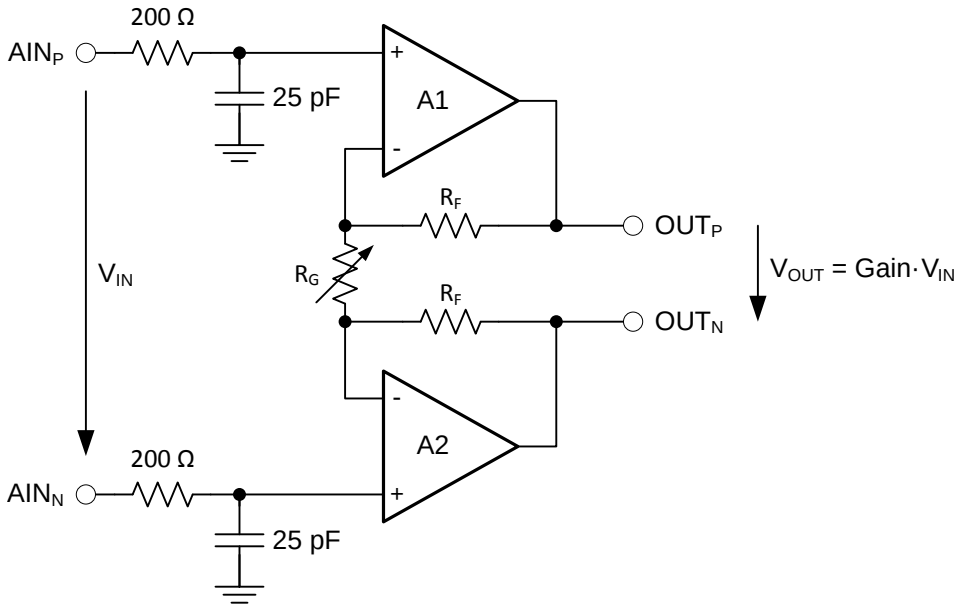


Figure 39. Simplified PGA Diagram

V_{IN} denotes the differential input voltage $V_{IN} = (V_{AINP} – V_{AINN})$. The gain of the PGA can be calculated with Equation 5:

$$Gain = 1 + 2 \cdot R_F / R_G \quad (5)$$

Gain is changed inside the device by switching in and out different values of R_G. The differential full-scale (FS) input voltage range of the PGA is defined by the gain setting and the reference voltage used, as shown in Equation 6:

$$FS = \pm V_{REF} / Gain \quad (6)$$

Table 5 shows the corresponding full-scale ranges when using an internal 2.048-V reference.

Table 5. PGA Full-Scale Range

GAIN SETTING	FS
1	±2.048 V
2	±1.024 V
4	±0.512 V
8	±0.256 V
16	±0.128 V
32	±0.064 V
64	±0.032 V
128	±0.016 V

To stay within the linear operating range of the PGA, the input signals must meet certain requirements that are discussed in this section.

The outputs of both amplifiers (A1 and A2) in Figure 39 can not swing closer to the supplies (AVSS and AVDD) than 200 mV. If the outputs OUT_P and OUT_N are driven closer to the analog supply rails than 200 mV, the amplifiers saturate and consequently become nonlinear. This condition means that the output voltages must meet Equation 7:

$$AVSS + 0.2\ V \le V_{OUTN},\ V_{OUTP} \le AVDD - 0.2\ V \quad (7)$$

To derive the equation for the voltages at the outputs (OUT_P and OUT_N), splitting Figure 39 horizontally in the middle is a convenient method. This split can be accomplished because the PGA is a symmetrical design. Accordingly, the gain setting resistor (R_G) must be divided by two and all voltages at the horizontal cutting points must be referenced to the common-mode voltage (V_{CM}), as shown in Figure 40.

$$V_{CM} = \frac{V_{AINP} + V_{AINN}}{2} = \frac{V_{OUTP} + V_{OUTN}}{2} \quad (8)$$

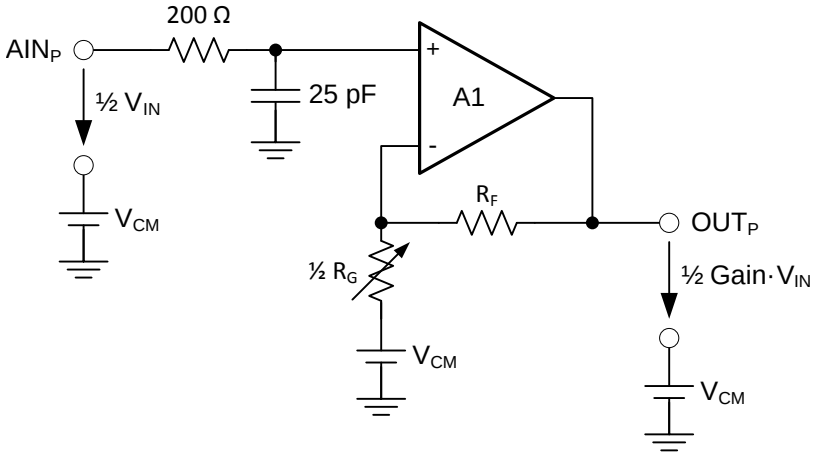


Figure 40. Positive Input Path of the PGA Referenced to V_{CM}

The voltages at the PGA inputs (AIN_P and AIN_N) can be expressed as Equation 9 and Equation 10:

$$V_{AINP} = V_{CM} + ½\ V_{IN} \quad (9)$$

$$V_{AINN} = V_{CM} - ½\ V_{IN} \quad (10)$$

The output voltages (V_{OUTP} and V_{OUTN}) can then be calculated as Equation 11 and Equation 12:

$$V_{OUTP} = \left(1 + 2\frac{R_F}{R_G}\right) \cdot V_{AINP} - \left(2\frac{R_F}{R_G}\right) \cdot V_{CM} = Gain \cdot V_{AINP} - (Gain - 1) \cdot V_{CM} = Gain \cdot \left(V_{CM} + \frac{1}{2} V_{IN}\right) - (Gain - 1) \cdot V_{CM}$$

$$V_{OUTP} = V_{CM} + \frac{1}{2} Gain \cdot V_{IN} \quad (11)$$

$$V_{OUTN} = \left(1 + 2\frac{R_F}{R_G}\right) \cdot V_{AINN} - \left(2\frac{R_F}{R_G}\right) \cdot V_{CM} = Gain \cdot V_{AINN} - (Gain - 1) \cdot V_{CM} = Gain \cdot \left(V_{CM} + \frac{1}{2} V_{IN}\right) - (Gain - 1) \cdot V_{CM}$$

$$V_{OUTN} = V_{CM} - \frac{1}{2} Gain \cdot V_{IN} \quad (12)$$

The requirements for the output voltages of amplifiers A1 and A2 (Equation 7) can also be translated into requirements for the input common-mode voltage range using Equation 11 and Equation 12, which are given in Equation 13 and Equation 14:

$$V_{CM\ (MIN)} \geq AVSS + 0.2\ V + ½\ Gain \cdot V_{IN\ (MAX)} \quad (13)$$

$$V_{CM\ (MAX)} \leq AVDD - 0.2\ V - ½\ Gain \cdot V_{IN\ (MAX)} \quad (14)$$

In order to calculate the minimum and maximum common-mode voltage limits, the maximum differential input voltage ($V_{IN\ (MAX)}$) that occurs in the application must be used, which is not necessarily the possible FS range.

The minimum V_{CM} must also meet Equation 15 because of the specific design implementation of the PGA.

$$V_{CM\ (MIN)} \geq AVSS + ¼\ (AVDD - AVSS) \quad (15)$$

NOTE

Common-mode voltage requirements are:

$V_{CM\ (MIN)} \geq AVSS + ¼\ (AVDD - AVSS)$

$V_{CM\ (MIN)} \geq AVSS + 0.2\ V + ½\ Gain \cdot V_{IN\ (MAX)}$

$V_{CM\ (MAX)} \leq AVDD - 0.2\ V - ½\ Gain \cdot V_{IN\ (MAX)}$

Figure 41 and Figure 42 show a graphical representation of the common-mode voltage limits for AVDD = 3.3 V and AVSS = 0 V, with gain = 1 and gain = 16, respectively.

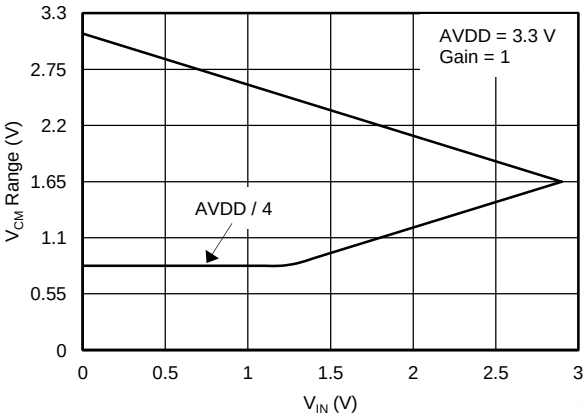


Figure 41. Common-Mode Voltage Limits (AVDD = 3.3 V, Gain = 1)

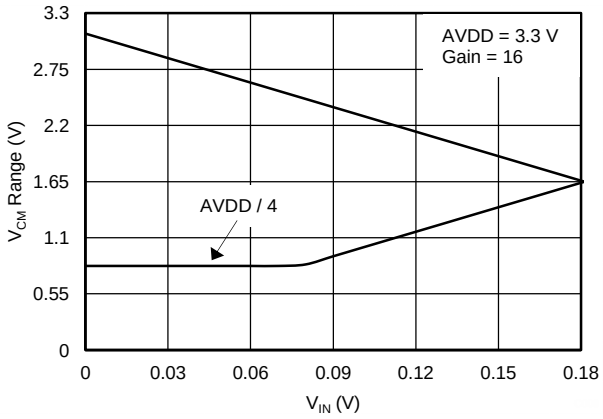


Figure 42. Common-Mode Voltage Limits (AVDD = 3.3 V, Gain = 16)

The following discussion explains how to apply Equation 13 through Equation 15 to a hypothetical application. The setup for this example is AVDD = 3.3 V, AVSS = 0 V, and gain = 16, using an external reference, V_{REF} = 2.5 V. The maximum possible differential input voltage $V_{IN} = (V_{AINP} - V_{AINN})$ that can be applied is then limited to the full-scale range of FS = ±2.5 V / 16 = ±0.156 V. Consequently, Equation 13 through Equation 15 yield an allowed V_{CM} range of 1.45 V ≤ V_{CM} ≤ 1.85 V.

If the sensor signal connected to the inputs in this hypothetical application does not make use of the entire full-scale range but is limited to $V_{IN\ (MAX)}$ = ±0.1 V, for example, then this reduced input signal amplitude relaxes the V_{CM} restriction to 1.0 V ≤ V_{CM} ≤ 2.3 V.

In the case of a fully-differential sensor signal, each input (AIN_P, AIN_N) can swing up to ±50 mV around the common-mode voltage (V_{AINP} + V_{AINN}) / 2, which must remain between the limits of 1.0 V and 2.3 V. The output of a symmetrical wheatstone bridge is an example of a fully-differential signal.

In contrast, the signal of an RTD is of a pseudo-differential nature (if implemented as shown in the *RTD Measurement* section), where the negative input is held at a constant voltage other than 0 V and only the voltage on the positive input changes. When a pseudo-differential signal must be measured, the negative input in this example must be biased at a voltage between 0.95 V and 2.25 V. The positive input can then swing up to $V_{IN\ (MAX)}$ = 100 mV above the negative input. Note that in this case the common-mode voltage changes at the same time the voltage on the positive input changes. That is, while the input signal swings between 0 V ≤ V_{IN} ≤ $V_{IN\ (MAX)}$, the common-mode voltage swings between V_{AINN} ≤ V_{CM} ≤ V_{AINN} + ½ $V_{IN\ (MAX)}$. Satisfying the common-mode voltage requirements for the maximum input voltage $V_{IN\ (MAX)}$ ensures the requirements are met throughout the entire signal range.

Figure 43 and Figure 44 illustrate examples of both fully-differential and pseudo-differential signals, respectively.

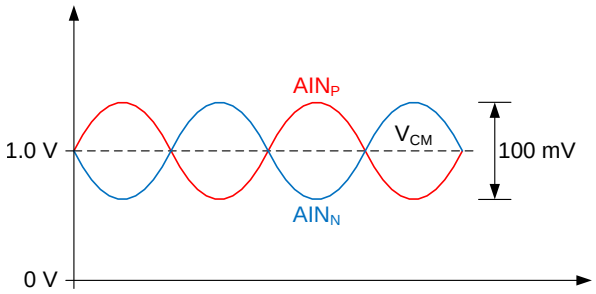


Figure 43. Fully-Differential Input Signal

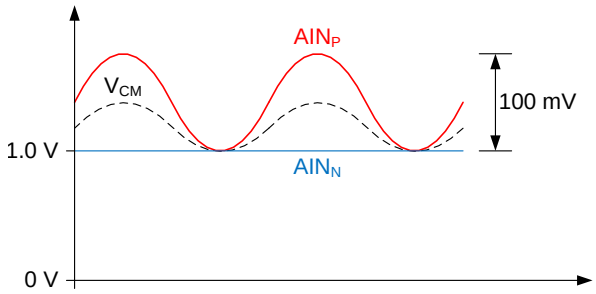


Figure 44. Pseudo-Differential Input Signal

Bypassing the PGA

At gains of 1, 2, and 4, the device can be configured to disable and bypass the low-noise PGA. Disabling the PGA lowers the overall power consumption and also removes the restrictions of Equation 13 through Equation 15 for the common-mode input voltage range, V_{CM}. The usable absolute and common-mode input voltage range is (AVSS – 0.1 V ≤ V_{AINx}, V_{CM} ≤ AVDD + 0.1 V) when the PGA is disabled. In order to measure single-ended signals that are referenced to AVSS (AIN_P = V_{IN}, AIN_N = AVSS), the PGA must be bypassed.

When the PGA is disabled by setting the PGA_BYPASS bit in the configuration register, the device uses a buffered switched-capacitor stage to obtain gains 1, 2, and 4. An internal buffer in front of the switched-capacitor stage ensures that the effect on the input loading resulting from the capacitors charging and discharging is minimal. Refer to Figure 20 to Figure 25 for the typical values of absolute input currents (current flowing into or out of each input) and differential input currents (difference in absolute current between positive and negative input) when the PGA is disabled.

For signal sources with high output impedance, external buffering may still be necessary. Note that active buffers introduce noise and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Modulator

A ΔΣ modulator is used in the ADS1120 to convert the analog input voltage into a pulse code modulated (PCM) data stream. The modulator runs at a modulator clock frequency of $f_{MOD} = f_{CLK} / 16$ in normal and duty-cycle mode and $f_{MOD} = f_{CLK} / 8$ in turbo mode, where f_{CLK} is either provided by the internal oscillator or the external clock source. Table 6 shows the modulator frequency for each mode using either the internal oscillator or an external clock of 4.096 MHz.

Table 6. Modulator Clock Frequency for Different Operating Modes using the Internal Oscillator

OPERATING MODE	f_{MOD}
Duty-cycle mode	256 kHz
Normal mode	256 kHz
Turbo mode	512 kHz

Digital Filter

The device uses a linear-phase finite impulse response (FIR) digital filter that performs both filtering and decimation of the digital data stream coming from the modulator. The digital filter is automatically adjusted for the different data rates and always settles within a single cycle. Only at data rates of 5 SPS and 20 SPS can the filter be configured to reject 50-Hz or 60-Hz line frequencies or to simultaneously reject 50 Hz and 60 Hz. Two bits (50/60[1:0]) in the configuration register are used to configure the filter accordingly. The frequency responses of the digital filter are shown in Figure 45 to Figure 58 for different output data rates using the internal oscillator or an external 4.096-MHz clock.

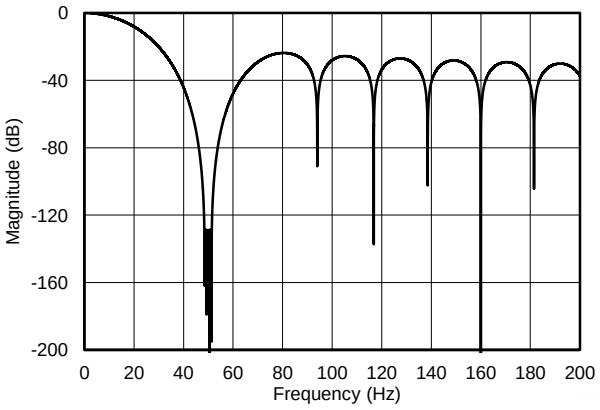


Figure 45. Filter Response (Data Rate = 20 SPS, 50-Hz Rejection Only)

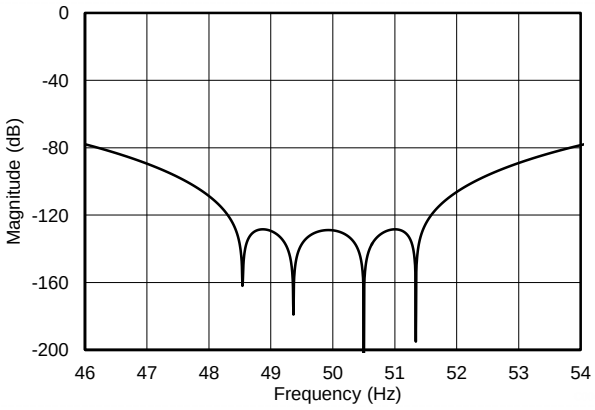


Figure 46. Detailed View of Filter Response (Data Rate = 20 SPS, 50-Hz Rejection Only)

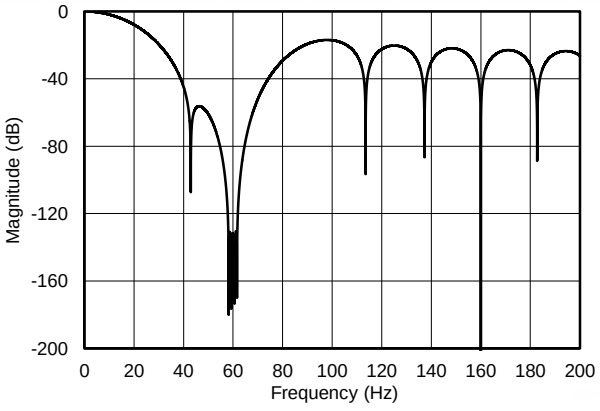


Figure 47. Filter Response (Data Rate = 20 SPS, 60-Hz Rejection Only)

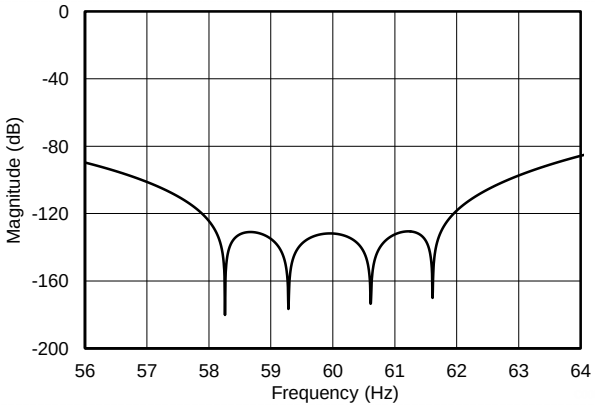


Figure 48. Detailed View of Filter Response (Data Rate = 20 SPS, 60-Hz Rejection Only)

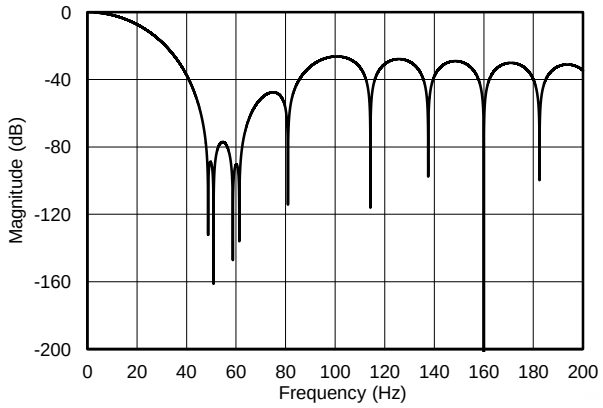


Figure 49. Filter Response (Data Rate = 20 SPS, Simultaneous 50- and 60-Hz Rejection)

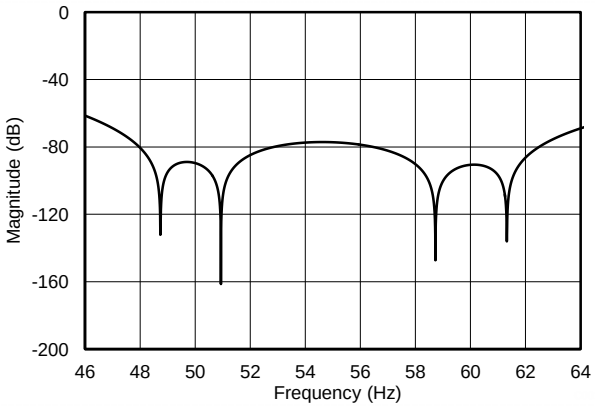


Figure 50. Detailed View of Filter Response (Data Rate = 20 SPS, Simultaneous 50- and 60-Hz Rejection)

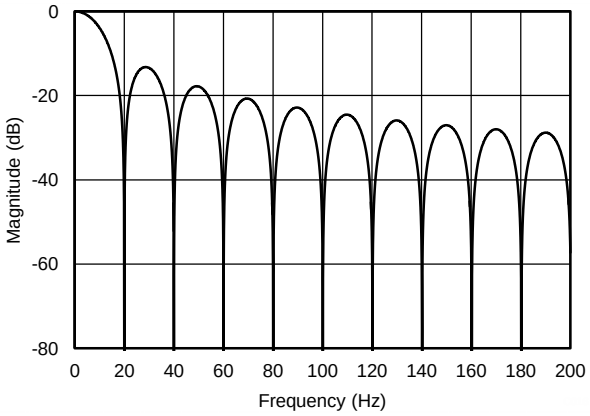


Figure 51. Filter Response (Data Rate = 20 SPS, No 50- or 60-Hz Rejection)

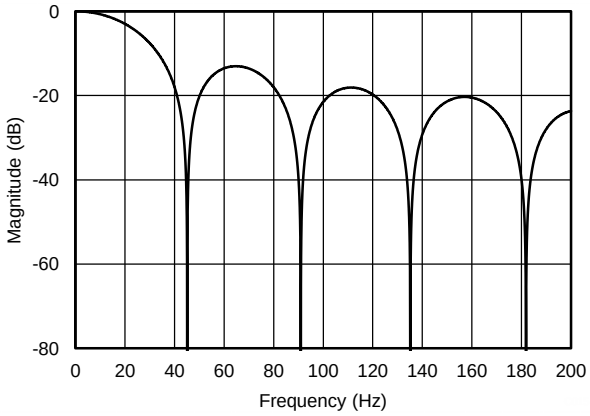


Figure 52. Filter Response (Data Rate = 45 SPS)

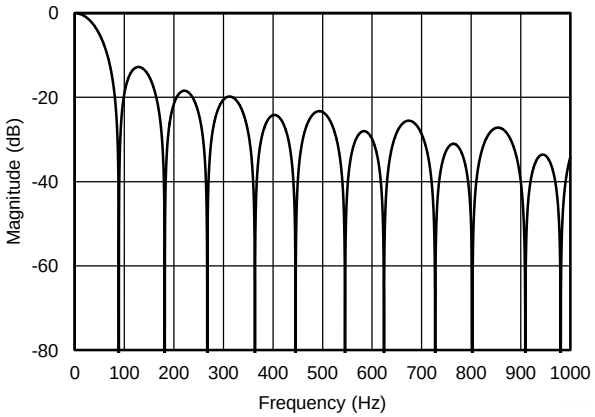


Figure 53. Filter Response (Data Rate = 90 SPS)

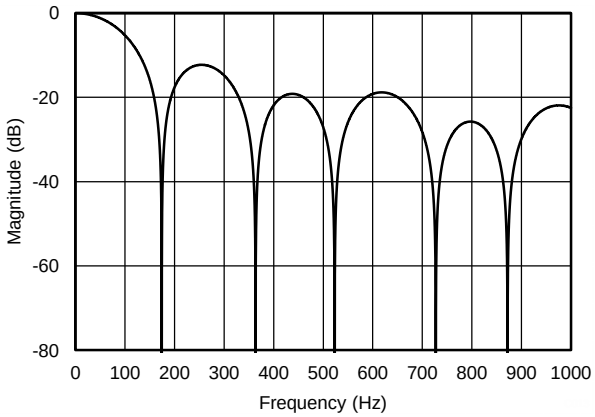


Figure 54. Filter Response (Data Rate = 175 SPS)

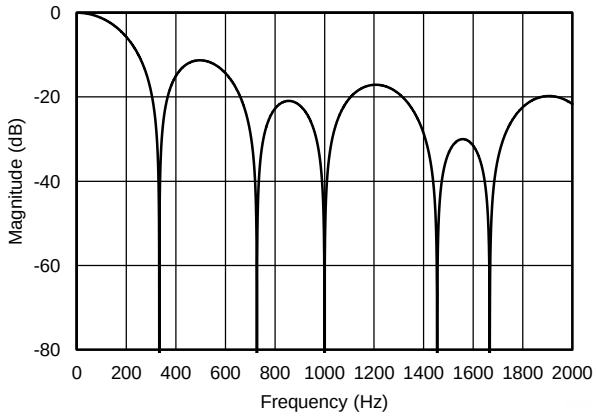


Figure 55. Filter Response (Data Rate = 330 SPS)

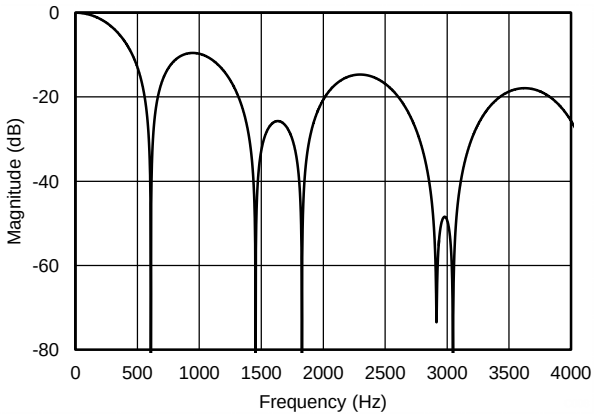


Figure 56. Filter Response (Data Rate = 600 SPS)

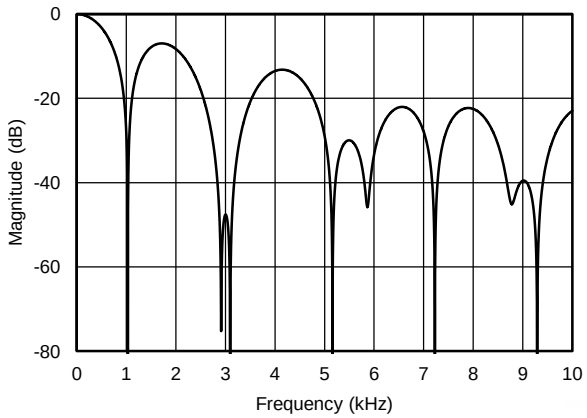


Figure 57. Filter Response (Data Rate = 1 kSPS)

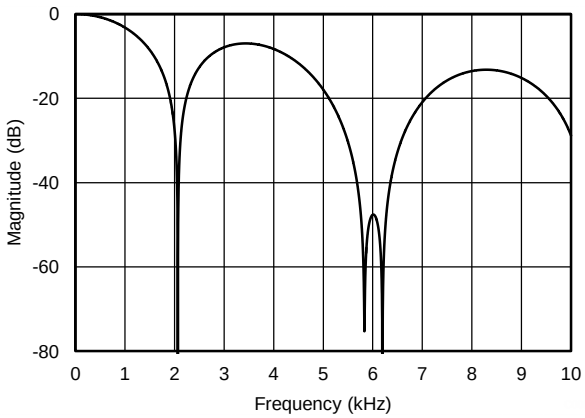


Figure 58. Filter Response (Data Rate = 2 kSPS)

NOTE

The filter notches change proportional to the clock frequency if an external clock with a frequency other than 4.096 MHz is used. For example, a notch that appears at 20 Hz when using a 4.096-MHz clock appears at 10 Hz if a 2.048-MHz clock is used.

Output Data Rate

Table 7 shows the actual conversion times for each data rate setting. The values provided are in terms of t_{CLK} cycles using an external clock with a clock frequency of f_{CLK} = 4.096 MHz. The data rates scale proportionally in case an external clock with a frequency other than 4.096 MHz is used.

Continuous conversion mode data rates are timed from one $\overline{DRDY}$ falling edge to the next $\overline{DRDY}$ falling edge. The first conversion starts 210 · t_{CLK} (normal mode, duty-cycle mode) or 114 · t_{CLK} (turbo mode) after the last SCLK falling edge of the START/SYNC command.

Single-shot mode data rates are timed from the last SCLK falling edge of the START/SYNC command to the $\overline{DRDY}$ falling edge and rounded to the next t_{CLK}. In case the internal oscillator is used, an additional oscillator wake-up time of up to 50 µs (normal mode, duty-cycle mode) or 25 µs (turbo mode) must be added in single-shot mode. The internal oscillator starts to power up at the first SCLK rising edge of the START/SYNC command. If an SCLK frequency higher than 160 kHz (normal mode, duty-cycle mode) or 320 kHz (turbo mode) is used, the oscillator may not be fully powered up at the end of the START/SYNC command. The ADC then waits until the internal oscillator is fully powered up before starting a conversion.

Single-shot conversion times in duty-cycle mode are the same as in normal mode. See the Duty-Cycle Mode section for more details on duty-cycle mode operation.

Table 7. Conversion Times

NOMINAL DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	ACTUAL CONVERSION TIME (t_{CLK})	
		CONTINUOUS CONVERSION MODE	SINGLE-SHOT MODE
Normal Mode			
20	13.1	204768	204850
45	20.0	91120	91218
90	39.6	46128	46226
175	77.8	23664	23762
330	150.1	12464	12562
600	279.0	6896	6994
1000	483.8	4144	4242
Duty-Cycle Mode			
5	13.1	823120	n/a
11.25	20.0	364560	n/a
22.5	39.6	184592	n/a
44	77.8	94736	n/a
82.5	150.1	49936	n/a
150	279.0	27664	n/a
250	483.8	16656	n/a
Turbo Mode			
40	26.2	102384	102434
90	39.9	45560	45618
180	79.2	23064	23122
350	155.6	11832	11890
660	300.3	6232	6290
1200	558.1	3448	3506
2000	967.6	2072	2130

Note that even though the conversion time at the 20-SPS setting is not exactly 1 / 20 Hz = 50 ms, this discrepancy does not affect the 50-Hz or 60-Hz rejection. To achieve the specified 50-Hz and 60-Hz rejection, the external clock frequency must only be ensured to be exactly 4.096 MHz.

Aliasing

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components in the input signal that are higher than half the sampling frequency of the ADC (also known as the *Nyquist frequency*) are folded back and show up in the actual frequency band of interest below half the sampling frequency. Note that inside a ΔΣ ADC, the input signal is sampled at the modulator frequency f_{MOD} and not at the output data rate. The filter response of the digital filter repeats at multiples of the sampling frequency (f_{MOD}), as shown in Figure 59. Signals or noise up to a frequency where the filter response repeats are attenuated by the digital filter. Unless attenuated by an external analog filter, any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and thus alias back into the band of interest. Some signals are inherently bandlimited; for example, the output of a thermocouple has a limited rate of change. Nevertheless, these signals can contain noise and interference components at higher frequencies, which can fold back into the frequency band of interest. A simple RC filter is (in most cases) sufficient to reject these high-frequency components. When designing an input filter circuit, be sure to take into account the interaction between the filter network and the input impedance of the ADS1120.

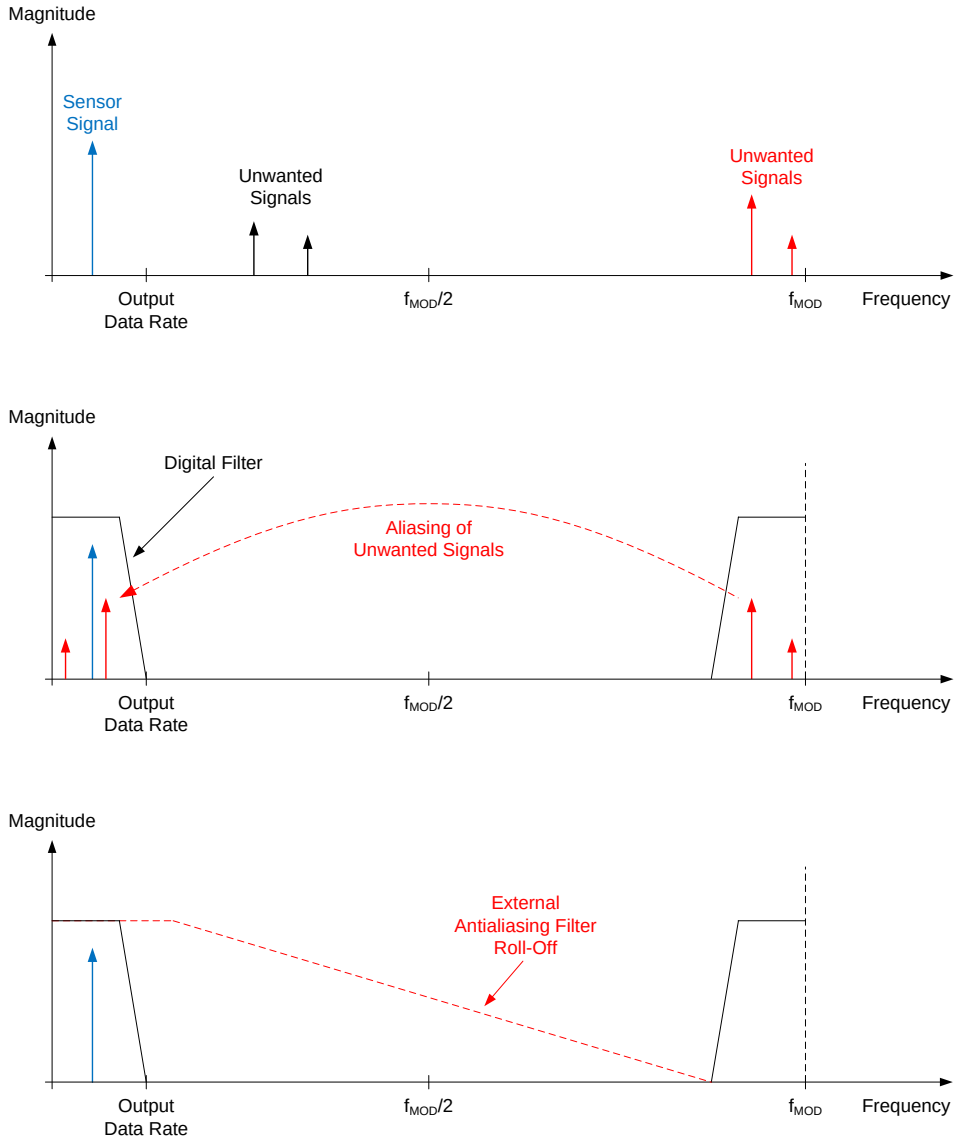


Figure 59. Effect of Aliasing

Voltage Reference

The device offers an integrated low-drift, 2.048-V reference. For applications that require a different reference voltage value or a ratiometric measurement approach, the device offers two differential reference inputs (REFP0, REFN0 and REFP1, REFN1). In addition, the analog supply (AVDD) can be used as a reference. The differential reference inputs allow freedom in the reference common-mode voltage. REFP0 and REFN0 are dedicated reference inputs whereas REFP1 and REFN1 are shared with inputs AIN0 and AIN3, respectively. The reference inputs are internally buffered to increase input impedance. Therefore, additional reference buffers are usually not required when using an external reference and the reference inputs do not load any external circuitry when used in ratiometric applications. The reference source is selected by two bits (VREF[1:0]) in the configuration register. By default, the internal reference is selected. The internal voltage reference requires less than 25 µs to fully settle after power-up, when coming out of power-down mode or when switching from an external reference source to the internal reference.

Clock Source

The device system clock can either be provided by the internal low-drift oscillator or by an external clock source on the CLK input. Connect the CLK pin to DGND before power-up or reset to activate the internal oscillator. Connecting an external clock to the CLK pin at any time deactivates the internal oscillator after two rising edges on the CLK pin are detected. The device then operates on the external clock. After the ADS1120 switches to the external clock, the device cannot be switched back to the internal oscillator without cycling the power supplies or sending a RESET command.

Excitation Current Sources

The device provides two matched programmable excitation current sources (IDACs) for RTD applications. The output current of the current sources can be programmed to 50 µA, 100 µA, 250 µA, 500 µA, 1000 µA, or 1500 µA using the respective bits (IDAC[2:0]) in the configuration register. Each current source can be connected to any of the analog inputs (AINx) as well as to any of the dedicated reference inputs (REFP0 and REFN0). Both current sources can also be connected to the same pin. Routing of the IDACs is configured by bits (I1MUX[2:0], I2MUX[2:0]) in the configuration register. Care should be taken not to exceed the compliance voltage of the IDACs. In other words, the voltage on the pin where the IDAC is routed to should be limited to ≤ (AVDD – 0.9 V), otherwise the specified accuracy of the IDAC current is not met. For three-wire RTD applications, the matched current sources can be used to cancel errors caused by sensor lead resistance (see the *RTD Measurement* section for more details).

The IDACs require up to 200 µs to start up after the IDAC current is programmed to the respective value using bits IDAC[2:0]. If configuration register 2 and 3 are not written during the same WREG command, TI recommends to first set the IDAC current to the respective value using bits IDAC[2:0] and thereafter select the routing for each IDAC (I1MUX[2:0], I2MUX[2:0]).

In single-shot mode, the IDACs remain active between any two conversions if the IDAC[2:0] bits are set to a value other than 000. However, the IDACs are powered down whenever the POWERDOWN command is issued.

Sensor Detection

To help detect a possible sensor malfunction, the device provides internal 10-µA, burn-out current sources. When enabled by setting the respective bit (BCS) in the configuration register, one current source sources current to the positive analog input (AIN_P) currently selected and the other current source sinks current form the selected negative analog input (AIN_N).

In case of an open circuit in the sensor, these burn-out current sources pull the positive input towards AVDD and the negative input towards AVSS, resulting in a full-scale reading. A full-scale reading may also indicate that the sensor is overloaded or that the reference voltage is absent. A near-zero reading may indicate a shorted sensor. Note that the absolute value of the burn-out current sources typically varies by ±10% and the internal multiplexer adds a small series resistance. Therefore, distinguishing a shorted sensor condition from a normal reading can be difficult, especially if an RC filter is used at the inputs. In other words, even if the sensor is shorted, the voltage drop across the external filter resistance and the residual resistance of the multiplexer causes the output to read a value higher than zero.

If a higher precision current source is required for sensor short detection, TI recommends using the excitation current sources (IDACs). Keep in mind that ADC readings of a functional sensor may be corrupted when the burn-out current sources are enabled.

Low-Side Power Switch

A low-side power switch with low on-resistance connected between the analog input AIN3/REFN1 and AVSS is integrated in the device as well. This power switch can be used to reduce system power consumption in bridge sensor applications by powering down the bridge circuit between conversions. When the respective bit (PSW) in the configuration register is set, the switch automatically closes when the START/SYNC command is sent and opens when the POWERDOWN command is issued. Note that the switch stays closed between conversions in single-shot mode in case the PSW bit is set to 1. The switch can be opened at any time by setting the PSW bit to 0. By default, the switch is always open.

System Monitor

The device provides some means for monitoring the AVDD analog power supply and the external voltage reference. To select any monitoring voltages, the internal multiplexer (MUX[3:0]) must be configured accordingly in the configuration register. The device automatically bypasses the PGA and sets the gain to 1, irrespective of the configuration register settings while the monitoring feature is used. Note that the system monitor function only provides a coarse result and is not meant to be a precision measurement.

When measuring the analog power supply (MUX[3:0] = 1101), the resulting conversion is approximately (AVDD – AVSS) / 4. The device uses the internal 2.048-V reference for the measurement regardless of what reference source is selected in the configuration register (VREF[1:0]).

When monitoring one of the two possible external reference voltage sources (MUX[3:0] = 1100), the result is approximately (V_{REFPx} – V_{REFNx}) / 4. REFPx and REFNx denote the external reference input pair selected in the configuration register (VREF[1:0]). The device automatically uses the internal reference for the measurement.

Offset Calibration

The internal multiplexer offers the option to short both PGA inputs (AIN_P and AIN_N) to mid-supply (AVDD + AVSS) / 2. This option can be used to measure and calibrate the device offset voltage by storing the result of the shorted input voltage reading in a microcontroller and consequently subtracting the result from each following reading. TI recommends taking multiple readings with the inputs shorted and averaging the result to reduce the effect of noise.

Power Supplies

The device requires two power supplies: analog (AVDD, AVSS) and digital (DVDD, DGND). The analog power supply can be bipolar (for example, AVDD = +2.5 V, AVSS = –2.5 V) or single supply (for example, AVDD = +3.3 V, AVSS = 0 V) and is independent of the digital power supply. The digital supply sets the digital I/O levels. The power supplies can be sequenced in any order but in no case should any analog or digital inputs exceed the respective analog or digital power-supply voltage limits.

Temperature Sensor

The temperature measurement mode of the device is configured as a 14-bit result when enabled by the TS bit in the configuration register. Data are output starting with the most significant byte (MSB). When reading the two data bytes, the first 14 bits are used to indicate the temperature measurement result. The last 2 bits are random data and must be ignored. That is, the 14-bit temperature result is left-justified within the 16-bit conversion result. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary twos complement format.

Table 8. 14-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	0FFF
100	00 1100 1000 0000	0C80
80	00 1010 0000 0000	0A00
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0	00 0000 0000 0000	0000
–0.25	11 1111 1111 1000	3FF8
–25	11 1100 1110 0000	3CE0
–55	11 1001 0010 0000	3920

Converting from Temperature to Digital Codes

For Positive Temperatures (for example, +50°C):

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 14-bit, left-justified format with the MSB = 0 to denote the positive sign.

Example: +50°C / (0.03125°C per count) = 1600 = 0640h = 00 0110 0100 0000

For Negative Temperatures (for example, –25°C):

Generate the twos complement of a negative number by complementing the absolute binary number and adding 1. Then, denote the negative sign with the MSB = 1.

Example: |–25°C| / (0.03125°C per count) = 800 = 0320h = 00 0011 0010 0000

Twos complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000

Converting from Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a 0 or a 1. If the MSB is a 0, simply multiply the decimal code by 0.03125°C to obtain the result. If the MSB = 1, subtract 1 from the result and complement all bits. Then, multiply the result by –0.03125°C.

Example: The device reads back 0960h: 0960h has an MSB = 0.

0960h · 0.03125°C = 2400 · 0.03125°C = +75°C

Example: The device reads back 3CE0h: 3CE0h has an MSB = 1.

Complement the result: 3CE0h → 0320h

0320h · 0.03125°C = 800 · 0.03125°C = –25°C

Reset and Power-Up

When the device powers up, a reset is performed. As part of the reset process, the device sets all bits in the configuration registers to the respective default settings. By default, the device is set to single-shot mode. After power-up, the device performs a single conversion using the default register settings and then enters a low-power state. The power-up behavior is intended to prevent systems with tight power-supply requirements from encountering a current surge during power-up. The reset process takes approximately 50 µs. After that, all internal circuitry (including the voltage reference) are stable and communication with the device is possible.

Conversion Modes

The device can be operated in one of two conversion modes that can be selected by the CM bit in the configuration register. These conversion modes are single-shot or continuous conversion mode.

Single-Shot Mode

In single-shot mode, the device only performs a conversion when a START/SYNC command is issued. The device consequently performs one single conversion and returns to a low-power state afterwards. The internal oscillator and all analog circuitry (except for the excitation current sources) are turned off while the device waits in this low-power state until the next conversion is started. In addition, every write access to any configuration register also starts a new conversion. Writing to any configuration register while a conversion is ongoing functions as a new START/SYNC command that stops the current conversion and restarts a single new conversion. Each conversion is fully settled (assuming the analog input signal settles to its final value before the conversion starts) because the device digital filter settles within a single cycle.

Continuous Conversion Mode

In continuous conversion mode, the device continuously performs conversions. When a conversion completes, the device places the result in the output buffer and immediately begins another conversion.

In order to start continuous conversion mode, the CM bit must be set to 1 followed by a START/SYNC command. The first conversion starts at $210 \cdot t_{CLK}$ (normal mode, duty-cycle mode) or $114 \cdot t_{CLK}$ (turbo mode) after the last SCLK falling edge of the START/SYNC command. Writing to any configuration register while the START/SYNC command is not issued starts a single conversion, whereas a write access to the configuration register during an ongoing conversion restarts the current conversion. TI recommends always sending a START/SYNC command immediately after the CM bit is set to 1.

Operating Modes

In addition to the different conversion modes, the device can also be operated in different operating modes that can be selected to trade-off power consumption, noise performance, and output data rate.

Normal Mode

Normal mode is the default mode that the device operates in. In this mode, the internal modulator of the ΔΣ ADC runs at a modulator clock frequency of $f_{MOD} = f_{CLK} / 16$, where the system clock (f_{CLK}) is either provided by the internal oscillator or the external clock source. The modulator frequency is 256 kHz when using the internal oscillator. Normal mode offers output data rate options ranging from 20 SPS to 1 kSPS with the internal oscillator. The data rate is selected by the DR[2:0] bits in the configuration register. In case an external clock source with a clock frequency other than 4.096 MHz is used, the data rates scale accordingly. For example, using an external clock with f_{CLK} = 2.048 MHz yields data rates ranging from 10 SPS to 500 SPS.

Duty-Cycle Mode

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator can be averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the device supports an automatic duty-cycle mode that can yield significant power savings by periodically entering a low-power state between conversions. In principle, the device runs in normal mode with a duty cycle of 25%. This functionality means the device performs one conversion in the same manner as when running in normal mode but then automatically enters a low power-state for three consecutive conversion cycles. The noise performance in duty-cycle mode is therefore comparable to the noise performance in normal mode at four times the data rate. Data rates in duty-cycle mode range from 5 SPS to 250 SPS with the internal oscillator.

Turbo Mode

Applications that require higher data rates up to 2 kSPS can operate the device in turbo mode. In this mode, the internal modulator runs at a higher frequency of $f_{MOD} = f_{CLK} / 8$. f_{MOD} equals 512 kHz when the internal oscillator or an external 4.096-MHz clock is used. Note that the device power consumption increases because the modulator runs at a higher frequency.

Power-Down Mode

When the POWERDOWN command is issued, the device enters power-down mode after completing the current conversion. In this mode, all analog circuitry (including the voltage reference and both IDACs) are powered down and the device typically only uses 400 nA of current. During this time, the device holds the configuration register settings and responds to commands, but does not perform any data conversion.

Issuing a START/SYNC command wakes up the device and either starts a single conversion or starts continuous conversion mode, depending on the conversion mode selected by the CM bit. Writing to any configuration register bit wakes up the device as well, but only starts a single conversion regardless of what conversion mode (CM) the device is set to.

Serial Interface

The SPI-compatible serial interface of the device is used to read conversion data, read and write the device configuration registers, and control device operation. Only SPI mode 1 (CPOL = 0, CPHA = 1) is supported. The interface consists of five control lines ($\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, and $\overline{DRDY}$) but can be used with four or even three control signals (SCLK, DIN, and DOUT/$\overline{DRDY}$) as well. In the latter case, $\overline{CS}$ may be tied low if the serial bus is not shared with any other device. The dedicated data-ready signal ($\overline{DRDY}$) can be configured to be shared with DOUT/$\overline{DRDY}$.

Chip Select ($\overline{CS}$)

Chip select ($\overline{CS}$) is an active-low input that selects the device for SPI communication. This feature is useful when multiple devices share the same serial bus. $\overline{CS}$ must remain low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK is ignored, and DOUT/$\overline{DRDY}$ enters a high-impedance state; as such, DOUT/$\overline{DRDY}$ cannot indicate when data are ready. In situations where multiple devices are present on the bus, the dedicated $\overline{DRDY}$ pin can provide an uninterrupted monitor of the result status. If the serial bus is not shared with another peripheral, $\overline{CS}$ can be tied low.

Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data into and out of the device on the DIN and DOUT/$\overline{DRDY}$ pins, respectively. Even though the input has hysteresis, TI recommends keeping SCLK as clean as possible to prevent glitches from accidentally shifting the data. If a complete command is not sent within $13955 \cdot t_{MOD}$ (normal mode, duty-cycle mode) or $27910 \cdot t_{MOD}$ (turbo mode), the serial interface resets and the next SCLK pulse starts a new communication cycle. This timeout feature can be used to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ indicates when a new conversion result is ready for retrieval. When $\overline{DRDY}$ falls low, new conversion data are ready. $\overline{DRDY}$ transitions back high on the next SCLK rising edge. When no data are read during continuous conversion mode, $\overline{DRDY}$ remains low but pulses high $2 \cdot t_{MOD}$ before the next $\overline{DRDY}$ falling edge. The $\overline{DRDY}$ pin is always actively driven, even when $\overline{CS}$ is high.

Data Input (DIN)

The data input pin (DIN) is used along with SCLK to send data (commands and register data) to the device. The device latches data on DIN on the SCLK falling edge. The device never drives the DIN pin.

Data Output and Data Ready (DOUT/$\overline{\text{DRDY}}$)

DOUT/$\overline{\text{DRDY}}$ serves a dual-purpose function. This pin is used with SCLK to read conversion and register data from the device. Data on DOUT/$\overline{\text{DRDY}}$ are shifted out on the SCLK rising edge. DOUT/$\overline{\text{DRDY}}$ goes to a high-impedance state when $\overline{\text{CS}}$ is high.

In addition, the DOUT/$\overline{\text{DRDY}}$ pin can also be configured as a data-ready indicator by setting DRDYM in the configuration register high. DOUT/$\overline{\text{DRDY}}$ then transitions low at the same time that the $\overline{\text{DRDY}}$ pin goes low to indicate new conversion data are available. Both signals can be used to detect if new data are ready. However, because DOUT/$\overline{\text{DRDY}}$ is disabled when $\overline{\text{CS}}$ is high, the recommended method of monitoring the end of a conversion when multiple devices are present on the SPI bus is to use the dedicated $\overline{\text{DRDY}}$ pin.

Data Format

The device provides 16 bits of data in binary twos complement format. The positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale (FS). Table 9 summarizes the ideal output codes for different input signals.

Table 9. Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} ($V_{AINP} - V_{AINN}$)	IDEAL OUTPUT CODE(1)
≥ +FS ($2^{15} - 1$) / 2^{15}	7FFFh
+FS / 2^{15}	0001h
0	0
–FS / 2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

Mapping of the analog input signal to the output codes is illustrated in Figure 60.

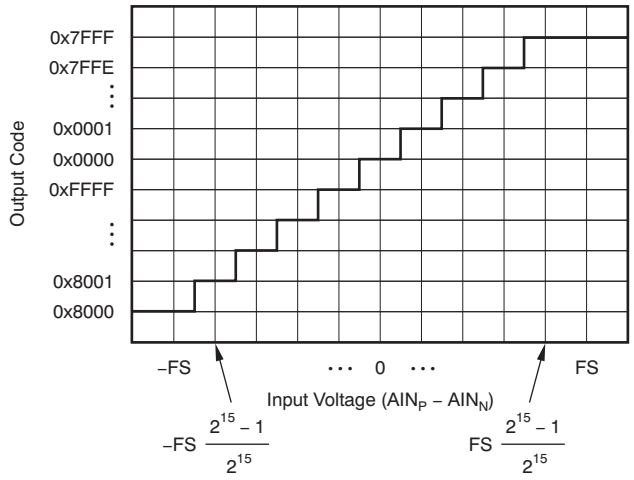


Figure 60. Code Transition Diagram

Commands

The device offers six different commands to control device operation, as shown in Table 10. Four commands are stand-alone instructions (RESET, START/SYNC, POWERDOWN, and RDATA). The commands to read (RREG) and write (WREG) configuration register data from and to the device require additional information as part of the instruction.

Table 10. Command Definitions(1)

COMMAND	DESCRIPTION	COMMAND BYTE
RESET	Reset the device	0000 011x
START/SYNC	Start or restart conversions	0000 100x
POWERDOWN	Enter power-down mode	0000 001x
RDATA	Read data by command	0001 xxxx
RREG	Read *nn* registers starting at address *rr*	0010 *rrnn*
WREG	Write *nn* registers starting at address *rr*	0100 *rrnn*

(1) Operands: rr = configuration register (00 to 11), nn = number of bytes – 1 (00 to 11), and x = don't care.

RESET (0000 011x)

Resets the device to the default values.

START/SYNC (0000 100x)

In single-shot mode, the START/SYNC command is used to start a single conversion or (when sent during an ongoing conversion) to reset the digital filter, and to restart a single new conversion. When the device is set to continuous conversion mode, the START/SYNC command must be issued one time to start converting continuously. Sending the START/SYNC command while converting in continuous conversion mode resets the digital filter and starts converting from there.

POWERDOWN (0000 001x)

The POWERDOWN command places the device into power-down mode. This command shuts down all internal analog components, opens the low-side switch, turns off both IDACs, but holds all register values. As soon as a START/SYNC command is issued, all analog components return to their previous states.

RDATA (0001 xxxx)

The RDATA command loads the output shift register with the most recent conversion result. This command can be used when DOUT/DRDY or DRDY are not monitored to indicate that a new conversion result is available. If a conversion finishes in the middle of the RDATA command byte, the more reliable result (either the old result or the new one) is loaded into the output shift register. The state of the DRDY pin signals whether the old or the new result is loaded. If the old result is loaded, DRDY stays low, indicating that the new result has not been read out. The new conversion result loads when DRDY is high.

RREG (0010 rrnn)

The RREG command reads the number of bytes specified by *nn* (number of bytes to be read – 1) from the device configuration register, starting at register address rr. The command is completed after nn + 1 bytes are clocked out after the RREG command byte. For example, the command to read three bytes (nn = 10) starting at configuration register 1 (rr = 01) is 0010 0110.

WREG (0100 rrnn)

The WREG command writes the number of bytes specified by *nn* (number of bytes to be written – 1) to the device configuration register, starting at register address rr. The command is completed after nn + 1 bytes are clocked in after the WREG command byte. For example, the command to write two bytes (nn = 01) starting at configuration register 0 (rr = 00) is 0100 0001. The configuration registers are updated on the last SCLK falling edge.

Reading Data

Output pins $\overline{\text{DRDY}}$ and DOUT/$\overline{\text{DRDY}}$ (if configured in the respective DRDYM configuration register bit) transition low when new data are ready for retrieval. The conversion data are written to an internal data buffer. Data can be read directly from this buffer on DOUT/$\overline{\text{DRDY}}$ when $\overline{\text{DRDY}}$ falls low without concern of data corruption. An RDATA command does not have to be sent. Data are shifted out on the SCLK rising edges, MSB first, and consist of two bytes of data.

Figure 61 to Figure 63 show the timing diagrams for reading conversion data in continuous conversion mode and single-shot mode when not using the RDATA command.

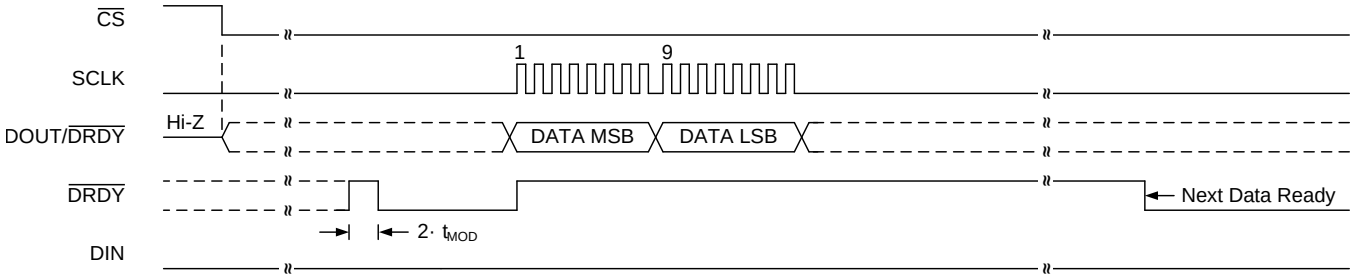


Figure 61. Continuous Conversion Mode (DRDYM = 0)

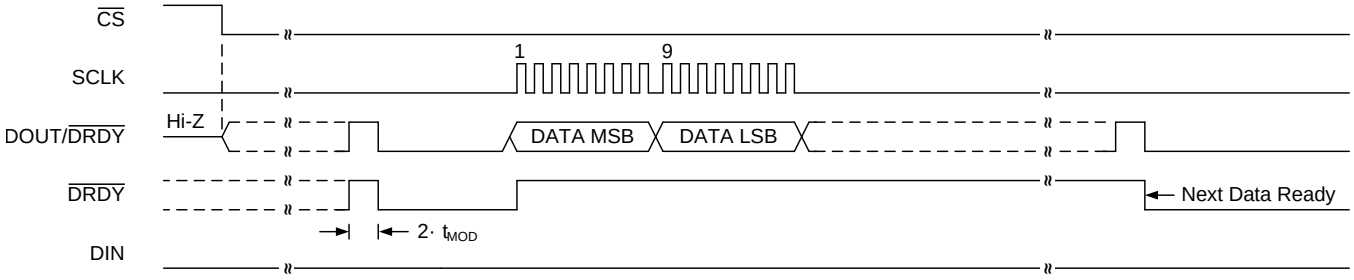


Figure 62. Continuous Conversion Mode (DRDYM = 1)

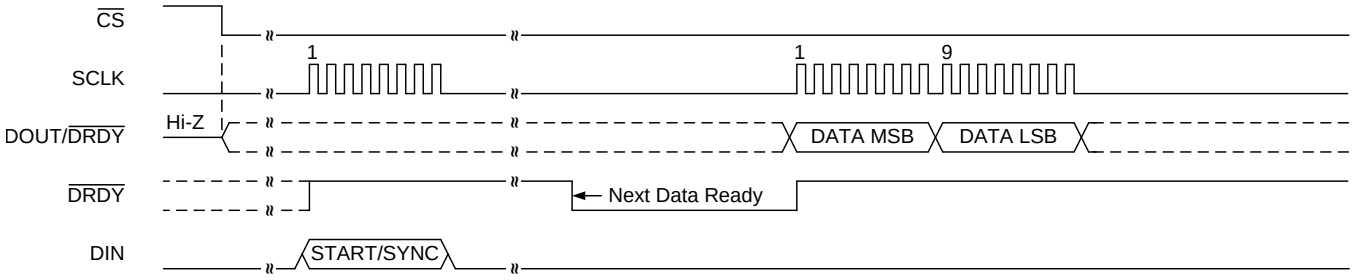


Figure 63. Single-Shot Mode (DRDYM = 0)

Data can also by read at any time without necessarily synchronizing to the $\overline{\text{DRDY}}$ signal with the RDATA command. When an RDATA command is issued, the conversion result currently stored in the data buffer can be shifted out on DOUT/$\overline{\text{DRDY}}$ on the following SCLK rising edge. Data can be read continuously with the RDATA command as an alternative to monitoring $\overline{\text{DRDY}}$ or DOUT/$\overline{\text{DRDY}}$. The $\overline{\text{DRDY}}$ pin must then be polled after the LSB is clocked out to determine if a new conversion result is loaded. If a new conversion completes during the read operation but data from the previous conversion are read, then $\overline{\text{DRDY}}$ is low. Otherwise, if the most recent result is read, $\overline{\text{DRDY}}$ is high. Figure 64 and Figure 65 illustrate the behavior for both cases.

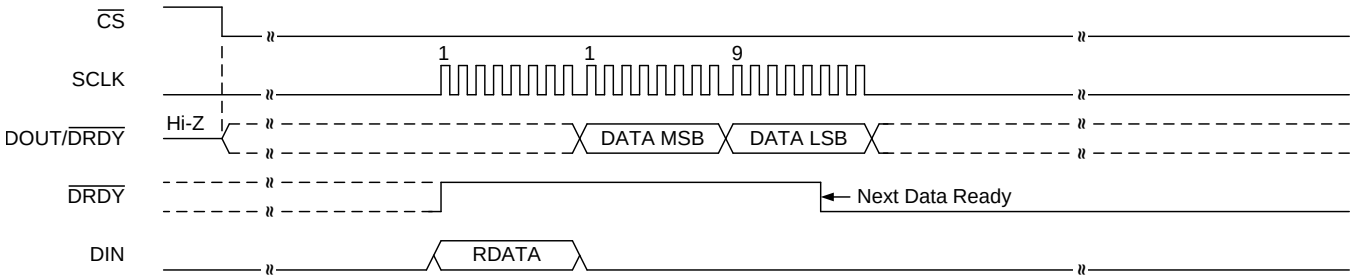


Figure 64. State of DRDY when a New Conversion Finishes During an RDATA Command

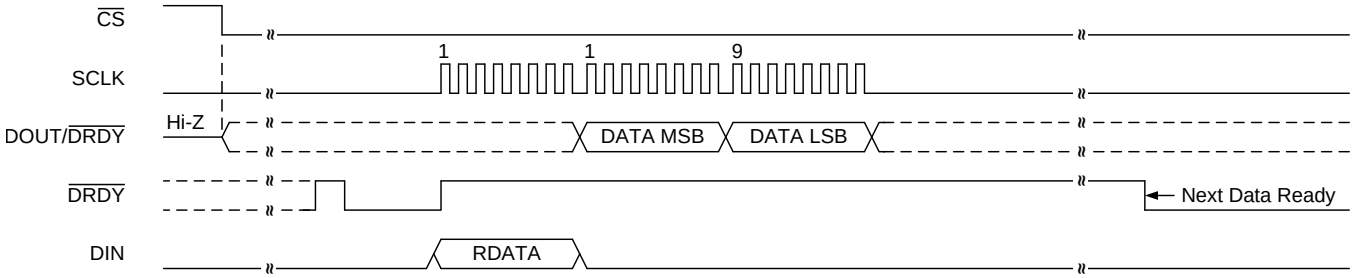


Figure 65. State of DRDY when the Most Recent Conversion Result is Read During an RDATA Command

Sending Commands

The device serial interface is capable of full-duplex operation while reading conversion data without using the RDATA command. Full-duplex operation means commands are decoded at the same time that conversion data are read. Commands can be sent on any 8-bit data boundary during a data read operation. When a RREG or RDATA command is recognized, the current data read operation is aborted and the conversion data are corrupted, unless the command is sent while the last byte of the conversion result is retrieved. The device starts to output the requested data on DOUT/DRDY at the first SCLK rising edge after the command byte. To read data without interruption, keep DIN low.

A WREG command can be sent without corrupting an ongoing read operation. Figure 66 shows an example for sending a WREG command to write two configuration registers while reading conversion data in continuous conversion mode. After the command is clocked in (after the 32nd SCLK falling edge), the device resets the digital filter and starts converting with the new register settings. The WREG command can be sent on any of the 8-bit boundaries.

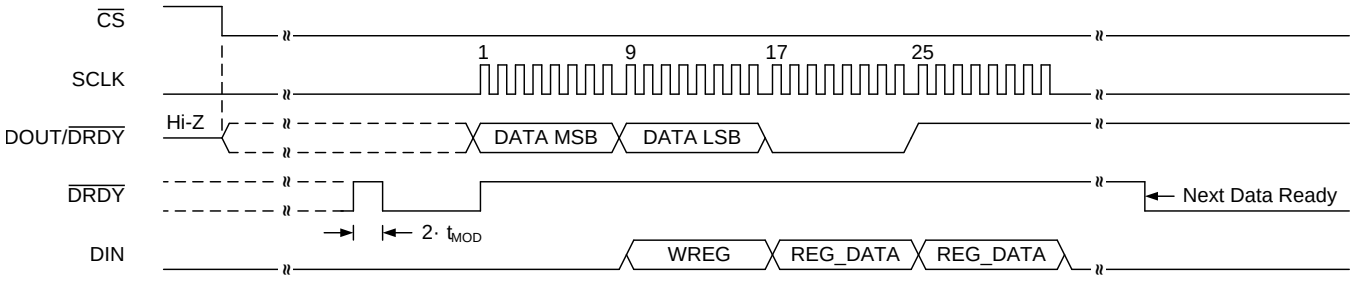


Figure 66. Example of a WREG Command

Note that the serial interface does not decode commands while an RDATA or RREG command is executed. That is, all 16 bits of the conversion result must be read after the RDATA command is issued and all requested registers must be read after a RREG command is sent before a new command can be issued.

Configuration Registers

The device has four 8-bit configuration registers that are accessible via the SPI port. The configuration registers control how the device operates and can be changed at any time without causing data corruption. After power-up and reset, all registers are set to the default values (which are all 0). Table 11 shows the register map of the configuration register.

Table 11. Configuration Register Map (Read/Write)

REGISTER (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	MUX[3:0]				GAIN[2:0]			PGA_BYPASS
01h	DR[2:0]			MODE[1:0]		CM	TS	BCS
02h	VREF[1:0]		50/60[1:0]		PSW	IDAC[2:0]		
03h	I1MUX[2:0]			I2MUX[2:0]			DRDYM	RESERVED

00h **Configuration Register 0**

Bits[7:4] **MUX[3:0]: Input multiplexer configuration**

These bits configure the input multiplexer and have no effect when in temperature sensor mode.
For settings where AIN_N = AVSS, the PGA must be disabled (PGA_BYPASS = 1) and only gains 1, 2, and 4 can be used.

0000 : AIN_P = AIN0, AIN_N = AIN1 (default)
0001 : AIN_P = AIN0, AIN_N = AIN2
0010 : AIN_P = AIN0, AIN_N = AIN3
0011 : AIN_P = AIN1, AIN_N = AIN2
0100 : AIN_P = AIN1, AIN_N = AIN3
0101 : AIN_P = AIN2, AIN_N = AIN3
0110 : AIN_P = AIN1, AIN_N = AIN0
0111 : AIN_P = AIN3, AIN_N = AIN2
1000 : AIN_P = AIN0, AIN_N = AVSS
1001 : AIN_P = AIN1, AIN_N = AVSS
1010 : AIN_P = AIN2, AIN_N = AVSS
1011 : AIN_P = AIN3, AIN_N = AVSS
1100 : (V_{REFPx} – V_{REFNx}) / 4 monitor (PGA bypassed)
1101 : (AVDD – AVSS) / 4 monitor (PGA bypassed)
1110 : AIN_P and AIN_N shorted to (AVDD + AVSS) / 2
1111 : Not used

Bits[3:1] **GAIN[2:0]: Gain configuration**

These bits configure the device gain.
Gains 1, 2, and 4 can be used without the PGA. In this case, gain is obtained by a switched-capacitor structure.
The gain setting has no effect when in temperature sensor mode.

000 : Gain = 1 (default)
001 : Gain = 2
010 : Gain = 4
011 : Gain = 8
100 : Gain = 16
101 : Gain = 32
110 : Gain = 64
111 : Gain = 128

Bit 0 **PGA_BYPASS: Disables internal low-noise PGA**

Disabling the PGA reduces overall power consumption and allows the common-mode voltage range (V_{CM}) to include AVSS and AVDD.
The PGA can only be disabled for gains 1, 2, and 4.
The PGA is always enabled for gain settings 8 to 128, regardless of the PGA_BYPASS setting.

0 : PGA enabled (default)
1 : PGA disabled and bypassed

01h **Configuration Register 1**

Bits[7:5] **DR[2:0]: Data rate**

These bits control the data rate setting depending on the selected operating mode.

Normal mode	Duty-cycle mode	Turbo mode
000 : 20 SPS (default)	000 : 5 SPS	000 : 40 SPS
001 : 45 SPS	001 : 11.25 SPS	001 : 90 SPS
010 : 90 SPS	010 : 22.5 SPS	010 : 180 SPS
011 : 175 SPS	011 : 44 SPS	011 : 350 SPS
100 : 330 SPS	100 : 82.5 SPS	100 : 660 SPS
101 : 600 SPS	101 : 150 SPS	101 : 1200 SPS
110 : 1000 SPS	110 : 250 SPS	110 : 2000 SPS
111 : Not used	111 : Not used	111 : Not used

Bits[4:3] **MODE[1:0]: Operating mode**

This bit controls the operating mode the device operates in.

00 : Normal mode (256-kHz modulator clock, default)
01 : Duty-cycle mode (internal duty cycle of 1:4)
10 : Turbo mode (512-kHz modulator clock)
11 : Not used

Bit 2 **CM: Conversion mode**

This bit sets the conversion mode for the device.

0 : Single-shot mode (default)
1 : Continuous conversion mode

Bit 1 **TS: Temperature sensor mode**

This bit enables the internal temperature sensor and puts the device in temperature sensor mode.

0 : Disables temperature sensor (default)
1 : Enables temperature sensor

Bit 0 **BCS: Burn-out current sources**

This bit controls the 10-µA, burn-out current sources to detect wire breaks and shorts in the sensor.

0 : Current sources off (default)
1 : Current sources on

02h **Configuration Register 2**

Bits[7:6] **VREF[1:0]: Voltage reference selection**

These bits select the voltage reference that is used for the conversion.

00 : Internal 2.048-V reference selected (default)
01 : External reference selected using dedicated REFP0 and REFN0 inputs
10 : External reference selected using AIN0/REFP1 and AIN3/REFN1 inputs
11 : Analog supply AVDD used as reference

Bits[5:4] **50/60[1:0]: FIR filter configuration**

These bits configure the filter coefficients for the internal FIR filter.
These bits only affect the 20-SPS setting in normal mode and 5-SPS setting in duty-cycle mode.

00 : No 50-Hz or 60-Hz rejection (default)
01 : Simultaneous 50-Hz and 60-Hz rejection
10 : 50-Hz rejection only
11 : 60-Hz rejection only

Bit 3 **PSW: Low-side power switch configuration**

This bit configures the behavior of the low-side switch connected to AIN3/REFN1.

0 : Switch is always open (default)
1 : Switch automatically closes when the START/SYNC command is sent and opens when the POWERDOWN command is issued

Bits[2:0] **IDAC[2:0]: IDAC current setting**

These bits set the current for both IDAC1 and IDAC2 excitation current sources.

000 : Off (default)
001 : Not used
010 : 50 µA
011 : 100 µA
100 : 250 µA
101 : 500 µA
110 : 1000 µA
111 : 1500 µA

03h	**Configuration Register 3**
Bits[7:5]	**I1MUX[2:0]: IDAC1 routing configuration**
	These bits select the channel where IDAC1 is routed to. 000 : IDAC1 disabled (default) 001 : IDAC1 connected to AIN0/REFP1 010 : IDAC1 connected to AIN1 011 : IDAC1 connected to AIN2 100 : IDAC1 connected to AIN3/REFN1 101 : IDAC1 connected to REFP0 110 : IDAC1 connected to REFN0 111 : Not used
Bits[4:2]	**I2MUX[2:0]: IDAC2 routing configuration**
	These bits select the channel where IDAC2 is routed to. 000 : IDAC2 disabled (default) 001 : IDAC2 connected to AIN0/REFP1 010 : IDAC2 connected to AIN1 011 : IDAC2 connected to AIN2 100 : IDAC2 connected to AIN3/REFN1 101 : IDAC2 connected to REFP0 110 : IDAC2 connected to REFN0 111 : Not used
Bit 1	**DRDYM: $\overline{\text{DRDY}}$ mode**
	This bit controls the behavior of the DOUT/$\overline{\text{DRDY}}$ pin when new data are ready. 0 : Only the dedicated $\overline{\text{DRDY}}$ pin is used to indicate when data are ready (default) 1 : Data ready is indicated simultaneously on DOUT/$\overline{\text{DRDY}}$ and $\overline{\text{DRDY}}$
Bit 0	**Reserved**
	Always write 0

Application Information

The following sections give example circuits and suggestions for using the device in various situations.

Basic Connections and Layout Considerations

For many applications, connecting the device is simple. Figure 67 shows the principle power-supply and interface connections for the ADS1120.

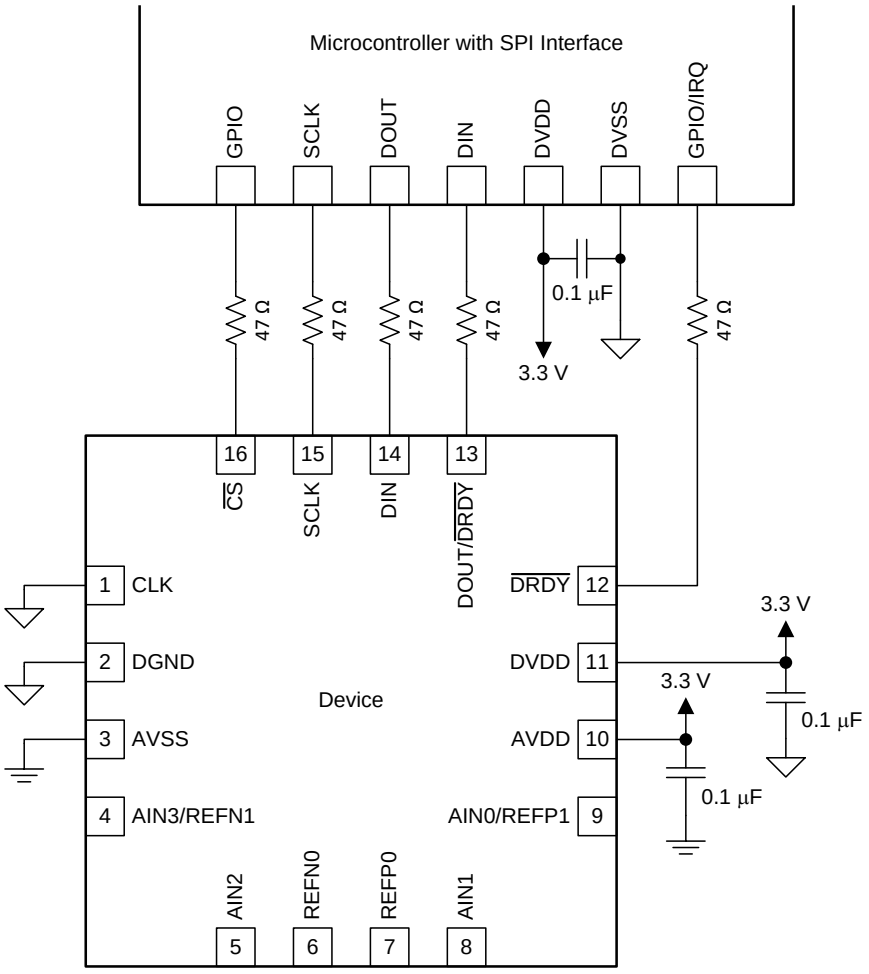


Figure 67. Power-Supply and Interface Connections

Most microcontroller SPI peripherals can operate with the ADS1120. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the device can be found in the SPI Timing Characteristics.

TI recommends placing 47-Ω resistors in series with all digital input and output pins ($\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, and $\overline{DRDY}$). This resistance smooths sharp transitions, suppresses overshoot, and offers some overvoltage protection. Care must be taken to still meet all SPI timing requirements because the additional resistors interact with the bus capacitances present on the digital signal lines.

Good power-supply decoupling is important to achieve optimum performance. Both AVDD and DVDD should be decoupled with at least a 0.1-µF bypass capacitor each. The bypass capacitors should be placed as close to the power-supply pins as possible with a low impedance connection. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the bypass capacitor may offer superior bypass and noise immunity.

TI recommends employing best design practices when laying out a printed circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout should separate analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in Figure 68. While Figure 68 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

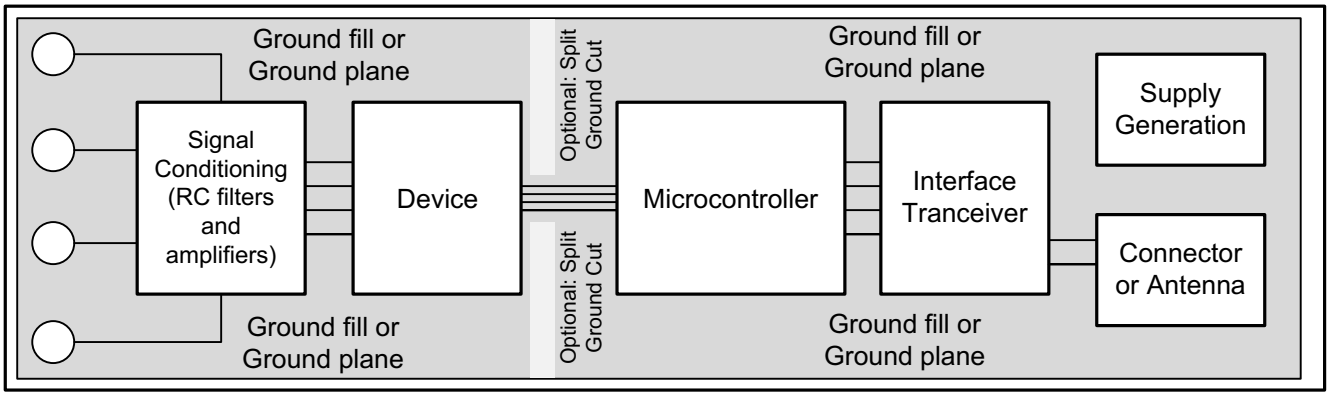


Figure 68. System Component Placement

The use of split analog and digital ground planes is not necessary for improved noise performance (although for thermal isolation this option is a worthwhile consideration). However, the use of a solid ground plane or ground fill in PCB areas with no components is essential for optimum performance. If the system being used employs a split digital and analog ground plane, TI generally recommends that the ground planes be connected together as close to the device as possible.

TI also strongly recommends that digital components, especially RF portions, be kept as far as practically possible from analog circuitry in a given system. Additionally, minimize the distance that digital control traces run through analog areas and avoid placing these traces near sensitive analog components. Digital return currents usually flow through a ground path that is as close to the digital path as possible. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature-sensing functions are much more significant than for ADC functions.

Connecting Multiple Devices

When connecting multiple ADS1120 devices to a single SPI bus, SCLK, DIN, and DOUT/$\overline{\text{DRDY}}$ can be safely shared by using a dedicated chip-select ($\overline{\text{CS}}$) line for each SPI-enabled device. When $\overline{\text{CS}}$ transitions high for the respective device, DOUT/$\overline{\text{DRDY}}$ enters a 3-state mode. Therefore, DOUT/$\overline{\text{DRDY}}$ cannot be used to indicate when new data are available if $\overline{\text{CS}}$ is high, regardless if the DRDYM bit in the configuration register is set to 0 or 1. Only the dedicated $\overline{\text{DRDY}}$ pin indicates that new data are available, because the $\overline{\text{DRDY}}$ pin is actively driven even when $\overline{\text{CS}}$ is high.

In some cases, however, the $\overline{\text{DRDY}}$ pin cannot be interfaced to the microcontroller. This scenario can occur if there are insufficient GPIO channels available on the microcontroller or if the serial interface must be galvanically isolated and thus the amount of channels must be limited. Therefore, in order to evaluate when a new conversion of one of the devices is ready, the microcontroller can periodically drop $\overline{\text{CS}}$ to the respective device and poll the state of the DOUT/$\overline{\text{DRDY}}$ pin. When $\overline{\text{CS}}$ goes low, the DOUT/$\overline{\text{DRDY}}$ pin immediately drives either high or low, provided that the DRDYM bit is configured to 1. If the DOUT/$\overline{\text{DRDY}}$ line drives low on a low $\overline{\text{CS}}$, new data are currently available for clocking out. If the DOUT/$\overline{\text{DRDY}}$ line drives high, no new data are available. For this procedure to work properly, 16 additional SCLKs must be sent after each data read operation to make sure DOUT/$\overline{\text{DRDY}}$ is taken high before a new conversion completes. Alternatively, valid data can be retrieved from the device at any time without concern of data corruption by using the RDATA command.

Thermocouple Measurement

Figure 69 shows the basic connections of a thermocouple measurement system, when using the internal high-precision temperature sensor for cold-junction compensation. Apart from the thermocouple itself, the only external circuitry required are two biasing resistors, a simple low-pass, antialiasing filter, and the power-supply decoupling capacitors.

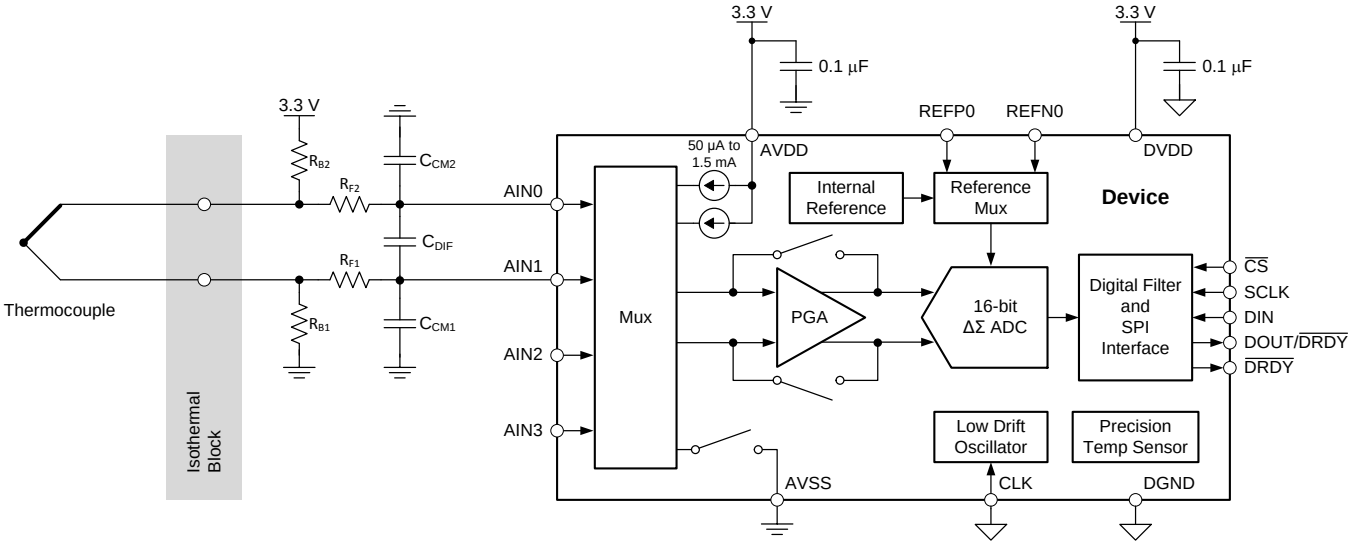


Figure 69. Thermocouple Measurement

The biasing resistors R_{B1} and R_{B2} are used to set the common-mode voltage of the thermocouple to within the specified common-mode voltage range of the PGA (in this example, to mid-supply AVDD / 2). If the application requires the thermocouple to be biased to GND, either a bipolar supply (for example, AVSS = –2.5 V and AVDD = +2.5 V) must be used for the device to meet the common-mode voltage requirement of the PGA, or the PGA must be bypassed. When choosing the values of the biasing resistors, care must be taken so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops in the thermocouple leads.

In addition to biasing the thermocouple, R_{B1} and R_{B2} are also useful to detect an open thermocouple lead. When one of the thermocouple leads fails open, the biasing resistors pull the analog inputs AIN0 and AIN1 to AVDD and AVSS, respectively. The ADC consequently reads a full-scale value, which is outside the normal measurement range of the thermocouple voltage, to indicate this failure condition.

While the device digital filter attenuates high-frequency components of noise, TI generally recommends providing a first-order, passive RC filter at the inputs to further improve performance. The differential RC filter formed by R_{F1}, R_{F2}, and the differential capacitor C_{DIF} offers a cutoff frequency of $f_C = 1 / [2\pi \cdot (R_{F1} + R_{F2}) \cdot C_{DIF}]$. Two common-mode filter capacitors C_{M1} and C_{M2} are also added to offer attenuation of high-frequency, common-mode noise components. TI recommends that the differential capacitor C_{DIF} be at least an order of magnitude (10x) larger than the common-mode capacitors C_{M1} and C_{M2} because mismatches in the common-mode capacitors can cause differential noise.

The filter resistors R_{F1} and R_{F2} also serve as current-limiting resistors. These resistors limit the current into the analog inputs (AIN0 and AIN1) of the device to safe levels, should an overvoltage on the inputs occur. Care should be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. TI recommends limiting the filter resistor values to below 1 kΩ.

The device integrates a high-precision temperature sensor that can be used to measure the temperature of the cold junction. To measure the internal temperature of the ADS1120, the device must be set to internal temperature sensor mode by setting the TS bit to 1 in the configuration register. For best performance, careful board layout is critical to achieve good thermal conductivity between the cold junction and the device package.

However, the device does not perform automatic cold-junction compensation of the thermocouple. This compensation must be done in the microcontroller that interfaces to the device. The microcontroller requests one or multiple readings of the thermocouple voltage from the device and then sets the device to internal temperature sensor mode (TS = 1) to acquire the temperature of the cold junction. The calculations to compensate for the cold-junction temperature must be implemented on the microcontroller.

In some applications, the integrated temperature sensor cannot be used (for example, if the accuracy is not high enough or if the device cannot be placed close enough to the cold junction). The additional analog input channels of the device can be used in this case to measure the cold-junction temperature with a thermistor, RTD, or an analog temperature sensor.

RTD Measurement

The device integrates all necessary features (such as dual-matched programmable current sources, buffered reference inputs, PGA, and so forth) to ease the implementation of ratiometric 2-, 3-, and 4-wire RTD measurements. Figure 70 shows a typical implementation of a ratiometric 3-wire RTD measurement using the excitation current sources integrated in the device to excite the RTD as well as to implement automatic RTD lead-resistance compensation.

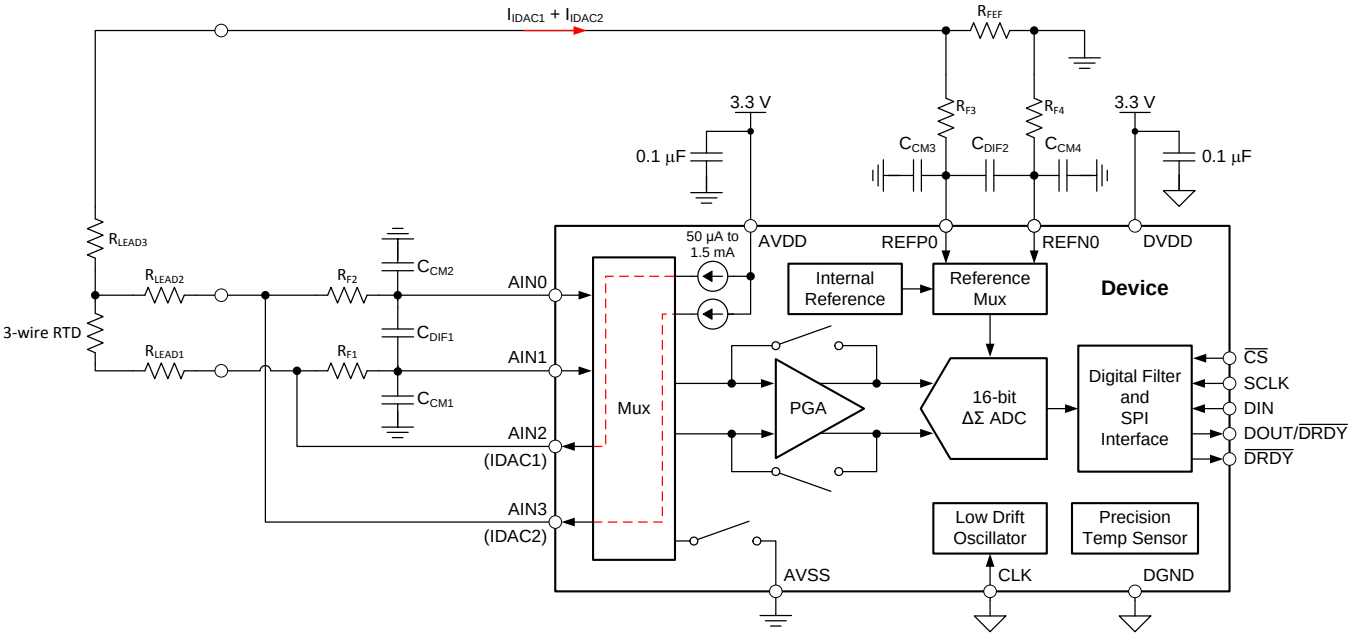


Figure 70. 3-Wire RTD Measurement

The circuit in Figure 70 employs a ratiometric measurement approach. In other words, the sensor signal (that is, the voltage across the RTD in this case) and the reference voltage for the ADC are derived from the same excitation source. Therefore, errors resulting from temperature drift or noise cancel out because these errors are common to both the sensor signal and the reference.

In order to implement a ratiometric 3-wire RTD measurement using the device, IDAC1 is routed to one of the excitation leads of the RTD while IDAC2 is routed to the second excitation lead. Both currents have the same value, which is programmable by the IDAC[2:0] bits in the configuration register. The design of the device ensures that both IDAC values are closely matched, even across temperature. The sum of both currents flows through a precision, low-drift reference resistor, R_{REF}. The voltage, V_{REF}, generated across the reference resistor is as shown in Equation 16. Equation 17 is then used as the ADC reference voltage because $I_{IDAC1} = I_{IDAC2}$.

$$V_{REF} = (I_{IDAC1} + I_{IDAC2}) \cdot R_{REF} \quad (16)$$

$$V_{REF} = 2 \cdot I_{IDAC1} \cdot R_{REF} \quad (17)$$

Equation 18 assumes for the moment that the individual lead resistance values of the RTD (R_{LEADx}) are zero. Only IDAC1 excites the RTD to produce a voltage (V_{RTD}), which is proportional to the temperature-dependable RTD value and the IDAC1 value.

$$V_{RTD} = R_{RTD}\,(\text{Temperature}) \cdot I_{IDAC1} \tag{18}$$

The device internally amplifies the voltage across the RTD using the PGA and compares the resulting voltage against the reference voltage to produce a digital output code, which is proportional to Equation 19 through Equation 21:

$$\text{Code} \propto V_{RTD} \cdot \text{Gain} / V_{REF} \tag{19}$$

$$\text{Code} \propto [R_{RTD}\,(\text{Temperature}) \cdot I_{IDAC1} \cdot \text{Gain}] / [2 \cdot I_{IDAC1} \cdot R_{REF}] \tag{20}$$

$$\text{Code} \propto [R_{RTD}\,(\text{Temperature}) \cdot \text{Gain}] / [2 \cdot R_{REF}] \tag{21}$$

As can be seen from Equation 21, the output code only depends on the value of the RTD, the PGA gain, and the reference resistor (R_{REF}), but not on the IDAC1 value. The absolute accuracy and temperature drift of the excitation current therefore does not matter. However, because the value of the reference resistor directly impacts the measurement result, choosing a reference resistor with a very low temperature coefficient is important to limit errors introduced by the temperature drift of R_{REF}.

The second IDAC2 is used to compensate for errors introduced by the voltage drop across the lead resistance of the RTD. All three leads of a 3-wire RTD typically have the same length and, thus, the same lead resistance. Also, IDAC1 and IDAC2 have the same value. Consequently, the differential voltage (V_{IN}) across the ADC inputs, AIN0 and AIN1, is as shown in Equation 22:

$$V_{IN} = V_{AIN0} - V_{AIN1} = I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1}) - I_{IDAC2} \cdot R_{LEAD2} \tag{22}$$

When $R_{LEAD1} = R_{LEAD2}$ and $I_{IDAC1} = I_{IDAC2}$, Equation 22 reduces to Equation 23:

$$V_{IN} = I_{IDAC1} \cdot R_{RTD} \tag{23}$$

In other words, the measurement error resulting from the voltage drop across the RTD lead resistance is compensated, as long as the lead resistance values and the IDAC values are well matched.

A first-order differential and common-mode RC filter (R_{F1}, R_{F2}, C_{DIF1}, C_{CM1}, and C_{CM2}) is placed on the ADC inputs, as well as on the reference inputs (R_{F3}, R_{F4}, C_{DIF2}, C_{CM3}, and C_{CM4}). The same guidelines for designing the input filter apply as described in the *Thermocouple Measurement* section. For best performance, TI recommends matching the corner frequencies of the input and reference filter. More detailed information on matching the input and reference filter can be found in application report *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248* (SBAA201).

The reference resistor R_{REF} not only serves to generate the reference voltage for the device, but also sets the common-mode voltage of the RTD to within the specified common-mode voltage range of the PGA. In other words, the voltage across the reference resistor must meet Equation 13 through Equation 15.

When designing the circuit, care should also be taken to meet the compliance voltage requirement of the IDACs. The IDACs require a minimum headroom of (AVDD – 0.9 V) in order to operate accurately. This requirement means that Equation 24 must be met at all times.

$$\text{AVSS} + I_{IDAC1} \cdot (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \cdot (R_{LEAD3} + R_{REF}) \le \text{AVDD} - 0.9\ \text{V} \tag{24}$$

The device also offers the possibility to route the IDACs to the same inputs used for measurement. If the filter resistor values R_{F1} and R_{F2} are small enough and well matched, IDAC1 can be routed to AIN1 and IDAC2 to AIN0 in Figure 70. In this manner, even two 3-wire RTDs sharing the same reference resistor can be measured with a single device.

Implementing a 2- or 4-wire RTD measurement is very similar to the 3-wire RTD measurement shown in Figure 70, except that only one IDAC is required. Figure 71 and Figure 72 show typical circuit implementations of a 2-wire and 4-wire RTD measurement, respectively.

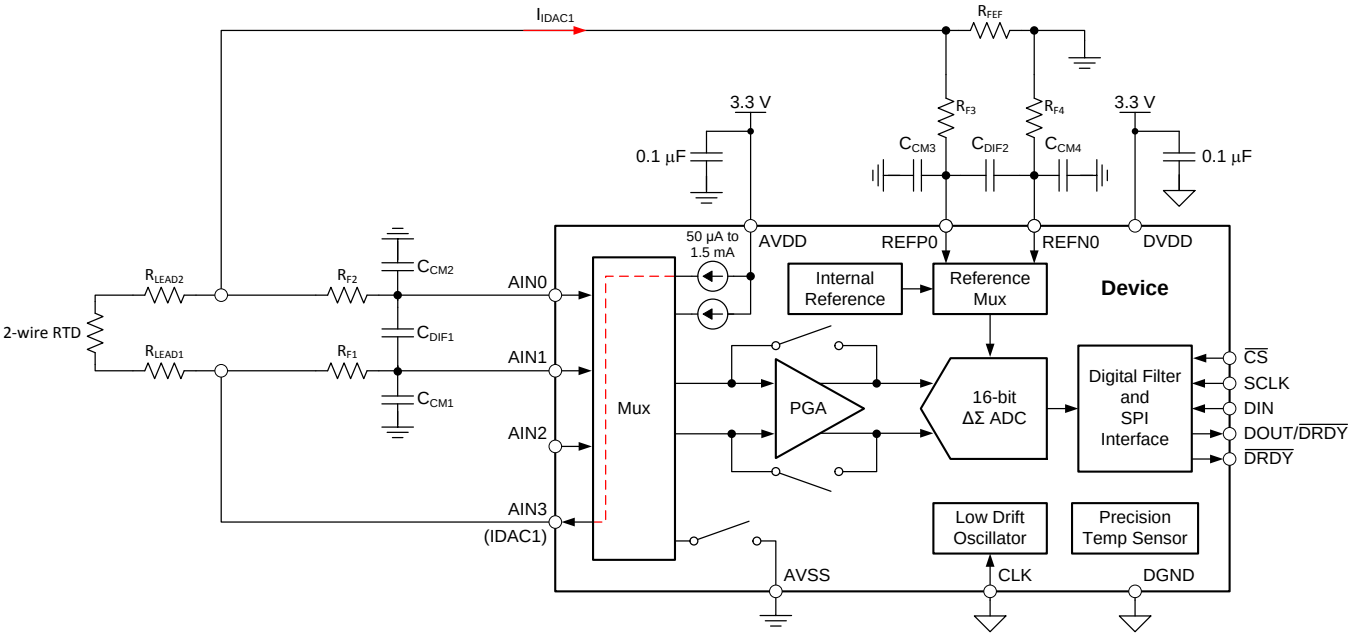


Figure 71. 2-Wire RTD Measurement

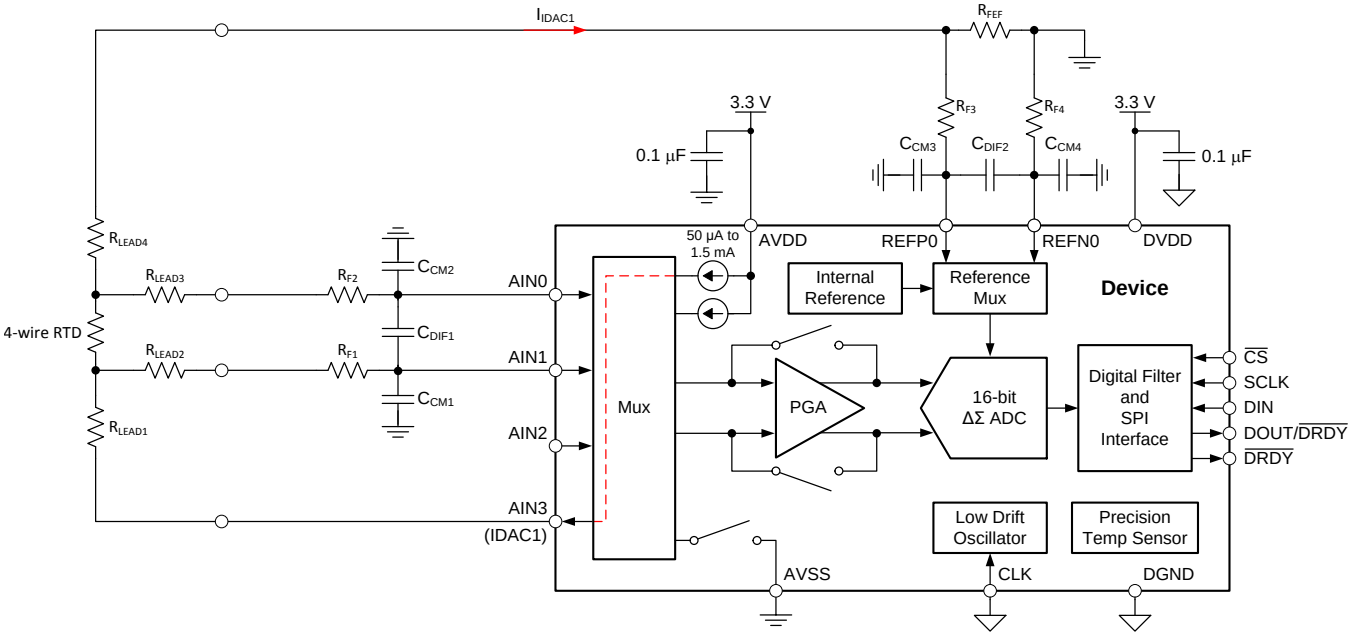


Figure 72. 4-Wire RTD Measurement

Bridge Measurement

The device offers several features to ease the implementation of ratiometric bridge measurements (such as a PGA with gains up to 128 V/V, buffered, differential reference inputs, and a low-side power switch).

To implement a ratiometric bridge measurement, the bridge excitation voltage is simultaneously used as the reference voltage for the ADC, as shown in Figure 73. With this configuration, any drift in excitation voltage also shows up on the reference voltage, consequently canceling out drift error. Either of the two device reference input pairs can be connected to the bridge excitation voltage. However, only the negative reference input (REFN1) can be internally routed to a low-side power switch. By connecting the low side of the bridge to REFN1, the device can automatically power down the bridge by opening the low-side power switch. When the PSW bit in the configuration register is set to 1, the device opens the switch every time a POWERDOWN command is issued and closes the switch again when a START/SYNC command is sent.

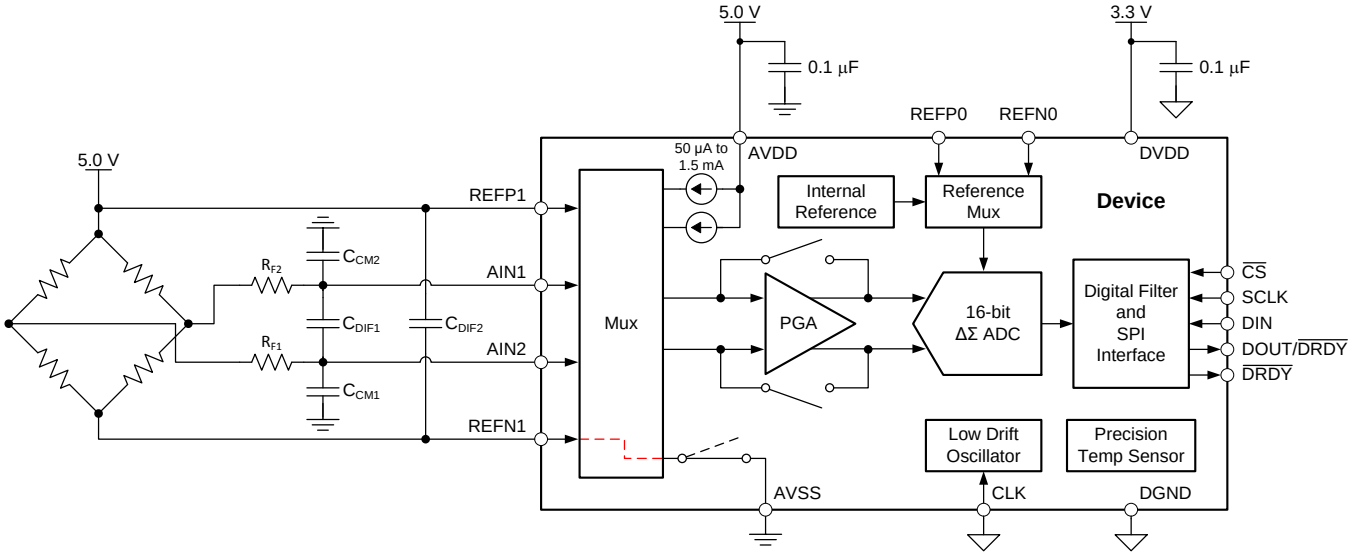


Figure 73. Bridge Measurement

The PGA offers gains up to 128 V/V, which helps to amplify the small differential bridge output signal to make optimal use of the ADC full-scale range. Using a symmetrical bridge with the excitation voltage equal to the supply voltage of the device ensures that the output signal of the bridge meets the common-mode voltage requirement of the PGA.

Note that the maximum input voltage is limited to $V_{IN\ (MAX)}$ = [(AVDD – AVSS) – 0.4 V] / gain, which means the entire full-scale range [FS = (AVDD – AVSS) / gain] cannot be used in this configuration. This limitation is a result of the output drive capability of the PGA amplifiers (A1 and A2); see Figure 39. The output of each amplifier must stay 200 mV away from the rails (AVDD and AVSS), otherwise the PGA becomes nonlinear. Consequently, the maximum output swing of the PGA is limited to V_{OUT} = (AVDD – AVSS) – 0.4 V.

Pseudo Code Example

The following list shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the device, in order to take subsequent readings from the ADS1120 in continuous conversion mode. The dedicated $\overline{DRDY}$ pin is used to indicate availability of new conversion data. The default configuration register settings are changed to gain = 16, continuous conversion mode, and simultaneous 50-Hz and 60-Hz rejection.

```
Power-up;
Delay;
Configure the SPI interface of the microcontroller to SPI mode 1 (CPOL = 0, CPHA = 1);
If the CS pin is not tied low permanently, configure the microcontroller GPIO connected to CS as an output;
Configure the microcontroller GPIO connected to the DRDY pin as an interrupt input;
Set CS to the device low;
Delay;
Send the RESET command (06h) to make sure the device is properly reset after power-up;
Write the respective register configuration with the WREG command (43h, 08h, 04h, 10h, and 00h);
Delay;
As a sanity check, read back all configuration registers with the RREG command (23h);
Delay;
Send the START/SYNC command (08h) to start converting in continuous conversion mode;
Delay;
Clear CS to high (resets the serial interface);
Loop
    {
    Wait for DRDY to transition low;
    Take CS low;
    Delay;
    Send 16 SCLK rising edges to read out conversion data on DOUT;
    Delay;
    Clear CS to high;
    }
Take CS low;
Delay;
Send the POWERDOWN command (02h) to stop conversions and put the device in power-down mode;
Delay;
Clear CS to high;
```

TI recommends running an offset calibration before performing any measurements or when changing the gain of the PGA. The internal offset of the device can, for example, be measured by shorting the inputs to mid-supply (MUX[3:1] = 1110). The microcontroller then takes multiple readings from the device with the inputs shorted and stores the average value in the microcontroller memory. When measuring the sensor signal, the microcontroller then subtracts the stored offset value from each device reading to obtain an offset compensated result.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2013) to Revision A	Page
• Released to production	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1120IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS1120	Samples
ADS1120IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS1120	Samples
ADS1120IRVAR	PREVIEW	VQFN	RVA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125		
ADS1120IRVAT	PREVIEW	VQFN	RVA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

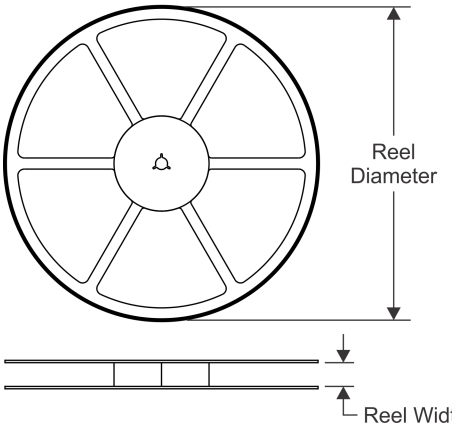
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

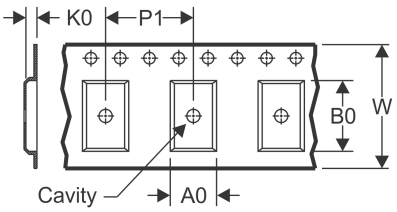
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

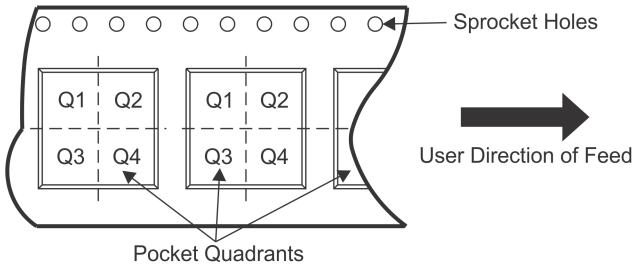


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

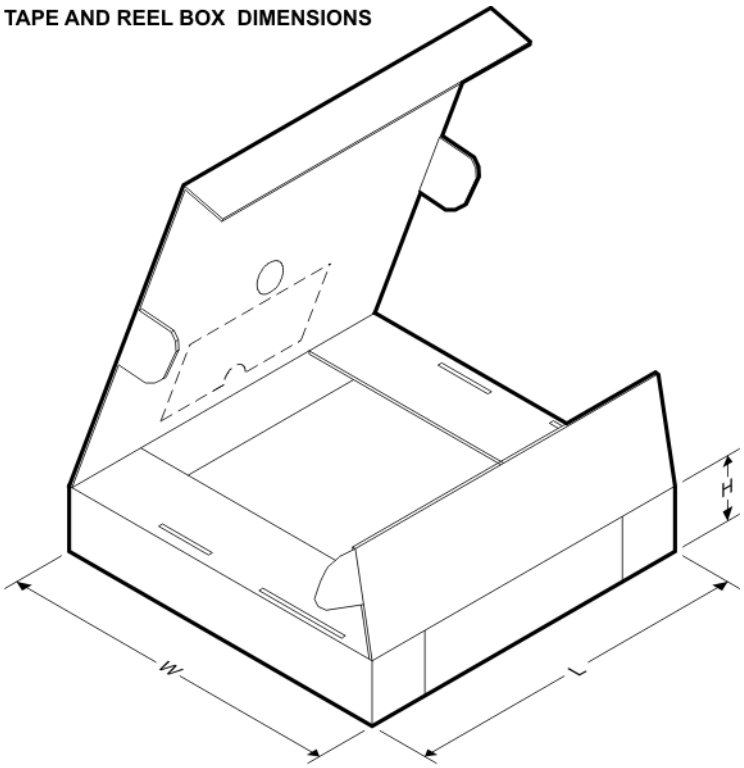
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1120IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

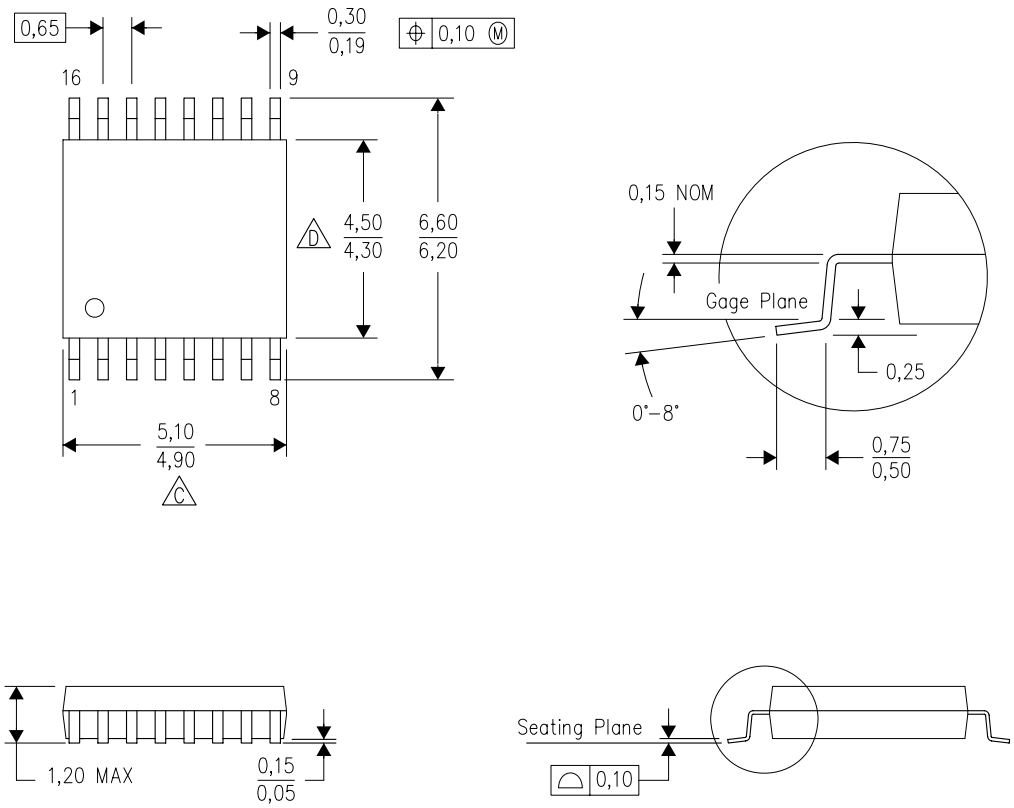
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1120IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

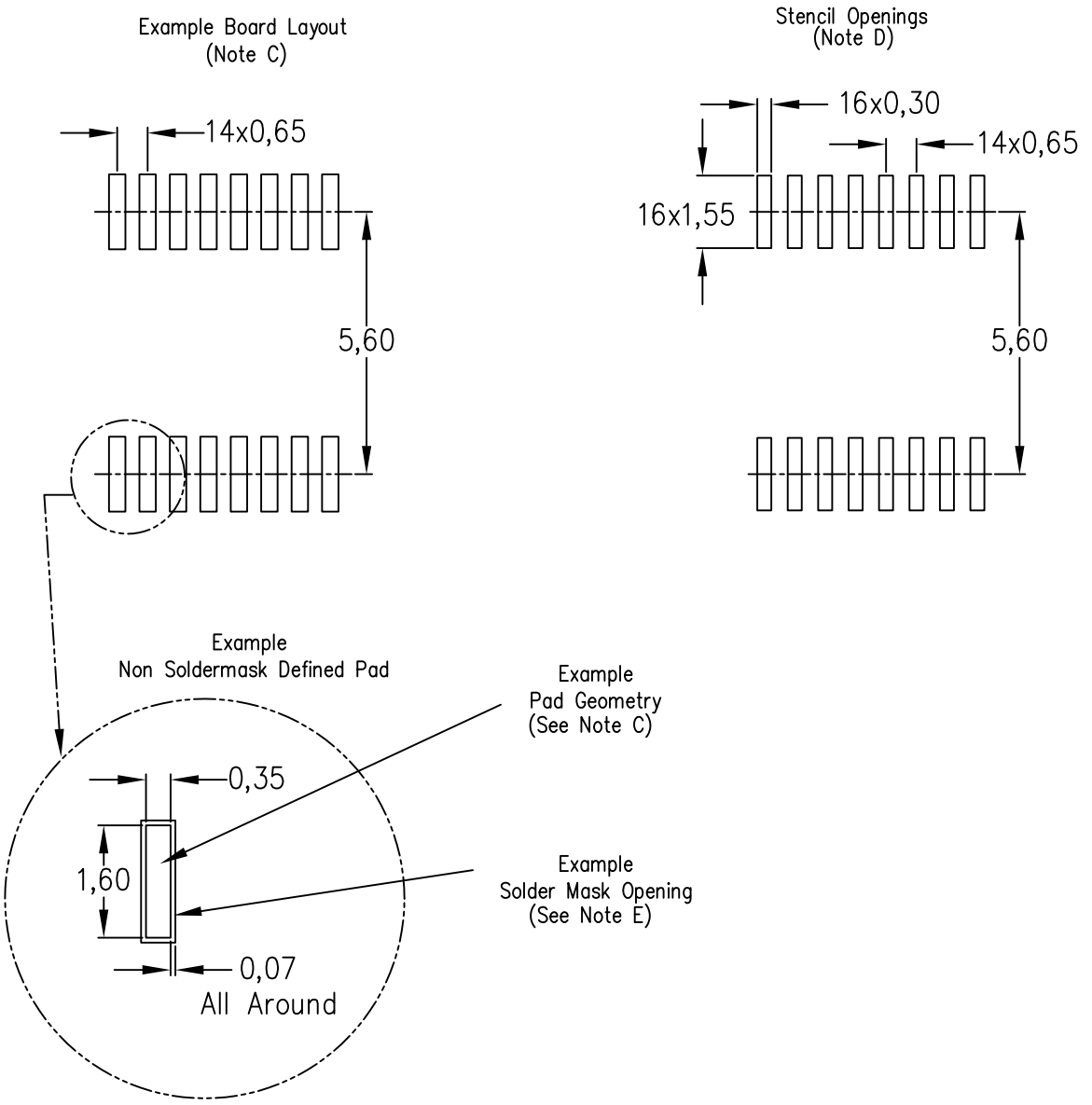
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

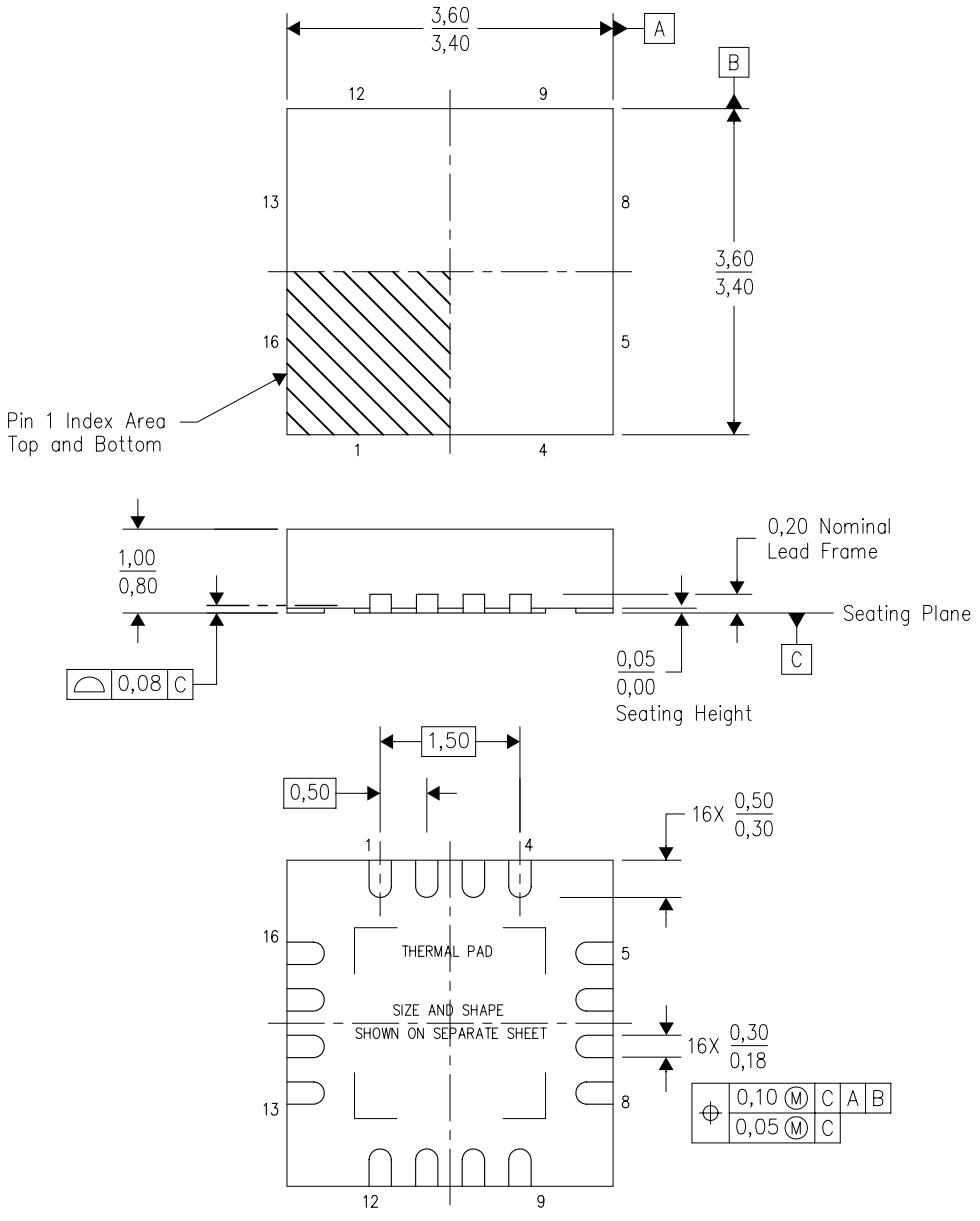
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RVA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



4209676/C 05/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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