

Current Mode PWM Controller

FEATURES

- Optimized for Off-line and DC to DC Converters
- Low Start Up Current (<0.5mA)
- Trimmed Oscillator Discharge Current
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Low Ro Error Amp

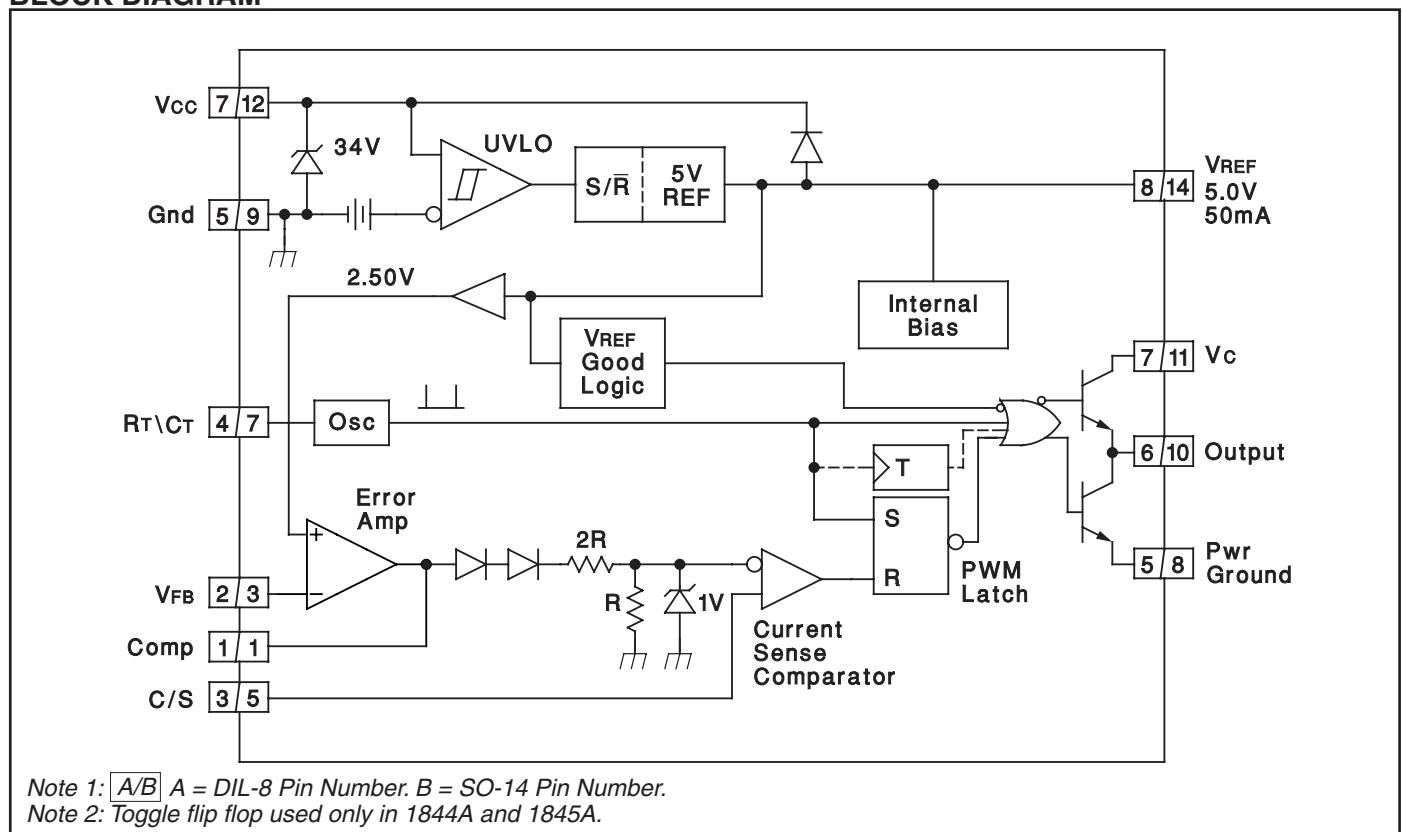
DESCRIPTION

The UC1842A/3A/4A/5A family of control ICs is a pin for pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5mA. Oscillator discharge is trimmed to 8.3mA. During under voltage lockout, the output stage can sink at least 10mA at less than 1.2V for VCC over 5V.

The difference between members of this family are shown in the table below.

Part #	UVLO On	UVLO Off	Maximum Duty Cycle
UC1842A	16.0V	10.0V	<100%
UC1843A	8.5V	7.9V	<100%
UC1844A	16.0V	10.0V	<50%
UC1845A	8.5V	7.9V	<50%

BLOCK DIAGRAM



CONNECTION DIAGRAMS

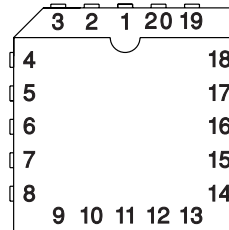
UC1842A/3A/4A/5A
UC2842A/3A/4A/5A
UC3842A/3A/4A/5A

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source)	30V
Supply Voltage (I _{CC} mA)	Self Limiting
Output Current	±1A
Output Energy (Capacitive Load)	5μJ
Analog Inputs (Pins 2, 3)	-0.3V to +6.3V
Error Amp Output Sink Current	10mA
Power Dissipation at T _A ≤ 25°C (DIL-8)	1W
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

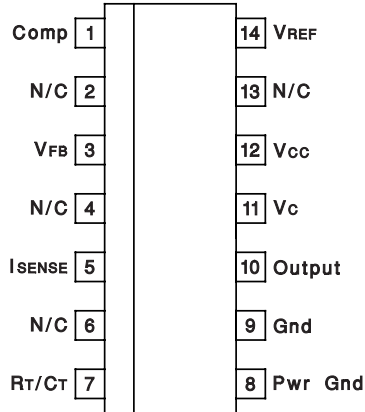
Note 1. All voltages are with respect to Ground, Pin 5. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL package only.

PLCC-20, LCC-20 (TOP VIEW) Q, L Packages

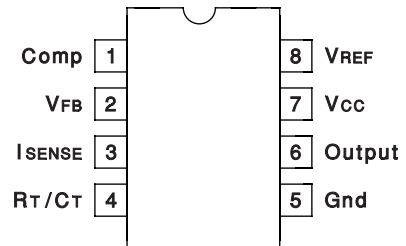


PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Comp	2
N/C	3-4
VFB	5
N/C	6
I _{SENSE}	7
N/C	8-9
R _T /C _T	10
N/C	11
Pwr Gnd	12
Gnd	13
N/C	14
Output	15
N/C	16
V _C	17
V _{CC}	18
N/C	19
VREF	20

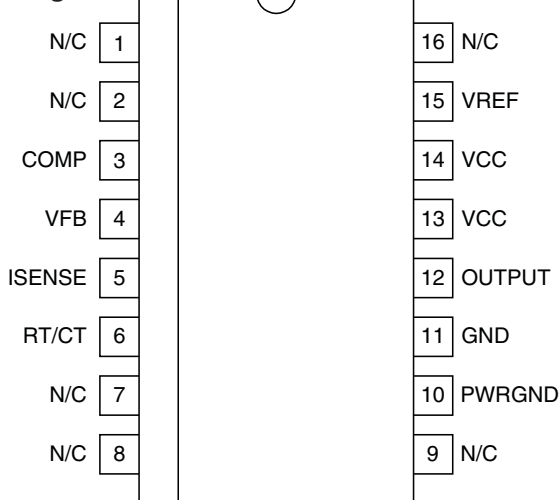
SOIC-14 (TOP VIEW) D Package



DIL-8, SOIC-8 (TOP VIEW) J or N, D8 Package



SOIC-WIDE16 (TOP VIEW) DW Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for the UC184xA; $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for the UC284xAQ; $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ for the UC284xA; $0 \leq T_A \leq 70^{\circ}\text{C}$ for the UC384xA; $V_{CC} = 15\text{V}$ (Note 5); $R_T = 10\text{k}$; $C_T = 3.3\text{nF}$; $T_A = T_J$; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA/UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	$T_J = 25^{\circ}\text{C}$, $I_O = 1\text{mA}$	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{IN} \leq 25\text{V}$		6	20		6	20	mV
Load Regulation	$1 \leq I_O \leq 20\text{mA}$		6	25		6	25	mV
Temp. Stability	(Note 2, Note 7)		0.2	0.4		0.2	0.4	mV/ $^{\circ}\text{C}$
Total Output Variation	Line, Load, Temp.	4.9		5.1	4.82		5.18	V
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}$ $T_J = 25^{\circ}\text{C}$ (Note 2)		50			50		μV
Long Term Stability	$T_A = 125^{\circ}\text{C}$, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	$T_J = 25^{\circ}\text{C}$ (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25\text{V}$		0.2	1		0.2	1	%
Temp. Stability	$T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2)		5			5		%
Amplitude	$V_{PIN 4}$ peak to peak (Note 2)		1.7			1.7		V
Discharge Current	$T_J = 25^{\circ}\text{C}$, $V_{PIN 4} = 2\text{V}$ (Note 8)	7.8	8.3	8.8	7.8	8.3	8.8	mA
	$V_{PIN 4} = 2\text{V}$ (Note 8)	7.5		8.8	7.6		8.8	mA
Error Amp Section								
Input Voltage	$V_{PIN 1} = 2.5\text{V}$	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	μA
AVOL	$2 \leq V_O \leq 4\text{V}$	65	90		65	90		dB
Unity Gain Bandwidth	$T_J = 25^{\circ}\text{C}$ (Note 2)	0.7	1		0.7	1		MHz
PSRR	$12 \leq V_{CC} \leq 25\text{V}$	60	70		60	70		dB
Output Sink Current	$V_{PIN 2} = 2.7\text{V}$, $V_{PIN 1} = 1.1\text{V}$	2	6		2	6		mA
Output Source Current	$V_{PIN 2} = 2.3\text{V}$, $V_{PIN 1} = 5\text{V}$	-0.5	-0.8		-0.5	-0.8		mA
VOUT High	$V_{PIN 2} = 2.3\text{V}$, $R_L = 15\text{k}$ to ground	5	6		5	6		V
VOUT Low	$V_{PIN 2} = 2.7\text{V}$, $R_L = 15\text{k}$ to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Note 3, Note 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN 1} = 5\text{V}$ (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	$12 \leq V_{CC} \leq 25\text{V}$ (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	μA
Delay to Output	$V_{PIN 3} = 0$ to 2V (Note 2)		150	300		150	300	ns
Output Section								
Output Low Level	$I_{SINK} = 20\text{mA}$		0.1	0.4		0.1	0.4	V
	$I_{SINK} = 200\text{mA}$		15	2.2		15	2.2	V
Output High Level	$I_{SOURCE} = 20\text{mA}$	13	13.5		13	13.5		V
	$I_{SOURCE} = 200\text{mA}$	12	13.5		12	13.5		V
Rise Time	$T_J = 25^{\circ}\text{C}$, $C_L = 1\text{nF}$ (Note 2)		50	150		50	150	ns
Fall Time	$T_J = 25^{\circ}\text{C}$, $C_L = 1\text{nF}$ (Note 2)		50	150		50	150	ns
UVLO Saturation	$V_{CC} = 5\text{V}$, $I_{SINK} = 10\text{mA}$		0.7	1.2		0.7	1.2	V

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PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Under-Voltage Lockout Section								
Start Threshold	x842A/4A	15	16	17	14.5	16	17.5	V
	x843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operation Voltage After Turn On	x842A/4A	9	10	11	8.5	10	11.5	V
	x843A/5A	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	x842A/3A	94	96	100	94	96	100	%
	x844A/5A	47	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.3	0.5		0.3	0.5	mA
Operating Supply Current	$V_{PIN2} = V_{PIN3} = 0\text{V}$		11	17		11	17	mA
Vcc Zener Voltage	$I_{CC} = 25\text{mA}$	30	34		30	34		V

Note 2: Ensured by design, but not 100% production tested.

Note 3: Parameter measured at trip point of latch with $V_{PIN2} = 0$.

Note 4: Gain defined as: $A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}}$; $0 \leq V_{PIN3} \leq 0.8\text{V}$.

Note 5: Adjust V_{CC} above the start threshold before setting at 15V.

Note 6: Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.

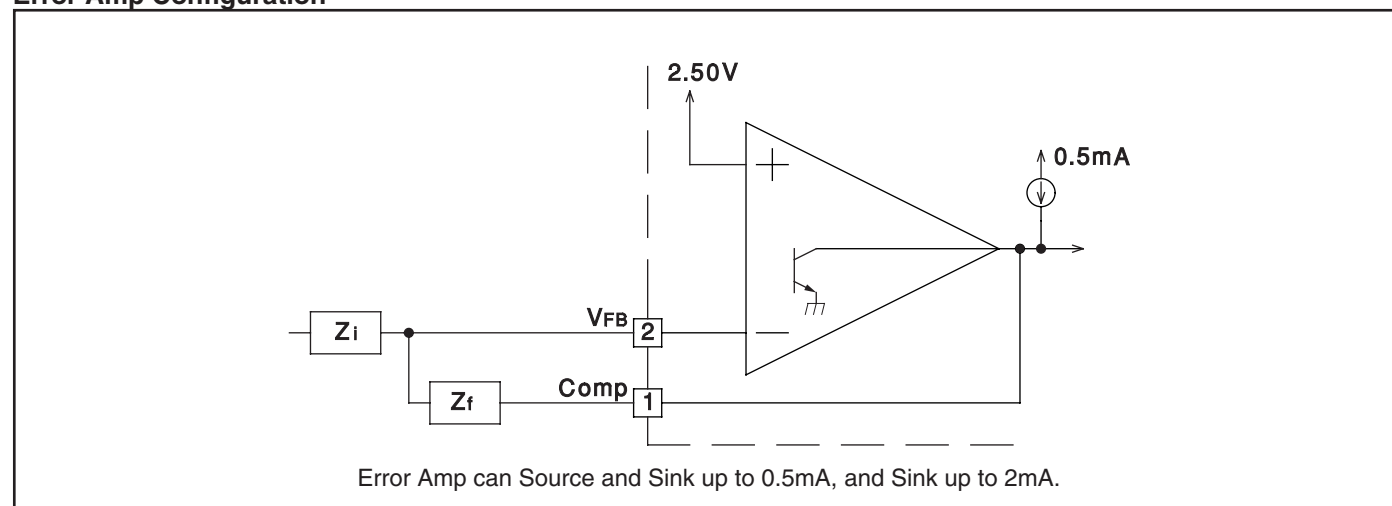
Note 7: "Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF}(\text{max}) - V_{REF}(\text{min})}{T_J(\text{max}) - T_J(\text{min})}. V_{REF}(\text{max}) \text{ and } V_{REF}(\text{min}) \text{ are the maximum \& minimum reference volt-}$$

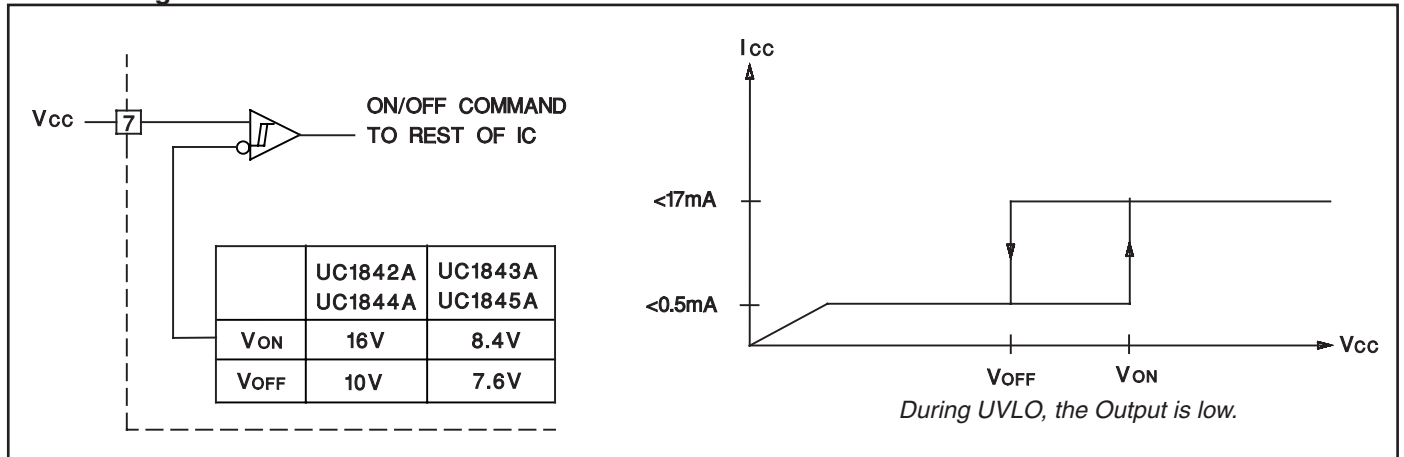
age measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature."

Note 8: This parameter is measured with $R_T = 10\text{k}\Omega$ to V_{REF} . This contributes approximately $300\mu\text{A}$ of current to the measurement. The total current flowing into the R_T/C pin will be approximately $300\mu\text{A}$ higher than the measured value.

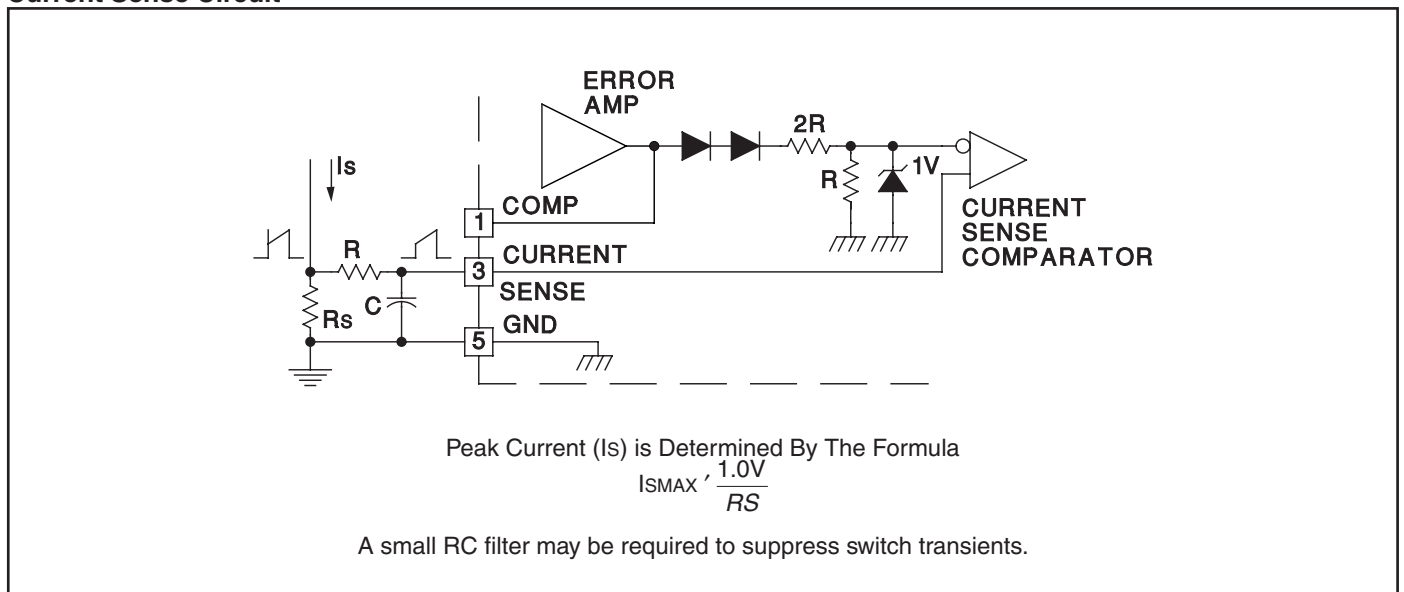
Error Amp Configuration



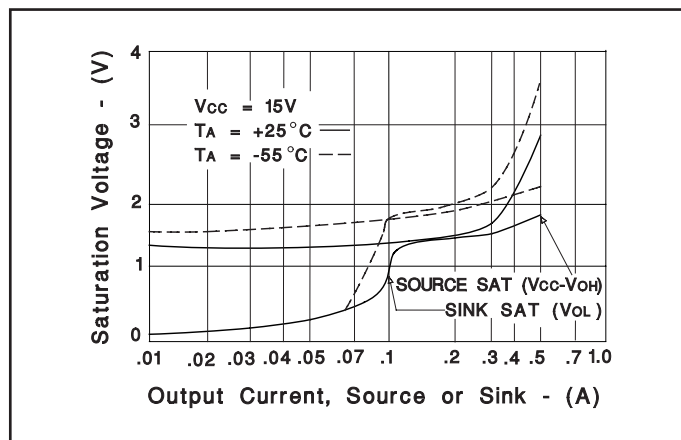
Under-Voltage Lockout



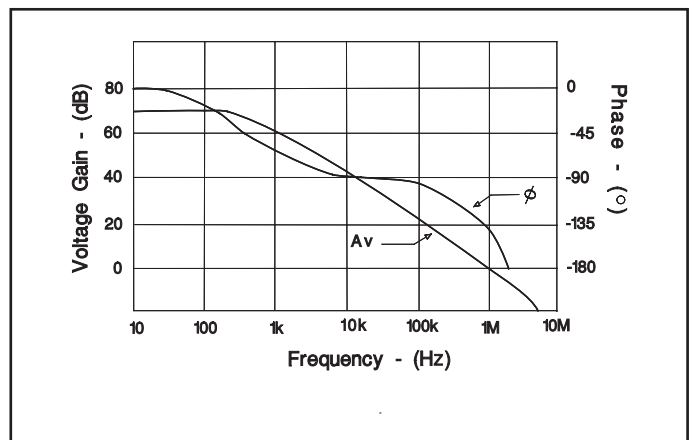
Current Sense Circuit



Output Saturation Characteristics

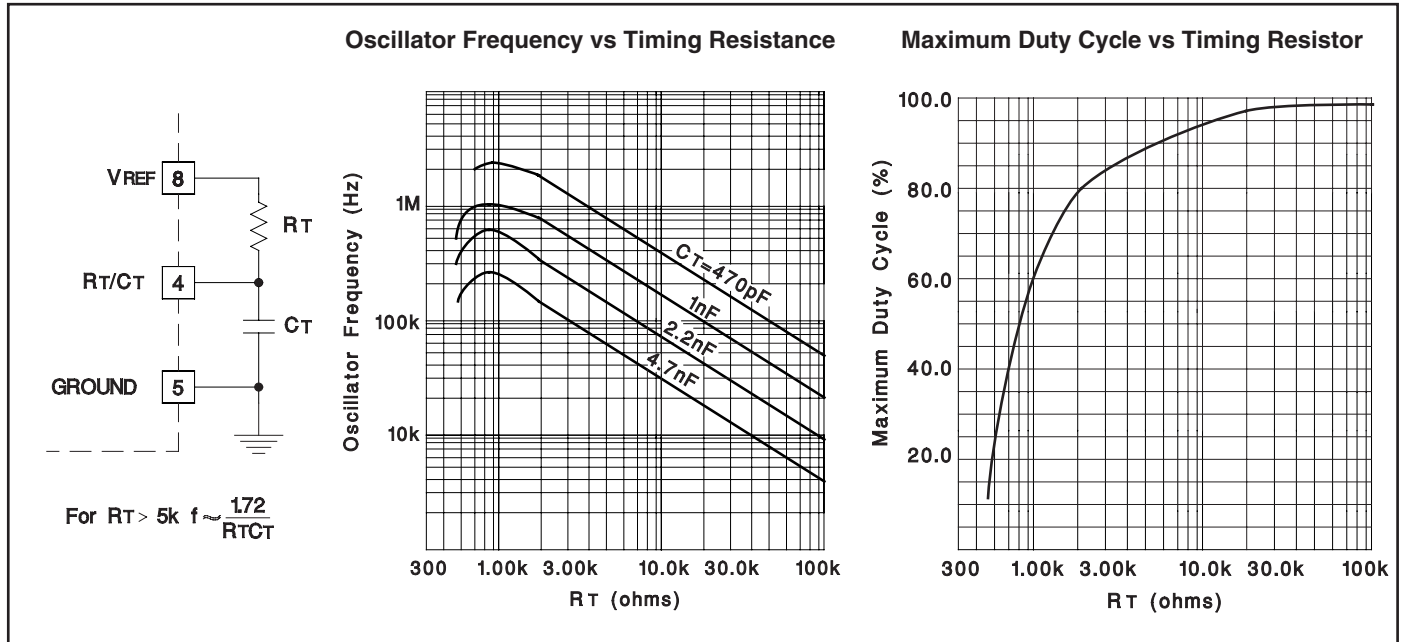


Error Amplifier Open-Loop Frequency Response

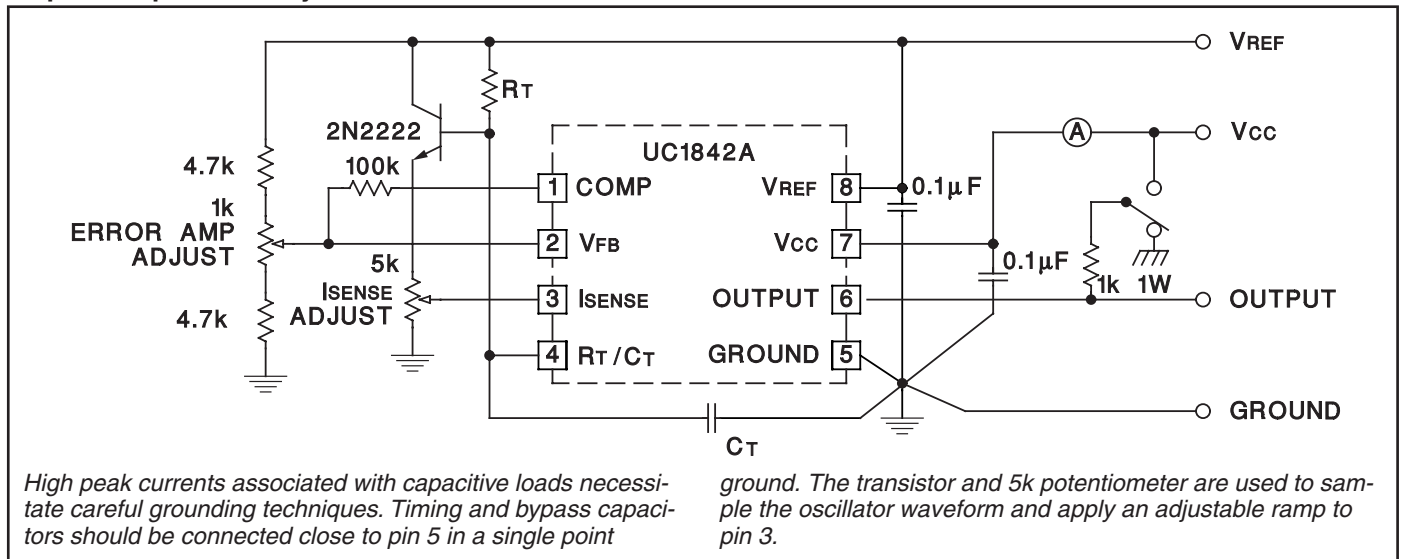


APPLICATIONS DATA (cont.)

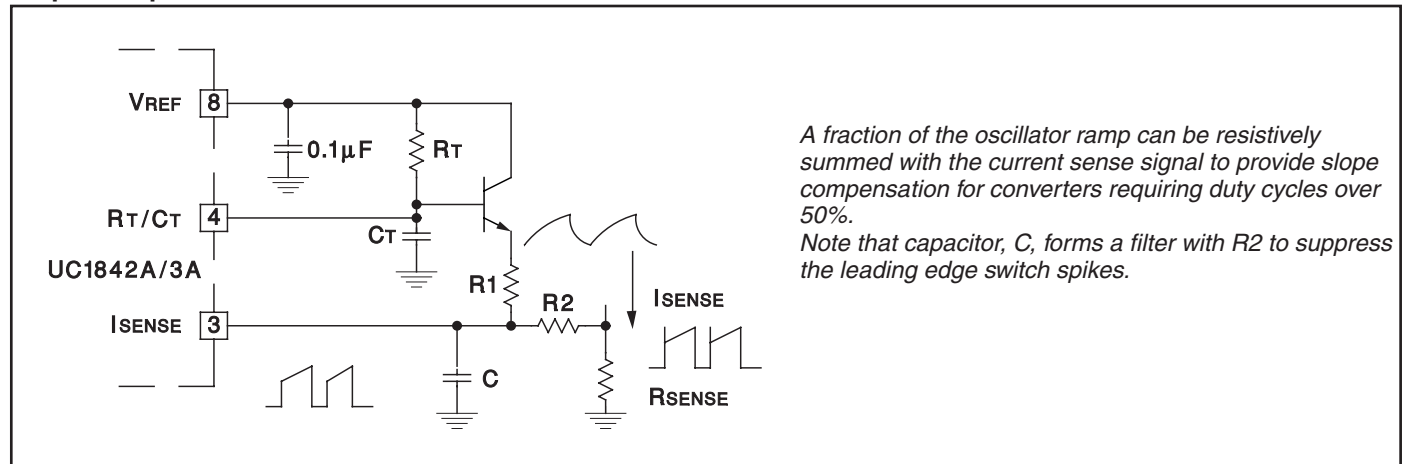
Oscillator Section



Open-Loop Laboratory Test Fixture

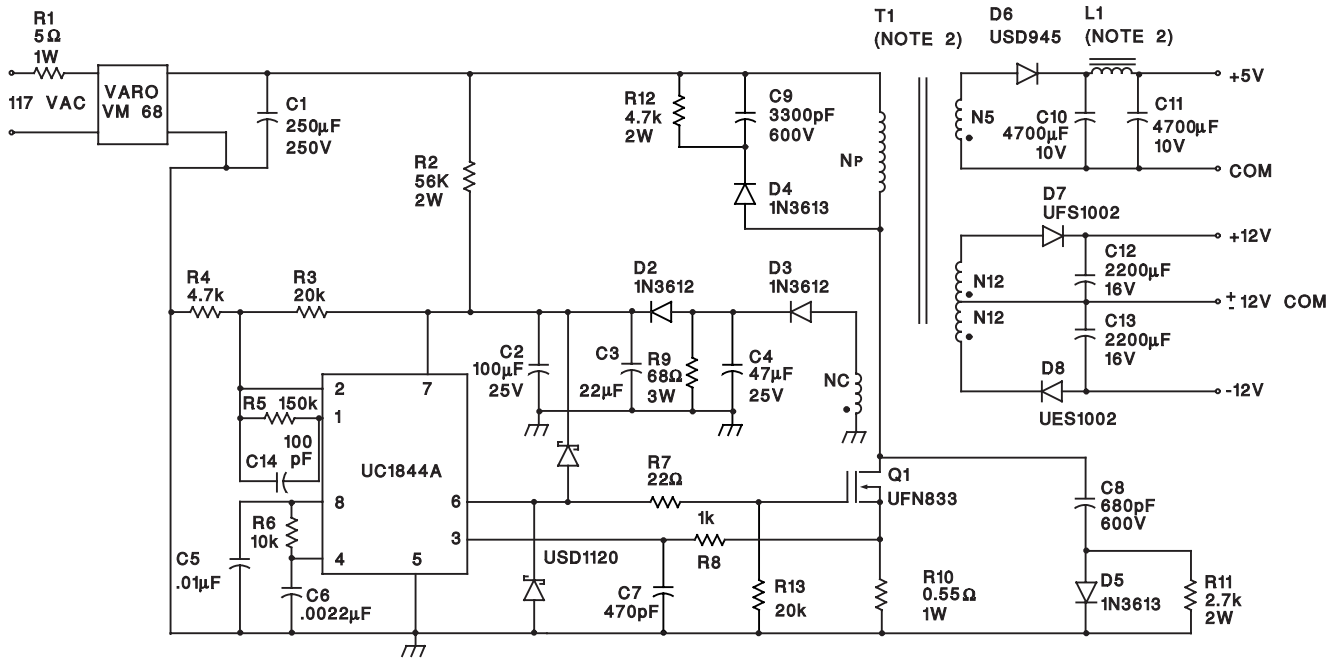


Slope Compensation



APPLICATIONS DATA (cont.)

Off-line Flyback Regulator



Power Supply Specifications

- | | |
|-------------------------|--------------------------------|
| 1. Input Voltage | 95VAC to 130VA
(50 Hz/60Hz) |
| 2. Line Isolation | 3750V |
| 3. Switching Frequency | 40kHz |
| 4. Efficiency Full Load | 70% |

5. Output Voltage:
- | | |
|---------------------------------|-------------------------------|
| A. +5V, ±5%; 1A to 4A load | Ripple voltage: 50mV P-P Max |
| B. +12V, ±3%; 0.1A to 0.3A load | Ripple voltage: 100mV P-P Max |
| C. -12V, ±3%; 0.1A to 0.3A load | Ripple voltage: 100mV P-P Max |

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-8670405PA	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
5962-8670405VPA	ACTIVE	CDIP	JG	8	1	None	Call TI	Level-NC-NC-NC
5962-8670405VXA	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8670405XA	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
5962-8670406PA	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
5962-8670406VPA	ACTIVE	CDIP	JG	8	1	None	Call TI	Level-NC-NC-NC
5962-8670406VXA	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8670406XA	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
5962-8670407PA	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
5962-8670407VPA	ACTIVE	CDIP	JG	8	1	None	Call TI	Level-NC-NC-NC
5962-8670407VXA	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8670407XA	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
5962-8670408PA	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
5962-8670408VPA	ACTIVE	CDIP	JG	8	1	None	Call TI	Level-NC-NC-NC
5962-8670408VXA	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8670408XA	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1842AJ	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1842AJ883B	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1842AJQMLV	ACTIVE	CDIP	JG	8		None	Call TI	Call TI
UC1842AL883B	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1842ALQMLV	ACTIVE	LCCC	FK	20		None	Call TI	Call TI
UC1843AJ	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1843AJ883B	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1843AJQMLV	ACTIVE	CDIP	JG	8		None	Call TI	Call TI
UC1843AL883B	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1843ALQMLV	ACTIVE	LCCC	FK	20		None	Call TI	Call TI
UC1844AJ	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1844AJ883B	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1844AJQMLV	ACTIVE	CDIP	JG	8		None	Call TI	Call TI
UC1844AL883B	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1844ALQMLV	ACTIVE	LCCC	FK	20		None	Call TI	Call TI
UC1845AJ	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1845AJ883B	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC1845AJQMLV	ACTIVE	CDIP	JG	8		None	Call TI	Call TI
UC1845AL883B	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
UC1845ALQMLV	ACTIVE	LCCC	FK	20		None	Call TI	Call TI
UC2842AD	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC2842AD8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC2842AD8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2842AD8TRG4	ACTIVE	SOIC	D	8	2500	None	Call TI	Call TI
UC2842ADTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2842ADW	ACTIVE	SOIC	DW	16	40	None	CU NIPDAU	Level-2-220C-1 YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UC2842ADWTR	ACTIVE	SOIC	DW	16	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
UC2842AJ	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
UC2842AN	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC2843AD	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC2843AD8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC2843AD8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2843ADTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2843ADW	ACTIVE	SOIC	DW	16	40	None	CU NIPDAU	Level-2-220C-1 YEAR
UC2843ADWTR	ACTIVE	SOIC	DW	16	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
UC2843AJ	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
UC2843AN	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC2843AQ	ACTIVE	PLCC	FN	20	46	None	CU SNPB	Level-2-220C-1 YEAR
UC2844AD	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC2844AD8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC2844AD8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2844AD8TRG4	PREVIEW	SOIC	D	8	2500	None	Call TI	Call TI
UC2844ADTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2844ADW	ACTIVE	SOIC	DW	16	40	None	CU NIPDAU	Level-2-220C-1 YEAR
UC2844ADWTR	ACTIVE	SOIC	DW	16	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
UC2844AJ	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC2844AN	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC2844AQD	ACTIVE	SOIC	D	14	50	None	Call TI	Level-1-220C-UNLIM
UC2844AQD8	ACTIVE	SOIC	D	8	75	None	Call TI	Level-1-220C-UNLIM
UC2844AQD8R	ACTIVE	SOIC	D	8	2500	None	Call TI	Level-1-220C-UNLIM
UC2844AQDR	ACTIVE	SOIC	D	14	2500	None	Call TI	Level-1-220C-UNLIM
UC2845AD	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC2845AD8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC2845AD8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2845AD8TRG4	PREVIEW	SOIC	D	8	2500	None	Call TI	Call TI
UC2845ADTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC2845ADW	ACTIVE	SOIC	DW	16	40	None	CU NIPDAU	Level-2-220C-1 YEAR
UC2845AN	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC3842AD	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC3842AD8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC3842AD8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3842ADTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3842ADW	ACTIVE	SOIC	DW	16	40	None	CU NIPDAU	Level-2-220C-1 YEAR
UC3842ADWTR	ACTIVE	SOIC	DW	16	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
UC3842AJ	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC3842AN	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UC3842ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NA-NA-NA
UC3843AD	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC3843AD8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC3843AD8G4	ACTIVE	SOIC	D	8	75	None	Call TI	Call TI
UC3843AD8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3843AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3843ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3843ADTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3843AJ	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC3843AN	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC3843ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NA-NA-NA
UC3844AD	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC3844AD8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC3844AD8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3844AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3844ADTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3844ADW	ACTIVE	SOIC	DW	16	40	None	CU NIPDAU	Level-2-220C-1 YEAR
UC3844ADWTR	ACTIVE	SOIC	DW	16	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
UC3844AN	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC3845AD	ACTIVE	SOIC	D	14	50	None	CU NIPDAU	Level-1-220C-UNLIM
UC3845AD8	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
UC3845AD8TR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3845ADTR	ACTIVE	SOIC	D	14	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3845ADW	ACTIVE	SOIC	DW	16	40	None	CU NIPDAU	Level-2-220C-1 YEAR
UC3845ADWTR	ACTIVE	SOIC	DW	16	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
UC3845AJ	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
UC3845AN	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SNPB	Level-NC-NC-NC
UC3845ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NA-NA-NA

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements

for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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