

8-PIN CURRENT MODE PUSH-PULL PWM CONTROLLERS WITH PROGRAMMABLE SLOPE COMPENSATION

FEATURES

- Programmable Slope Compensation
- Internal Soft-Start on the UCC38083/4
- Cycle-by-Cycle Current Limiting
- Low Start-Up Current of 120 μ A and 1.5 mA Typical Run Current
- Single External Component Oscillator Programmable from 50 kHz to 1 MHz
- High-Current Totem-Pole Dual Output Stage Drives Push-Pull Configuration with 1-A Sink and 0.5-A Source Capability
- Current Sense Discharge Transistor to Improve Dynamic Response
- Internally Trimmed Bandgap Reference
- Undervoltage Lockout with Hysteresis

APPLICATIONS

- **High-Efficiency Switch-Mode Power Supplies**
- **Telecom dc-to-dc Converters**
- **Point-of-Load or Point-of-Use Power Modules**
- **Low-Cost Push-Pull and Half-Bridge Applications**

DESCRIPTION

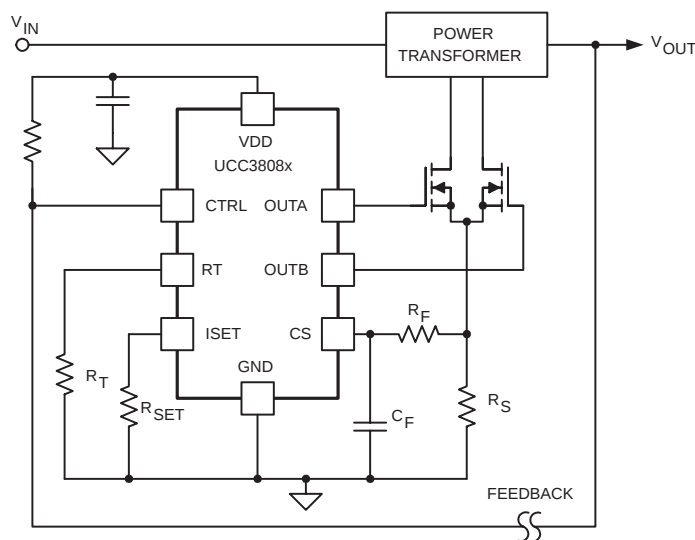
The UCC38083/4/5/6 is a family of BiCMOS pulse width modulation (PWM) controllers for dc-to-dc or off-line fixed-frequency current-mode switching power supplies. The dual output stages are configured for the push-pull topology. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 110 ns, limiting each output's duty cycle to less than 50%.

The new UCC3808x family is based on the UCC3808A architecture. The major differences include the addition of a programmable slope compensation ramp to the CS signal and the removal of the error amplifier. The current flowing out of the ISET pin through an external resistor is monitored internally to set the magnitude of the slope compensation function. This device also includes an internal discharge transistor from the CS pin to ground, which is activated at each clock cycle after the pulse is terminated. This discharges any filter capacitance on the CS pin during each cycle and helps minimize filter capacitor values and current sense delay.

The UCC38083 and the UCC38084 devices have a typical soft-start interval time of 3.5 ms while the UCC38085 and the UCC38086 has less than 100 μ s for applications where internal soft-start is not desired.

The UCC38083 and the UCC38085 devices have the turn-on/off thresholds of 12.5 V / 8.3 V, while the UCC38084 and the UCC38086 has the turn-on/off thresholds of 4.3 V / 4.1 V. Each device is offered in 8-pin TSSOP (PW), 8-pin SOIC (D) and 8-pin PDIP (P) packages.

BASIC APPLICATION



UDG-01080



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

UCC28083, UCC28084, UCC28085, UCC28086 UCC38083, UCC38084, UCC38085, UCC38086

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ORDERING INFORMATION

THERMAL RESISTANCE TABLE

PACKAGE	$\theta_{jc}(^{\circ}\text{C/W})$	$\theta_{ja}(^{\circ}\text{C/W})$
SOIC-8 (D)	42	84 to 160 ⁽¹⁾
PDIP-8 (P)	50	110 ⁽¹⁾
TSSOP-8 (PW)	32 ⁽²⁾	232 to 257 ⁽²⁾

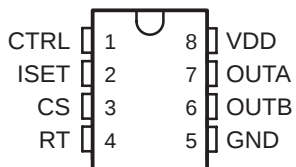
- NOTES: (1) Specified θ_{ja} (junction to ambient) is for devices mounted to 5-inch² FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 inch² aluminum PC board. Test PWB was 0.062 inch thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with a 100-mil x 100-mil probe land area at the end of each trace.
- (2). Modeled data. If value range given for θ_{ja} , lower value is for 3x3 inch. 1 oz internal copper ground plane, higher value is for 1x1-inch. ground plane. All model data assumes only one trace for each non-fused lead.

AVAILABLE OPTIONS

T _A	INTERNAL SOFT START	UVLO		PACKAGES		
		ON	OFF	SOIC-8 (D)	PDIP-8 (P)	TSSOP-8 (PW)
-40°C to 85°C	3.5 ms	12.5 V	8.3 V	UCC28083D	UCC28083P	UCC28083PW
		4.3 V	4.1 V	UCC28084D	UCC28084P	UCC28084PW
	75 μ s	12.5 V	8.3 V	UCC28085D	UCC28085P	UCC28085PW
		4.3 V	4.1 V	UCC28086D	UCC28086P	UCC28086PW
0°C to 70°C	3.5 ms	12.5 V	8.3 V	UCC38083D	UCC38083P	UCC38083PW
		4.3 V	4.1 V	UCC38084D	UCC38084P	UCC38084PW
	75 μ s	12.5 V	8.3 V	UCC38085D	UCC38085P	UCC38085PW
		4.3 V	4.1 V	UCC38086D	UCC38086P	UCC38086PW

† The D and PW packages are available taped and reeled. Add R suffix to device type, e.g. UCC28083DR (2500 devices per reel) or UCC38083PWR (2000 devices per reel).

**D OR P PACKAGE
(TOP VIEW)**



**PW PACKAGE
(TOP VIEW)**



absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{DD} ($I_{DD} < 10$ mA)	15 V
Supply current, I_{DD}	20 mA
Sink current (peak): OUTA	1.0 A
OUTB	1.0 A
Source current (peak): OUTA	-0.5 A
OUTB	-0.5 A
Analog inputs: CTRL	-0.3 V to $V_{DD} + 0.3$ V
CS	-0.3 V to $V_{DD} + 0.3$ V, not to exceed 6 V
R_{SET} (minimum)	>5 k Ω
R_T ($-100 \mu A < I_{RT} < 100 \mu A$)	-0.3 V to 2.0 V
Power dissipation at $T_A = 25^\circ C$ (P package)	1 W
Power dissipation at $T_A = 25^\circ C$ (D package)	650 mW
Power dissipation at $T_A = 25^\circ C$ (PW package)	400 mW
Junction operating temperature, T_J	-55°C to 150°C
Storage temperature, T_{stg}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, and negative out of the specified terminal.

electrical characteristics over recommended operating virtual junction temperature range, $V_{DD} = 10$ V (See Note 1), 1- μF capacitor from VDD to GND, $R_T = 165$ k Ω , $R_F = 1$ k Ω , $C_F = 220$ pF, $R_{SET} = 50$ k Ω , $T_A = -40^\circ C$ to $85^\circ C$ for UCC2808x, $T_A = 0^\circ C$ to $70^\circ C$ for UCC3808x, $T_A = T_J$ (unless otherwise noted)

overall

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Start-up current	$V_{DD} < UVLO$ start threshold voltage		120	200	μA
Supply current	CTRL = 0 V, See Note 1 CS = 0 V,		1.5	2.5	mA

undervoltage lockout

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Start threshold voltage	UCC38083/5	See Note 1	11.5	12.5	13.5	V
	UCC38084/6		4.1	4.3	4.5	
Minimum operating voltage after start	UCC38083/5		7.6	8.3	9.0	
	UCC38084/6		3.9	4.1	4.3	
Hysteresis voltage	UCC38083/5		3.5	4.2	5.1	
	UCC38084/6		0.1	0.2	0.3	

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency	$2 \times f(OUTA)$	180	200	220	kHz
Voltage amplitude	See Note 2	1.4	1.5	1.6	V
Oscillator fall time (dead time)			110	220	ns
R_T pin voltage		1.2	1.5	1.6	V

UCC28083, UCC28084, UCC28085, UCC28086 UCC38083, UCC38084, UCC38085, UCC38086

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current sense

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain	See Note 3	1.9	2.2	2.5	V/V
Maximum input signal voltage	CTRL = 5 V, See Note 4	0.47	0.52	0.57	V
CS to output delay time	CTRL = 3.5 V, $0\text{ mV} \leq CS \leq 600\text{ mV}$		100	200	ns
Source current		-200			nA
Sink current	CS = 0.5 V, RT = 2.0 V, See Note 5	3	7	12	mA
Overcurrent threshold voltage		0.70	0.75	0.80	V
CTRL to CS offset voltage	CS = 0 V, 25°C	0.55	0.70	0.90	V
	CS = 0 V	0.37	0.70	1.10	V

pulse width modulation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum duty cycle	Measured at OUTA or OUTB, See Note 7	48%	49%	50%	
Minimum duty cycle	CTRL = 0 V			0%	

output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Low-level output voltage (OUTA or OUTB)	$I_{OUT} = 100\text{ mA}$		0.5	1.0	V
High-level output voltage (OUTA or OUTB)	$I_{OUT} = -50\text{ mA}$, $(V_{DD} - V_{OUT})$, See Note 6		0.5	1.0	
Rise time	$C_{LOAD} = 1\text{ nF}$		25	60	ns
Fall time	$C_{LOAD} = 1\text{ nF}$		25	60	

soft-start

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTA/OUTB soft-start interval time, UCC38083/4	CTRL = 1.8 V, CS = 0 V, Duty cycle from 0 to full, See Note 8	1.3	3.5	8.5	ms
OUTA/OUTB soft-start interval time, UCC38085/6	CTRL = 1.8 V, CS = 0 V, Duty cycle from 0 to full, See Note 8	30	75	110	μs

slope compensation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{RAMP, peak}$	$I_{SET, peak} = 30\text{ }\mu\text{A}$, Full duty cycle	125	150	175	μA

NOTE 1: For UCCx8083/5, set VDD above the start threshold before setting to 10 V.

NOTE 2: Measured at ISET pin.

NOTE 3: Gain is defined by $A = \frac{\Delta V_{CTRL}}{\Delta V_{CS}}$, $0 \leq V_{CS} \leq 0.4\text{ V}$.

NOTE 4: Measured at trip point of latch with CS ramped from 0.4 V to 0.6 V.

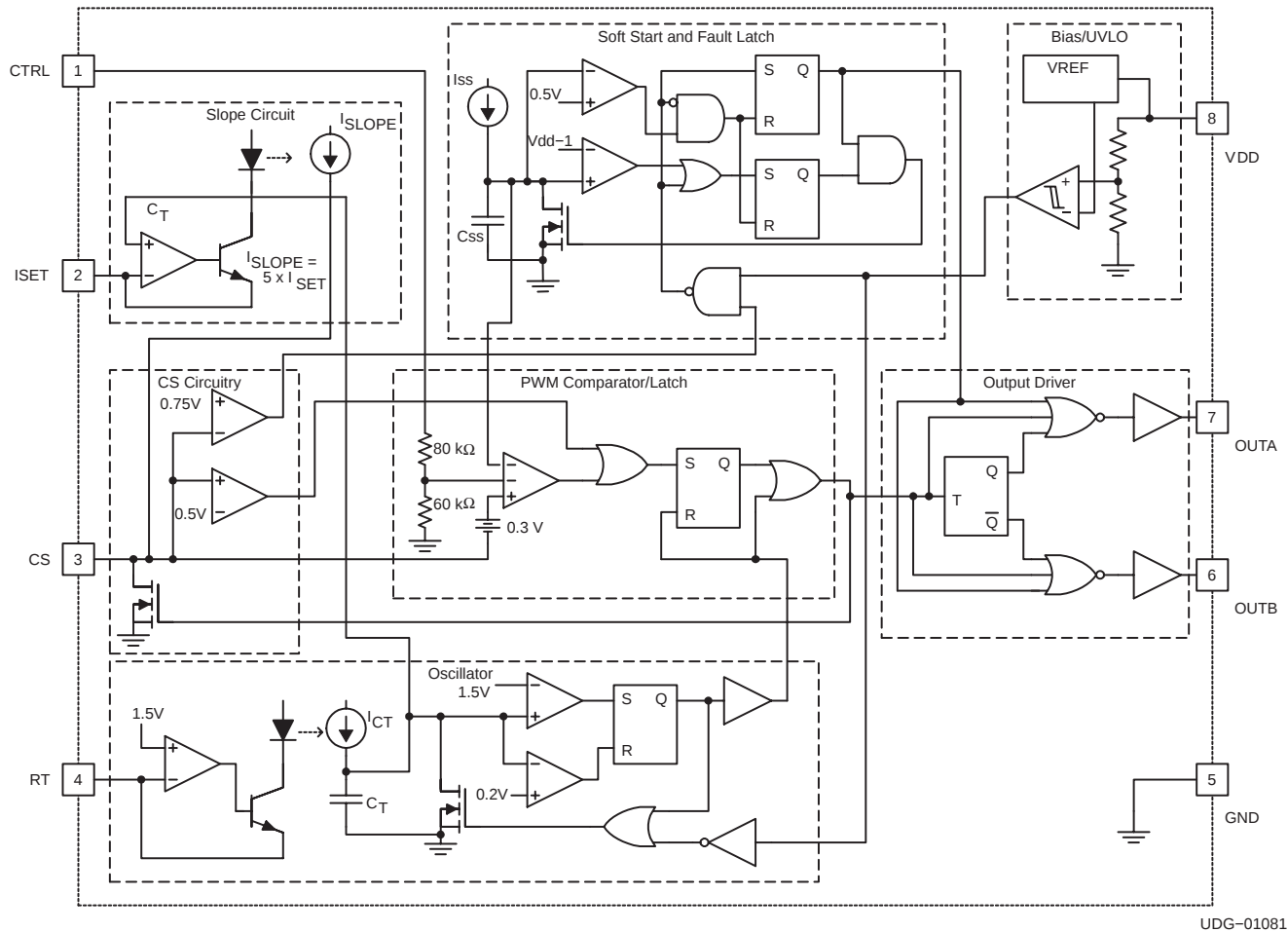
NOTE 5: This internal current sink on the CS pin is designed to discharge and external filter capacitor. It is not intended to be a dc sink path.

NOTE 6: Not 100% production tested. Ensured by design and also by the rise time test.

NOTE 7: For devices in PW package, parameter tested at wafer probe.

NOTE 8: Ensured by design.

functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	PACKAGE D OR P		
CS	3	I	The current-sense input to the PWM comparator, the cycle-by-cycle peak current comparator, and the overcurrent comparator. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft-start cycle. An internal MOSFET discharges the current-sense filter capacitor to improve dynamic performance of the power converter.
CTRL	1	I	Error voltage input to PWM comparator.
GND	5	–	Reference ground and power ground for all functions. Due to high currents, and high-frequency operation of the IC, a low-impedance circuit board ground plane is highly recommended.
ISET	2	I	Current selection for slope compensation.
OUTA	7	O	Alternating high-current output stages.
OUTB	6	O	
RT	4	I	Programs the oscillator.
VDD	8	I	Power input connection.

detailed pin descriptions

CTRL: The error voltage is typically generated by a secondary-side error amplifier and transmitted to the primary-side referenced UCC3808x by means of an opto-coupler. CTRL has an internal divider ratio of 0.45 to maintain a usable range with the minimum V_{DD} of 4.1 V. The UCC38083/UCC38084 family features a built-in full-cycle soft start while the UCC38085/6 does not.

For the UCC38083/4, soft-start is implemented as a clamp at the input to the PWM comparator. This causes the output pulses to start near 0% duty cycle and increase until the clamp exceeds the CTRL voltage.

ISET: Program the slope compensation current ramp by connecting a resistor, RSET, from ISET to ground. The voltage of the ISET pin tracks the 1.5-V internal oscillator ramp, as shown in Figure 1.

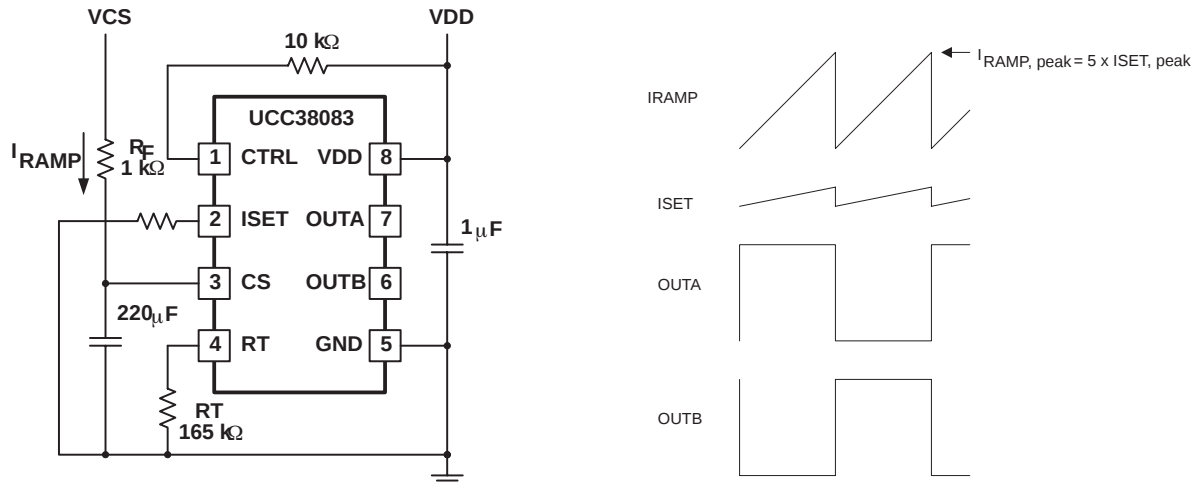


Figure 1. Full Duty Cycle Output

The compensating current source, I_{SLOPE} , at the CS pin is proportional to the ISET current, according to the relation:

$$I_{SLOPE} = 5 \times I_{SET} \quad (1)$$

The ramping current due to I_{SLOPE} develops a voltage across the effective filter impedance that is normally connected from the current sense resistor to the CS input. In order to program a desired compensating slope with a specific peak compensating ramp voltage at the CS pin, use the RSET value in the following equation:

$$RSET = V_{OSC(peak)} \times \left(\frac{5 \times R_F}{\text{RAMP VOLTAGE HEIGHT}} \right) \quad (2)$$

$$\text{Where } V_{OSC(peak)} = 1.5 \text{ V}$$

Notice that the PWM Latch drives an internal MOSFET that will discharge an external filtering capacitor on the CS pin. Thus, I_{SLOPE} will appear to terminate when the PWM comparator or the cycle-by-cycle current limit comparator sets the PWM latch. The actual compensating slope is not affected by premature termination of the switching cycle.

detailed pin descriptions (continued)

OUTA and OUTB: Alternating high-current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak-source current, and 1-A peak-sink current.

The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the internal oscillator capacitor is rising, one of the two outputs is high, but during fall time, both outputs are off. This dead time between the two outputs, along with a slower output rise time than fall time, ensures that the two outputs cannot be on at the same time. This dead time is typically 110 ns.

The high-current output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external Schottky clamp diodes are not required.

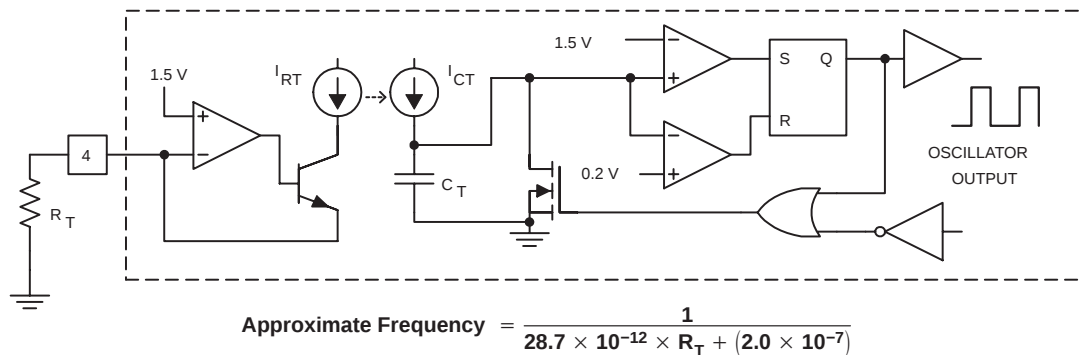
RT: The oscillator programming pin. The oscillator features an internal timing capacitor. An external resistor, R_T , sets a current from the RT pin to ground. Due to variations in the internal C_T , nominal V_{RT} of 1.5 V can vary from 1.2 V to 1.6 V

Selecting RT as shown programs the oscillator frequency:

$$RT = \frac{1}{28.7 \times 10^{-12}} \left(\frac{1}{f_{OSC}} - 2.0 \times 10^{-7} \right) \quad (3)$$

where f_{OSC} is in Hz, resistance in Ω . The recommended range of timing resistors is between 25 k Ω and 698 k Ω .

For best performance, keep the timing resistor lead from the RT pin to GND (pin 5) as short as possible.



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Figure 2. Block Diagram for Oscillator

VDD: The power input connection for this device. Although quiescent VDD current is very low, total supply current may be higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_G), average OUT current can be calculated from:

$$I_{OUT} = Q_G \times f_{OSC} \quad (4)$$

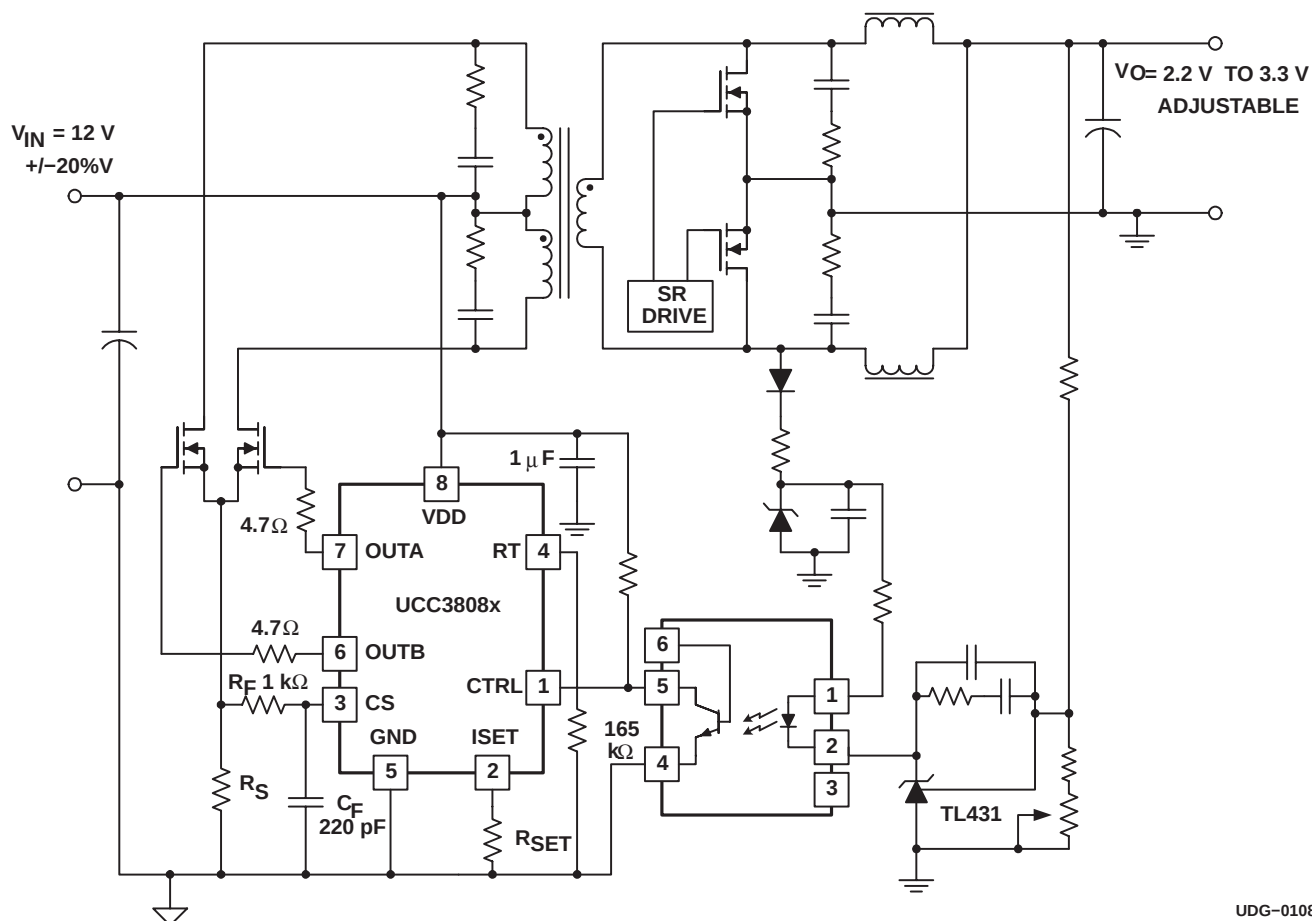
where f is the oscillator frequency.

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. A 1- μ F decoupling capacitor is recommended.

APPLICATION INFORMATION

The following application circuit shows an isolated 12-V_{IN} to 2.5 V_{OUT} push-pull converter with scalable output power (20 W to 200 W). Note that the pinout shown is for SOIC-8 and PDIP-8 packages.

typical application

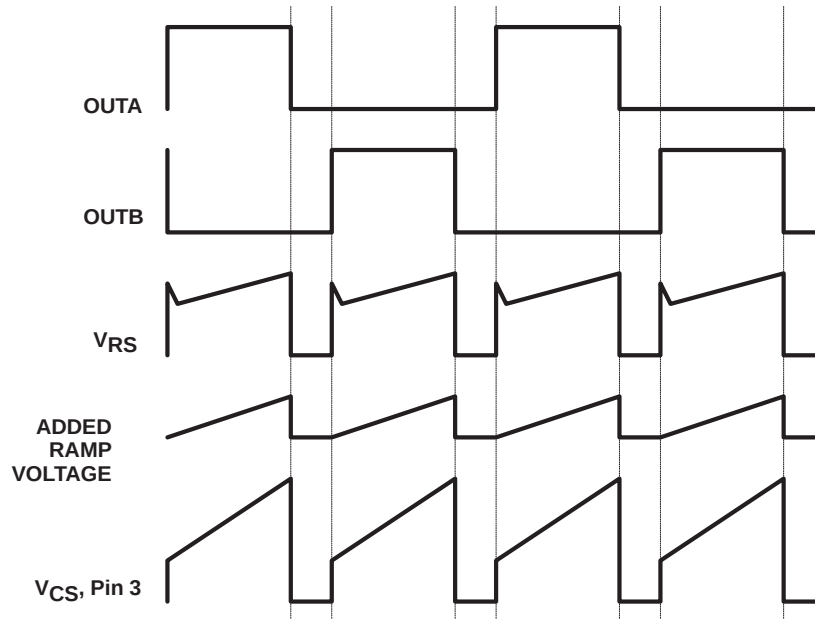


UDG-01084

APPLICATION INFORMATION

operational waveforms

Figure 3 illustrates how the voltage ramp is effectively added to the voltage across the current sense element V_{CS} , to implement slope compensation.



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Figure 3. Typical Slope Compensation Waveforms at 80% Duty Cycle

In Figure 3, OUTA and OUTB are shown at a duty cycle of 80%, with the associated voltage V_{RS} across the current sense resistor of the primary push-pull power MOSFETs. The current flowing out of CS generates the ramp voltage across the filter resistor R_F that is positioned between the power current sense resistor and the CS pin. This voltage is effectively added to V_{RS} to provide slope compensation at V_{CS} , pin 3. A capacitor C_F is also recommended to filter the waveform at CS.

layout considerations

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. A 1- μ F decoupling capacitor is recommended.

Use a local ground plane near the small signal pins (CTRL, ISET, CS and RT) of the IC for shielding. Connect the local ground plane to the GND pin with a single trace. Do not extend the local ground plane under the power pins (VDD, OUTA, OUTB and GND). Instead, use signal return traces to the GND pin for ground returns on the side of the integrated circuit with the power pins.

For best performance, keep the timing resistor lead from RT pin (pin 4) to GND (pin 5) as short as possible.

special layout considerations for the TSSOP package

Due to the different pinout and smaller lead pitch of the TSSOP package, special attention must be paid to minimize noise problems. The pinout is different because the device had to be rotated 90° to fit into the smaller TSSOP package.

For example, the two output pins are now on opposite sides of the package. The traces should not run under the package together as they will couple switching noise into analog pins.

Another common problem is when RT and OUTB (pins 6 and 8) are routed together for some distance even though they are not immediate side by side pins. Because of this, when OUTB rises, a voltage spike of upto 400 mV can couple into the RT. This spike causes the internal charge current into CT to be turned off momentarily resulting in lower duty cycle. It is also important that note that the RT pin voltage cannot be stabilized with a capacitor. The RT pin is just a dc voltage to program the internal CT. Instead, keep the OUTB and RT runs short and far from each other and follow the printed wiring board layout suggestions above to fix the problem.

reference design

A reference design is discussed in *50-W Push-Pull Converter Reference Design Using the UCC38083*, TI Literature Number SLUU135. This design controls a push-pull synchronous rectified topology with input range of 18 V to 35 V (24 nominal) and 3.3-V output at 15 A. The schematic is shown in Figure 5 and the board layout for the reference design is shown in Figure 4. Refer to the document for further details.

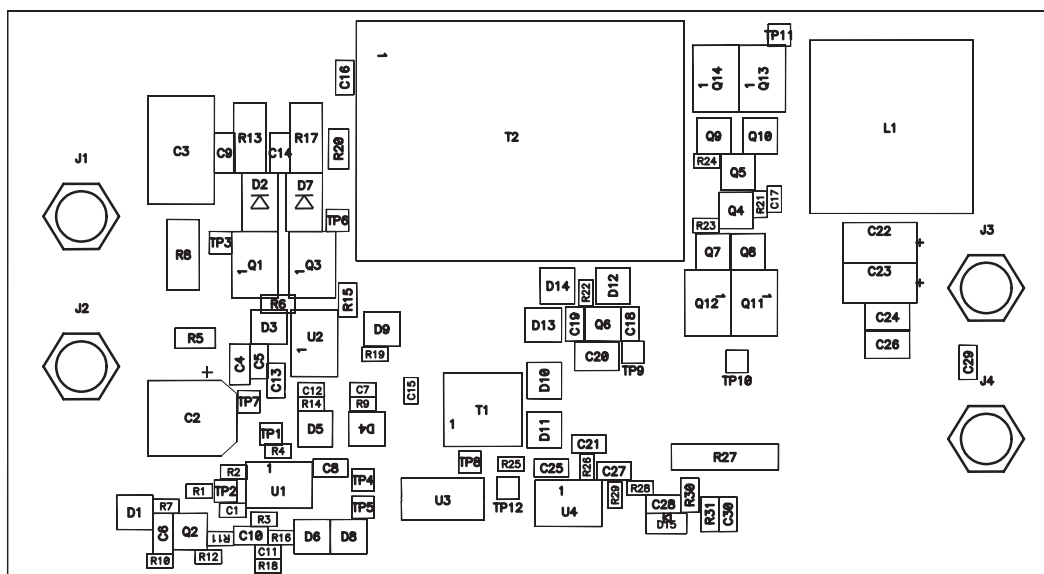


Figure 4. Reference Design Layout

APPLICATION INFORMATION

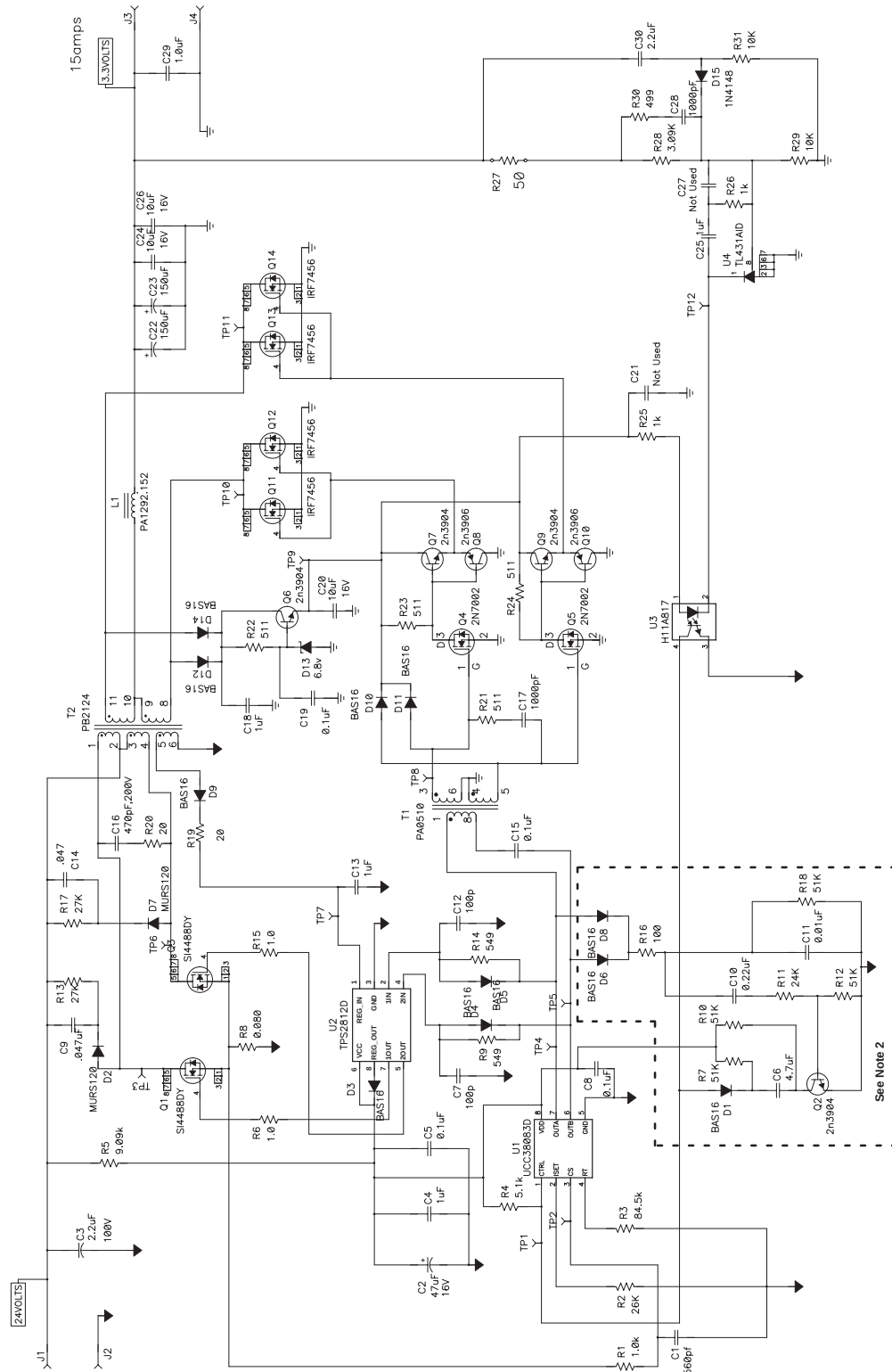


Figure 5. Reference Design Schematic

Note 1. C28, R25, and D12 accelerate the control to the secondary side feedback at start-up and prevent output voltage overshoot.
Note 2. Components used for the UCC38085 only.

TYPICAL CHARACTERISTICS

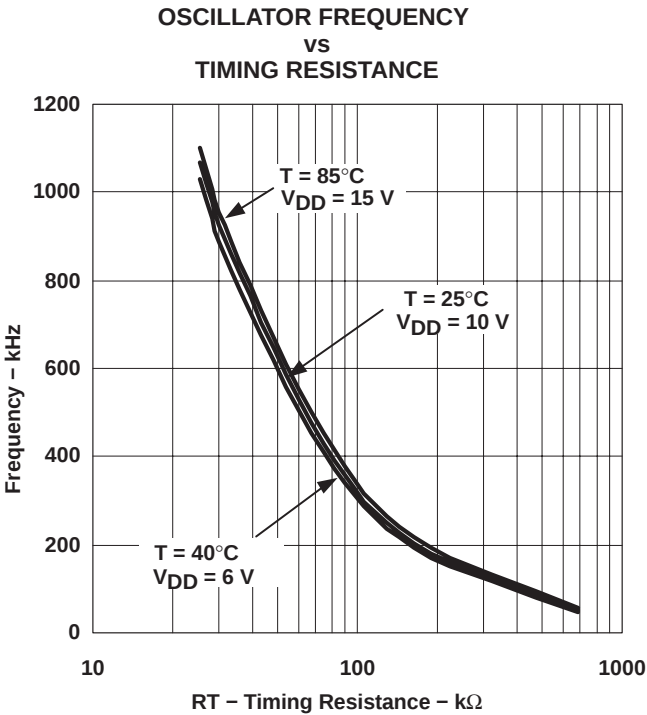


Figure 6

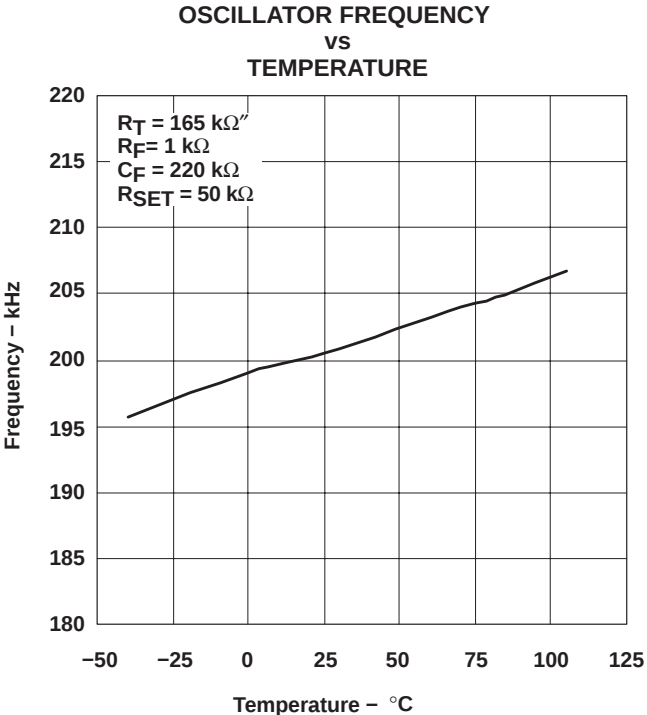


Figure 7

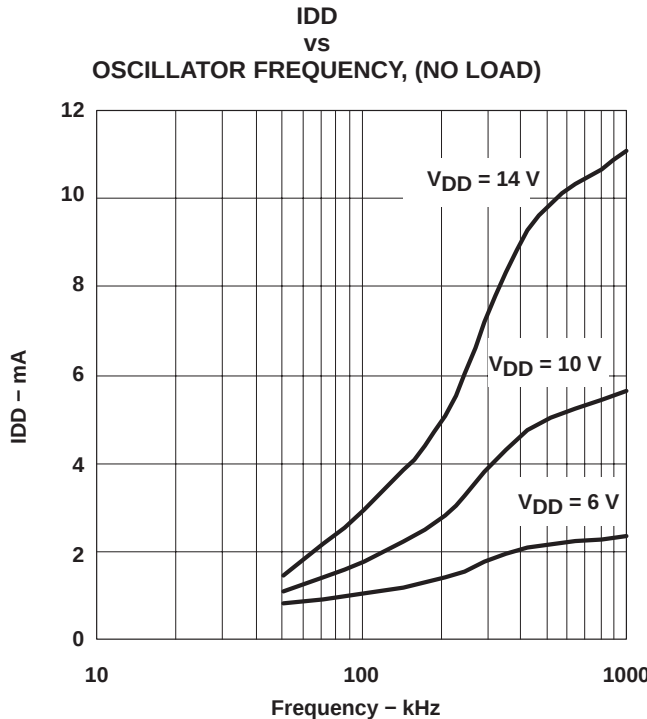


Figure 8

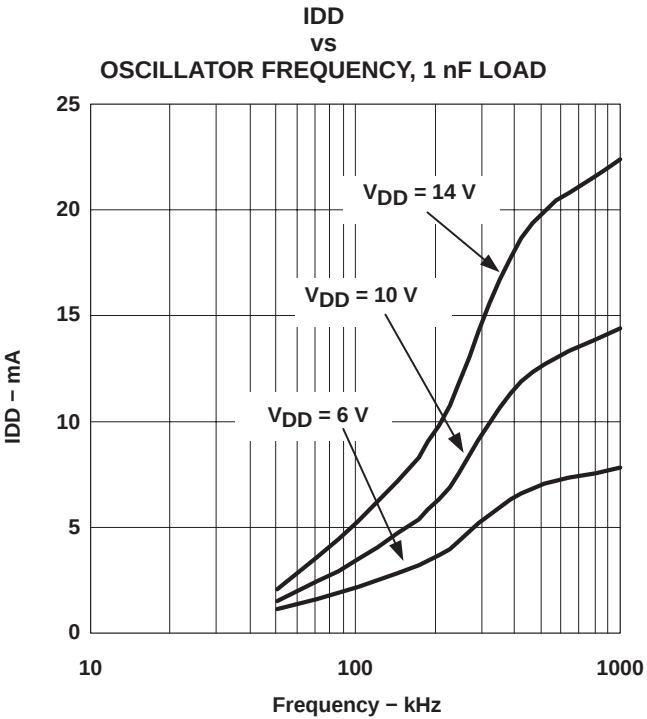


Figure 9

TYPICAL CHARACTERISTICS

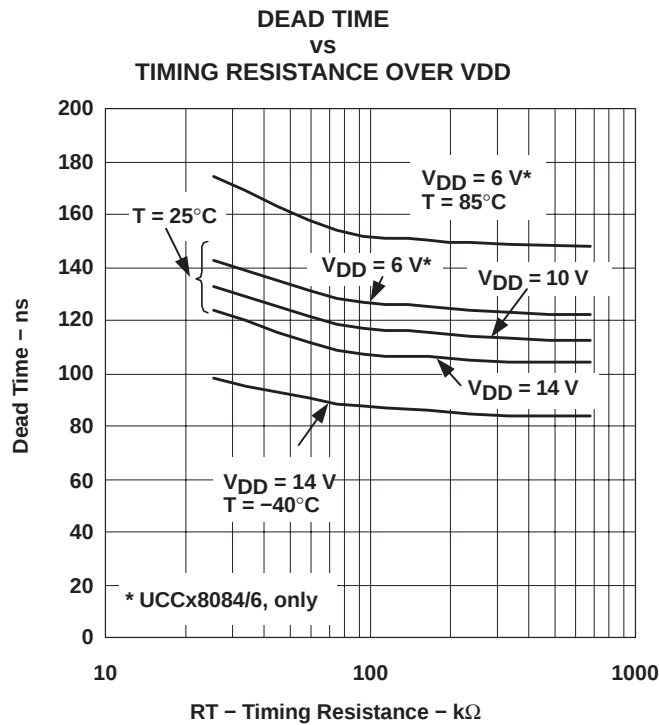


Figure 10

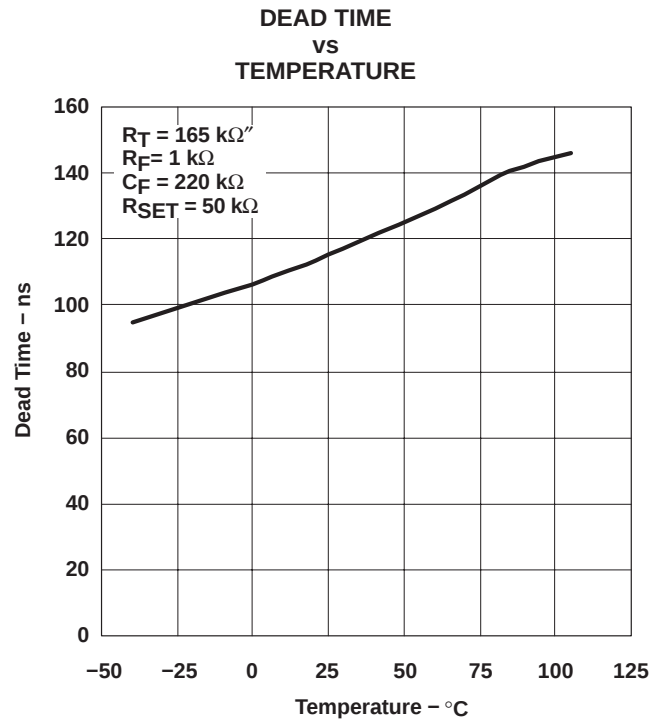


Figure 11

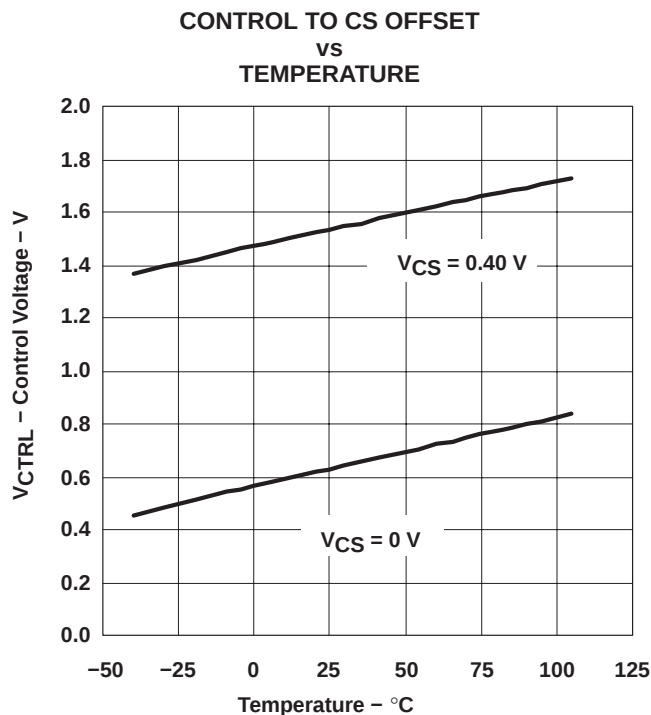


Figure 12

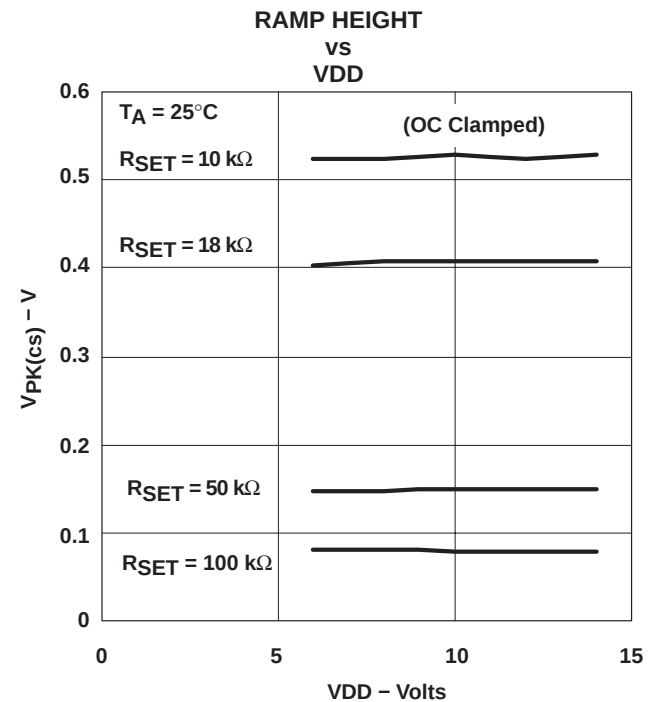


Figure 13

TYPICAL CHARACTERISTICS

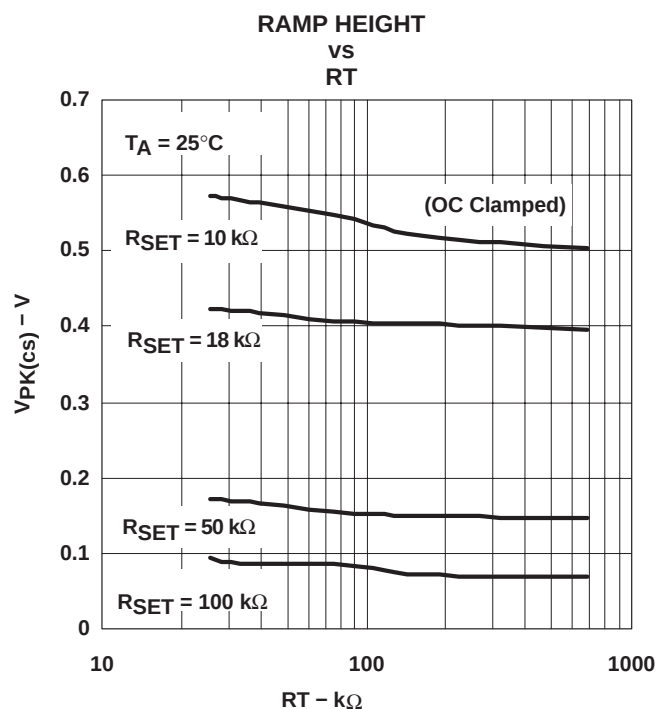


Figure 14

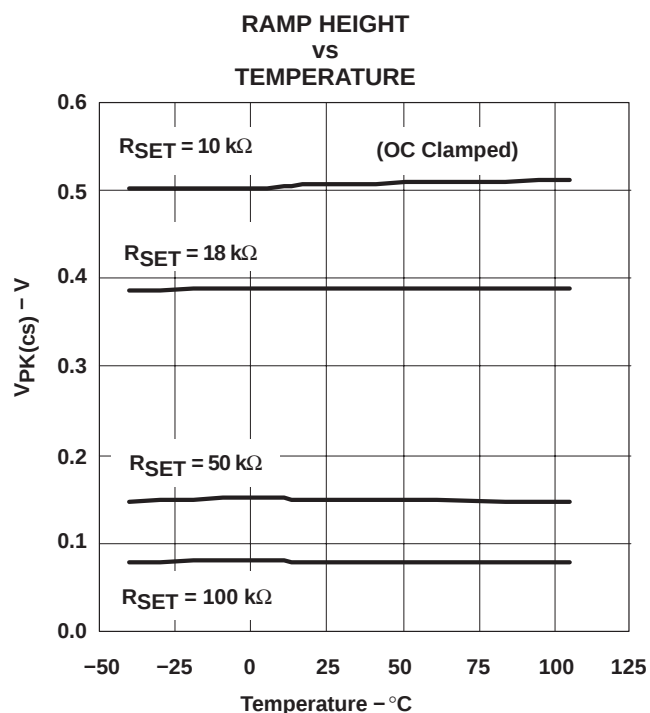


Figure 15

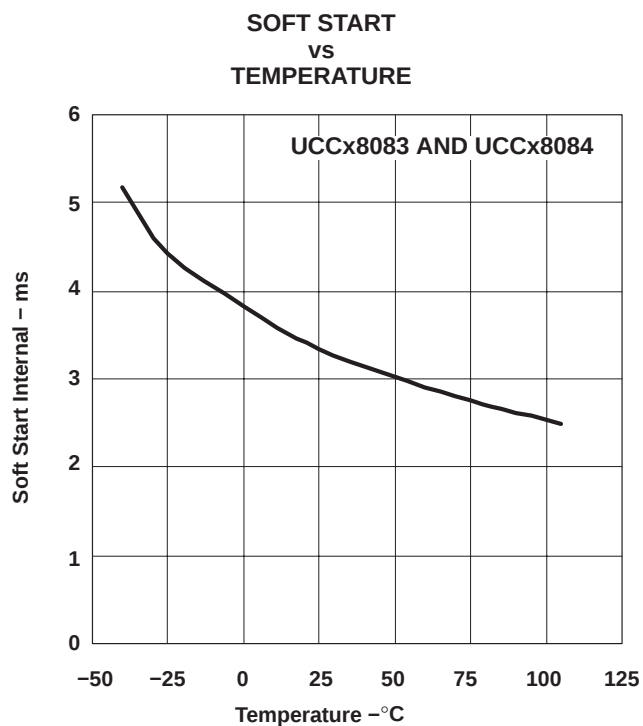


Figure 16

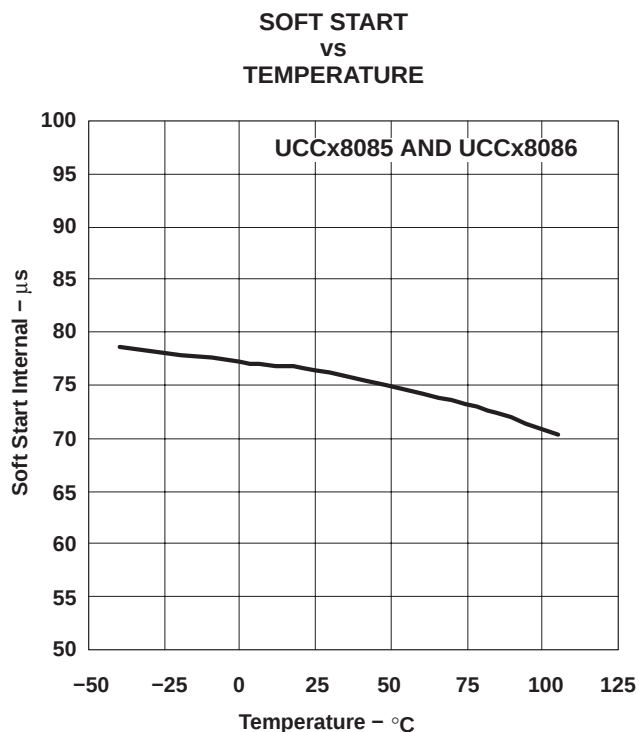


Figure 17

TYPICAL CHARACTERISTICS

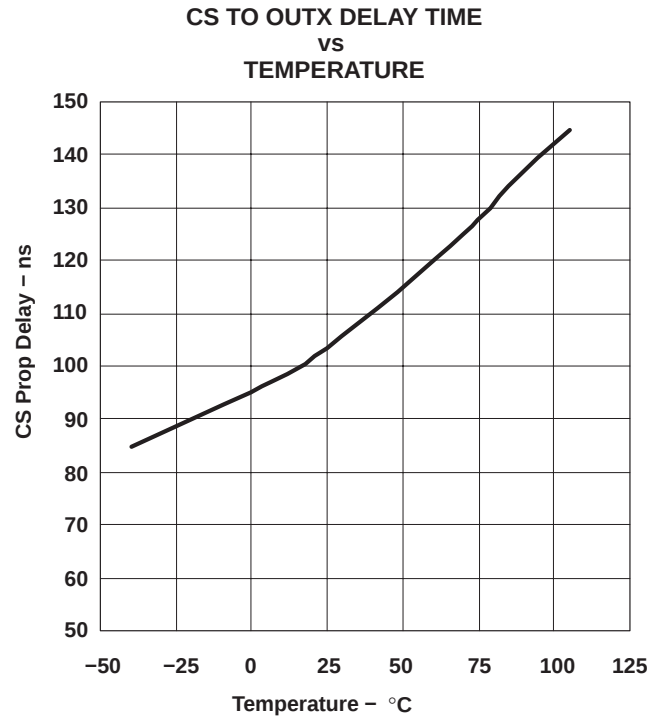


Figure 18

RELATED PRODUCTS

UCC3808, 8-Pin Low Power Current Mode Push-Pull PWM, (SLUS168)

UCC3808A, 8-Pin Low-Power Current-Mode Push-Pull PWM, (SLUS456)

UCC3806, Low Power, Dual Output, Current Mode PWM Controller, (SLUS272)

Table 1. 8-Pin Push-Pull PWM Controller Family Feature Comparison

Part Number	UVLO On	UVLO Off	CS Discharge FET	Error Amplifier	Programmable Slope Compensation	Internal Softstart
UCC38083	12.5 V	8.3 V	Yes	No	Yes	Yes
UCC38084	4.3 V	4.1 V	Yes	No	Yes	Yes
UCC38085	12.5 V	8.3 V	Yes	No	Yes	No
UCC38086	4.3 V	4.1 V	Yes	No	Yes	No
UCC3808A-1	12.5 V	8.3 V	Yes	Yes	No	Yes
UCC3808A-2	4.3 V	4.1 V	Yes	Yes	No	Yes
UCC3808-1	12.5 V	8.3 V	No	Yes	No	Yes
UCC3808-2	4.3 V	4.1 V	No	Yes	No	Yes

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC28083D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28083DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28083DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28083DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28083P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28083PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28083PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC28083PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC28084D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28084DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28084DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28084DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28084P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28084PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28084PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC28084PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC28084PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC28084PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC28085D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28085DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28085DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28085DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28085P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28085PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28085PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC28085PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC28086D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28086DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28086DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28086DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28086P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28086PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28086PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC28086PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC28086PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC28086PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38083D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38083DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38083DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38083DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38083P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38083PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38084D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38084DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38084DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38084DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38084P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38084PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38084PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38084PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38084PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38084PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38085D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC38085DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38085P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38085PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38086D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38086DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38086DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38086DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38086P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38086PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28083DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28084DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28084PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC28085DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28086DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28086PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC38083DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38084DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38084PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC38086DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28083DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC28084DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC28084PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC28085DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC28086DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC28086PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC38083DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC38084DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC38084PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC38086DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

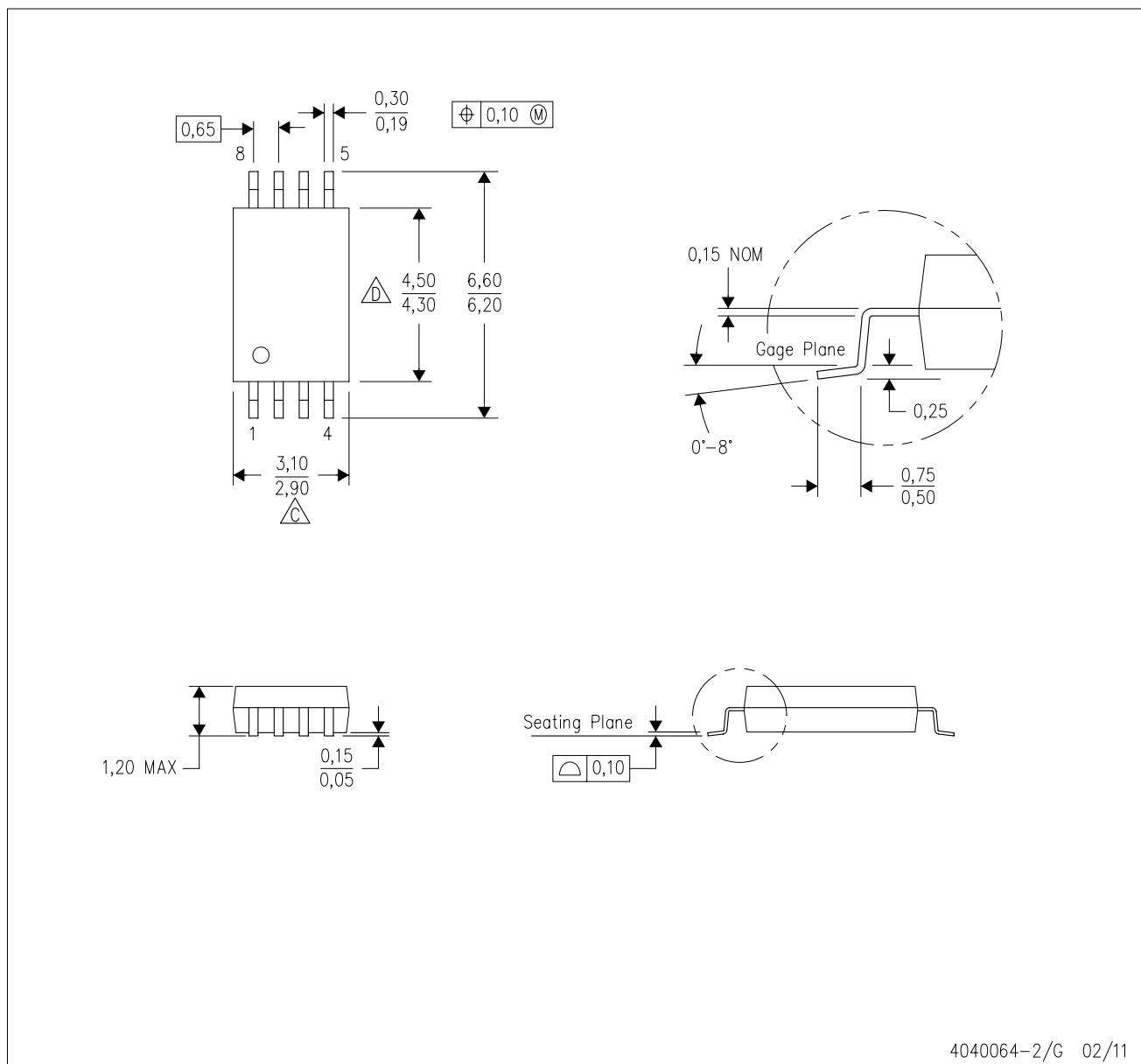
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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