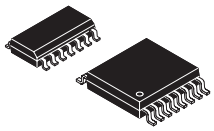


SLUS329B − JUNE 1998 − REVISED FEBRUARY 2005

ADVANCED HIGH-POWER FACTOR PREREGULATOR

FEATURES

- **Controls Boost PWM to Near-Unity Power Factor**
- **Limits Line Current Distortion To < 3%**
- **World-Wide Operation Without Switches**
- **Accurate Power Limiting**
- **Fixed-Frequency Average Current-Mode Control**
- **High Bandwidth (5 MHz), Low-Offset Current Amplifier**
- **Integrated Current- and Voltage Amplifier Output Clamps**
- **Multiplier Improvements: Linearity, 500 mV V_{AC} Offset (Eliminates External Resistor), 0 V to 5 V Multout Common-Mode Range**
- **V_{REF} GOOD Comparator**
- **Faster and Improved Accuracy ENABLE Comparator**
- **UVLO Options (16 V/10 V or 10.5 V/10 V)**
- **300-μA Start-Up Supply Current**

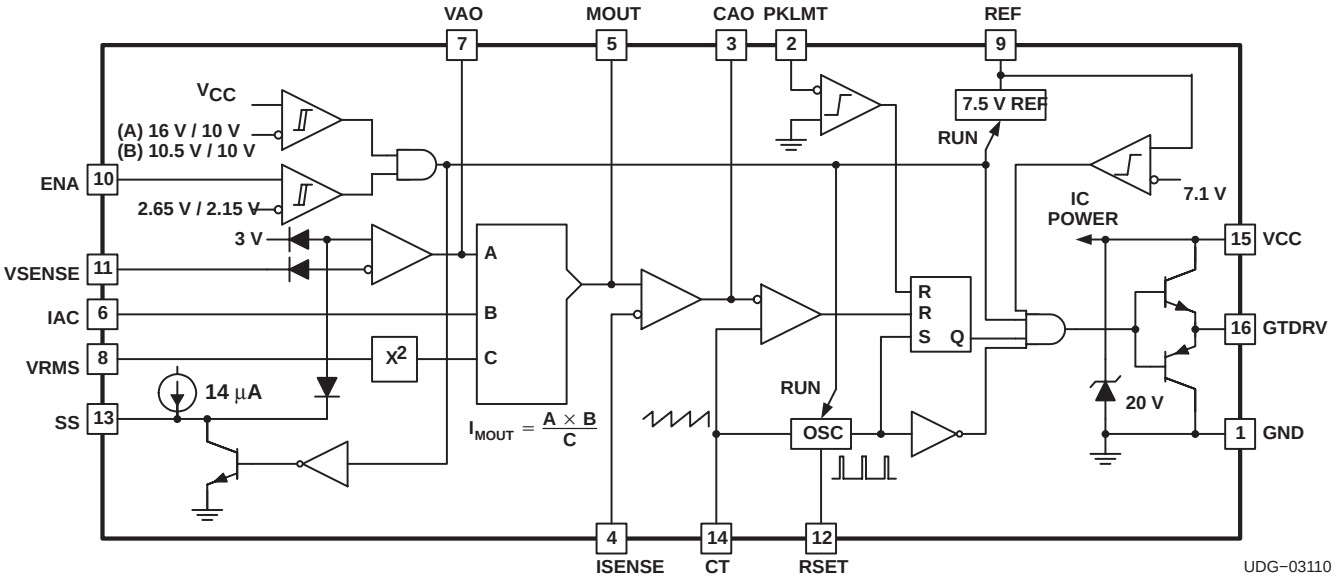
DESCRIPTION

The UC3854A/B products are pin compatible enhanced versions of the UC3854. Like the UC3854, these products provide all of the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage. To do this the UC3854A/B uses average current mode control. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, unlike peak current mode control.

A 1% 7.5 V reference, fixed frequency oscillator, PWM, voltage amplifier with soft-start, line voltage feedforward (V_{RMS} squarer), input supply voltage clamp, and over current comparator round out the list of features.

Available in the 16-pin N (PDIP), DW (SOIC-Wide), and J (CDIP) and 20-pin Q (PLCC) package. See ordering information on page 3 for availability by temperature range.

BLOCK DIAGRAM



DESCRIPTION (continued)

The UC3854A/B products improve upon the UC3854 by offering a wide bandwidth, low offset current amplifier, a faster responding and improved accuracy enable comparator, a VREF GOOD comparator, UVLO threshold options (16 V/10 V for offline, 10.5 V/10 V for startup from an auxiliary 12 V regulator), lower startup supply current, and an enhanced multiply/divide circuit. New features like the amplifier output clamps, improved amplifier current sinking capability, and low offset VAC pin reduce the external component count while improving performance. Improved common mode input range of the multiplier output/current amplifier input allow the designer greater flexibility in choosing a method for current sensing. Unlike its predecessor, R_{SET} controls only oscillator charging current and has no effect on clamping the maximum multiplier output current. This current is now clamped to a maximum of $2 \times I_{AC}$ at all times which simplifies the design process and provides foldback power limiting during brownout and extreme low line conditions.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UCX854A, UCX854B	UNIT
Supply voltage, V_{CC}		22	V
GTDRV current, I_{GTDRV}	Continuous	0.5	A
GTDRV Current, I_{GTDRV}	50% duty cycle	1.5	A
Input voltage	VSENSE, VRMS, ISENSE MOUT	11	V
	PKLMT	5	V
Input current	RSET, IAC, PKLMT, ENA	10	mA
Power dissipation		1	W
Junction temperature, T_J		−55 to 150	°C
Storage temperature, T_{stg}		−65 to 150	
Lead temperature, T_{sol}, 1,6 mm (1/16 inch) from case for 10 seconds		300	

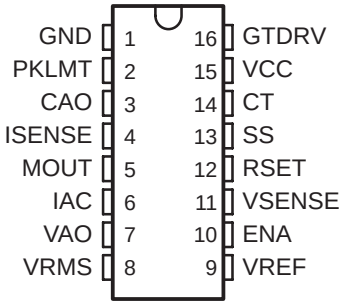
(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal. ENA input is internally clamped to approximately 10 V.

RECOMMENDED OPERATING CONDITIONS

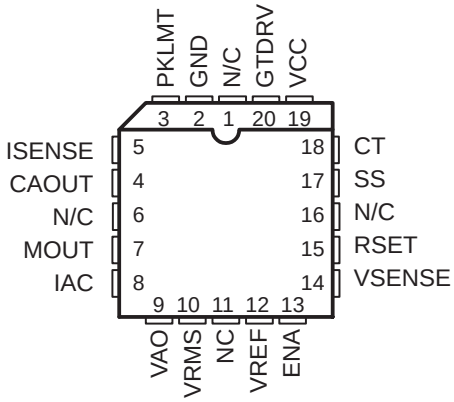
			MIN	MAX	UNIT
Supply voltage, V_{CC}			10	20	V
Operating junction temperature, T_J	UC1854X		−55	125	°C
	UC2854X		−40	85	
	UC3854X		0	70	

PACKAGE DESCRIPTION

J, N and DW PACKAGES
(TOP VIEW)



Q PACKAGE
(TOP VIEW)



N/C − No connection

ORDERING INFORMATION

T_A	UVLO TURN-ON (V)	UVLO TURN-OFF (V)	PART NUMBERS			
			CDIP−16 (J)	PDIP−16 (N)	SOIC−16 (DW)	PLCC−20 (Q)
−55°C to 125°C	16	10	−	−	−	−
	10.5	10	UC1854BJ	−	−	−
−40°C to 85°C	16	10	UC2854AJ	UC2854AN	UC2854ADW	UC2854AQ
	10.5	10	UC2854BJ	UC2854BN	UC2854BDW	UC2854BQ
0°C to 70°C	16	10	−	UC3854AN	UC3854ADW	−
	10.5	10	−	UC3854BN	UC3854BDW	−

(1) The DW and Q packages are available taped and reeled. Add TR suffix to device type (e.g. UC2854ADWTR) to order quantities of 2,000 devices per reel for the DW package and 1,000 devices per reel for the Q package.

THERMAL RESISTANCE

RESISTANCES	PACKAGED DEVICES			
	CDIP−16 (J)	PDIP−16 (N)	SOP−16 (DW)	PLCC−20 (Q)
θ_{JC} (°C/W)	28(2)	45	27	34
θ_{JA} (°C/W)	80−120	90(3)	50−130(3)	43−75(3)

(2) θ_{JC} data values stated are derived from MIL-STD-1835B which states “the baseline values shown are worst case (mean +2s) for a 60 × 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14,400 square mils. For device die sizes greater than 14,400 square mils use the following values, dual-in-line, 11°C/W; flat pack and pin grid array, 10°C/W.

(3) θ_{JA} (junction-to-ambient) applies to devices mounted to five square inch FR4 PC board with one ounce copper where noted. When resitance range is given, lower values are for five square inch aluminum PC board. Test PWB is 0.062 inches thick and typically uses 0.635 mm trace widths for power packages and 1.3 mm trace widths for non-power packages with a 100 × 100 mil probe land are at the end of each trace.

ELECTRICAL CHARACTERISTICS

V_{CC} = 18 V, R_T = 8.2 kΩ, C_T = 1.5 nF, V_{PKLMT} = 1 V, V_{VRMS} = 1.5 V, I_{IAC} = 100 μA, I_{ISENSE} = 0 V, V_{CAO} = 3.5 V, V_{VAO} = 5 V, V_{VSENSE} = 3 V, −40°C < T_A < 85°C for the UC2854A and UC2854B, and 0°C < T_A <70°C for the UC3854A and UC3854B, and T_A = T_J (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL						
	Supply current, off	CAO = 0 V, VAO = 0 V, V_{CC} = V_{UVLO}−0.3 V		250	400	μA
	Supply current, on			12	18	mA
	V_{CC} turn-on threshold voltage	UCx854A	15.0	16.0	17.5	V
		UCx854B	8.0	10.5	11.2	
	V_{CC} turn-off threshold voltage		9	10	12	
	V_{CC} clamp	I_{VCC} = $I_{VCC(on)}$ + 5 mA	18	20	22	
VOLTAGE AMPLIFIER						
	Input voltage		2.9	3.0	3.1	V
	V_{SENSE} bias current		−500	−25	500	nA
	Open loop gain	2 V ≤ V_{OUT} ≤ 5 V	70	100		dB
V_{OH}	High-level output voltage	I_{LOAD} = −500 μA		6		V
V_{OL}	Low-level output voltage	I_{LOAD} = 500 μA		0.3	0.5	V
I_{SC}	Output short-circuit current	V_{OUT} = 0 V		1.5	3.5	mA
	Gain bandwidth product(1)	f_{IN} = 100 kHz, 10 mV_{P-P}		1		MHz
CURRENT AMPLIFIER						
	Input offset voltage	V_{CM} = 0 V, T_A = 25°C	−4		0	mV
		V_{CM} = 0 V, overtemperature	−5.5		0	
	Input bias current, I_{SENSE}	V_{CM} = 0 V	−500		500	nA
	Open loop gain	2 V ≤ V_{OUT} ≤ 6 V	80	110		dB
V_{OH}	High-level output voltage	I_{LOAD} = −500 μA		8		V
V_{OL}	Low-level output voltage	I_{LOAD} = 500 μA		0.3	0.5	
I_{SC}	Output short-circuit current	V_{OUT} = 0 V		1.5	3.5	mA
CMRR	Common mode rejection range		−0.3		5.0	V
	Gain bandwidth product(1)	f_{IN} = 100 kHz, 10 mV_{P-P}	3	5		MHz
REFERENCE						
	Output voltage	I_{REF} = 0 mA, T_A = 25°C	7.4	7.5	7.6	V
		I_{REF} = 0 mA	7.35	7.50	7.65	
	Load regulation	1 mA ≤ I_{REF} ≤ 10 mA	0	8	20	mV
	Line regulation	12 V ≤ V_{CC} ≤ 18 V	0	14	25	
I_{SC}	Short circuit current	V_{REF} = 0 V	25	35	60	mA

(1) Ensured by design. Not production tested.

(2) Gain constant. $(K) = \dfrac{I_{IAC} \times \left(V_{VAO} - 1.5\ V\right)}{\left[\left(V_{VRMS}\right)^2 \times I_{MOUT}\right]}$

ELECTRICAL CHARACTERISTICS

V_{CC} = 18 V, R_T = 8.2 kΩ, C_T = 1.5 nF, V_{PKLMT} = 1 V, V_{VRMS} = 1.5 V, I_{IAC} = 100 µA, I_{ISENSE} = 0 V, V_{CAO} = 3.5 V, V_{VAO} = 5 V, V_{VSENSE} = 3 V, −40°C < T_A < 85°C for the UC2854A and UC2854B, and 0°C < T_A <70°C for the UC3854A and UC3854B, and T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
	Initial accuracy	T_A = 25°C	85	100	115	kHz
	Voltage stability	12 V ≤ V_{CC} ≤ 18 V		1%		
	Total variation	Line, temperature	80		120	kHz
	Ramp amplitude (peak-to-peak)		4.9		5.9	V
	Ramp valley voltage		0.8		1.3	
ENABLE/SOFT-START/CURRENT LIMIT						
	Enable threshold voltage		2.35	2.55	2.80	V
	Enable hysteresis	V_{FAULT} = 2.5 V		500	600	mV
	Enable input bias current	V_{ENA} = 0 V		−2	−5	µA
	Propagation delay to disable time(1)	Enable overdrive = 100 mV		300		ns
	Soft-start charge current	V_{SS} = 2.5 V	10	14	24	
	Peak limit offset voltage		−15		15	mV
	Peak limit input current	V_{PKLMT} = −0.1 V	−200	−100		µA
	Peak limit propagation delay time(1)			150		ns
MULTIPLIER						
	Output current, I_{AC} limited	I_{AC} = 100 µA, V_{RMS} = 1 V, R_{SET} = 10 kΩ	−220	−200	−170	µA
	Output current, zero	I_{AC} = 0 µA, R_{SET} = 10 kΩ	−2.0	−0.2	2.0	
	Output current, power limited	V_{RMS} = 1.5 V, Va = 6 V	−230	−200	−170	
	Output current	V_{RMS} = 1.5 V, Va = 2 V		−22		µA
		V_{RMS} = 1.5 V, Va = 5 V		−156		µA
		V_{RMS} = 5 V, Va = 2 V		−2		
		V_{RMS} = 5 V, Va = 5 V		−14		
	Gain constant(2)	V_{RMS} = 1.5 V, Va = 6V, T_A = 25°C	−1.1	−1.0	−0.9	A/A
GATE DRIVER						
V_{OH}	High-level output voltage	I_{OUT} = −200 mA, V_{CC} = 15 V	12.0	12.8		V
V_{OL}	Low-level output voltage	I_{OUT} = 200 mA		1.0	2.2	
		I_{OUT} = 10 mA		300	500	mV
	Low-level UVLO voltage	I_{OUT} = 50 mA, V_{CC} = 0 V		0.9	1.5	V
	Output rise time(1)	C_{LOAD} = 1 nF		35		ns
	Output fall time(1)	C_{LOAD} = 1 nF		35		
	Output peak current(1)	C_{LOAD} = 10 nF		1.0		A

(1) Ensured by design. Not production tested.

(2) Gain constant. $(K) = \dfrac{I_{IAC} \times \left(V_{VAO} - 1.5\ V\right\}}{\left[\left(V_{VRMS}\right)^2 \times I_{MOUT}\right]}$

TERMINAL FUNCTIONS

TERMINAL NAME	PACKAGES J/N/DW	PACKAGES Q/L	I/O	DESCRIPTION
CAO	3	4	O	Output of the wide bandwidth current amplifier and one of the inputs to the PWM duty-cycle comparator. The output signal generated by this amplifier commands the PWM to force the correct input current. The output can swing from 0.1 V to 7.5 V.
CT	14	18	I	Capacitor from CT to GND sets the PWM oscillator frequency
ENA	10	13	I	A nominal voltage above 2.65 V on this pin allows the device to begin operating. Once operating, the device shuts off if this pin goes below 2.15 V nominal.
GND	1	2	−	All bypass and timing capacitors connected to GND should have leads as short and direct as possible. All voltages are measured with respect GND.
GTDRV	16	20	O	Output of the PWM is a 1.5-A peak totem-pole MOSFET gate driver on GTDRV. This output is internally clamped to 15 V so that the device can be operated with VCC as high as 35 V. Use a series gate resistor of at least 5 Ω to prevent interaction between the gate impedance and the GTDRV output driver that might cause the GTDRV output to overshoot excessively. Some overshoot of the GTDRV output is always expected when driving a capacitive load.
IAC	6	8	I	Current input to the multiplier, proportional to the instantaneous line voltage. This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (IAC) to MOUT, so this is the only multiplier input that should be used for sensing instantaneous line voltage. The nominal voltage on IAC is 6 V, so in addition to a resistor from I_{AC} to rectified 60 Hz, connect a resistor from IAC to VREF. If the resistor to VREF is one-fourth of the value of the resistor to the rectifier, then the 6-V offset is cancelled, and the line current has minimal cross-over distortion.
ISENSE	4	5	I	Switch current sensing input. This is the inverting input to the current amplifier. This input and the non-inverting input MOUT remain functional down to and below GND. Care should be taken to avoid taking these inputs below −0.5V, because they are protected with diodes to GND.
MOUT	5	7	I/O	Multiplier output and current sense plus. The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at MOUT. The cautions about taking ISENSE below −0.5V also apply to MOUT. As the multiplier output is a current, this is a high-impedance input similar to I_{SENSE}, so the current amplifier can be configured as a differential amplifier to reject GND noise.
PKLMT	2	3	I	Peak limit. The threshold for PKLMT is 0.0 V. Connect this input to the negative voltage on the current sense resistor. Use a resistor to REF to offset the negative current sense signal up to GND.
RSET	12	15	I	Oscillator charging current and multiplier limit set. A resistor from RSET to ground programs oscillator charging current. Multiplier output current does not exceed 3.75V divided by the resistor from RSET to ground.
SS	13	17	I	Soft-start. SS remains at GND as long as the device is disabled or V_{CC} is too low. SS pulls up to over 8 V by an internal 14-mA current source when both V_{CC} becomes valid and the device is enabled. SS acts as the reference input to the voltage amplifier if SS is below VREF. With a large capacitor from SS to GND, the reference to the voltage regulating amplifier rises slowly, and increase the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS will quickly discharge to ground and disable the PWM.
VAO	7	9	I	Voltage amplifier output
VCC	15	19	I	Positive supply rail
VREF	9	12	O	Used to set the peak limit point and as an internal reference for various device functions. This voltage must be present for the device to operate.
VRMS	8	10	I	One of the inputs into the multiplier. This pin provides the input RMS voltage to the multiplier circuitry.
VSENSE	11	14	I	This pin provides the feedback from the output. This input goes into the voltage error amplifier and the output of the error amplifier is another of the inputs into the multiplier circuit.

FUNCTIONAL DESCRIPTION

The UC3854A and UC3854B family of products are designed as pin compatible upgrades to the industry standard UC3854 active power factor correction circuits. The circuit enhancements allow the user to eliminate in most cases several external components currently required to successfully apply the UC3854. In addition, linearity improvements to the multiply, square and divide circuitry optimizes overall system performance. Detailed descriptions of the circuit enhancements are provided below. For in-depth design applications reference data refer to the application notes, *UC3854 Controlled Power Factor Correction Circuit Design* (SLUA144) and *UC3854A and UC3854B Advanced Power Factor Correction Control ICs* (SLUA177).

Multiply/Square and Divide

The UC3854A/B multiplier design maintains the same gain constant $\left(K = \frac{-1}{V}\right)$ as the UC3854. The relationship between the inputs and output current is given as:

$$I_{MOUT} = I_{iAC} \times \frac{\left(V_{VAO} - 1.5\ V\right)}{K \times \left(V_{VRMS}\right)^2} \quad (1)$$

This is nearly the same as the UC3854, but circuit differences have improved the performance and application.

The first difference is with the IAC input. The UC3854A/B regulated this pin voltage to the nominal 500 mV over the full operating temperature range, rather than the 6.0 V used on the UC3854. The low offset voltage eliminates the need for a line zero crossing compensating resistor to VREF from IAC that UC3854 designs require. The maximum current at high line into IAC should be limited to 250 μA for best performance.

Therefore, if $V_{VAC(max)}$ = 270 V,

$$R_{IAC} = \frac{270 \times 1.414}{250\ \mu A} = 1.53\ M\Omega \quad (2)$$

The V_{RMS} pin linear operating range is improved with the UC3854A/B as well. The input range for VRMS extends from 0 V to 5.5 V. Since the UC3854A squaring circuit employs an analog multiplier, rather than a linear approximation, accuracy is improved, and discontinuities are eliminated. The external divider network connected to VRMS should produce 1.5 V at low line (85 VAC). This puts 4.77 V on VRMS at high line (27 VAC) which is well within its operating range.

The voltage amplifier output forms the third input to the multiplier and is internally clamped to 6.0 V. This eliminated an external zener clamp often used in UC3854 designs. The offset voltage at this input to the multiplier has been raised on the UC3854A/B to 1.5 V.

The multiplier output pin, which is also common to the current amplifier non-inverting input, has a −0.3 V to 5.0 V output range, compared to the −0.3 V to 2.5 V range of the UC3854. This improvement allows the UC3854A/B to be used in applications where the current sense signal amplitude is very large.

Voltage Amplifier

The UC3854A/B voltage amplifier design is essentially similar to the UC3854 with two exceptions. The first is with the internal connection. The lower voltage reduces the amount of charge on the compensation capacitors, which provides improved recovery form large signal events, such as line dropouts, or power interruption. It also minimizes the dc current flowing through the feedback. The output of the voltage amplifier is also changes. In addition to a 6.0 V temperature compensated clamp, the output short circuit current has been lowered to 2 mA typical, and an active pull down has replaced the passive pull down of the UC3854.

Current Amplifier

The current amplifier for an average current PFC controller needs a low offset voltage in order to minimize AC line current distortion. With this in mind, the UC3854A/B current amplifier has improved the input offset voltage from ±4 mV to 0 V to ±3 mV. The negative offset of the UC3854A/B guarantees that the PWM circuit will not drive the MOSFET is the current command is zero (both current amplifier inputs zero.) Previous designs required an external offset cancellation network to implement this key feature. The bandwidth of the current amplifier has been improved as well to 5 MHz typical. While this is not generally an issue at 50 Hz or 60 Hz inputs, it is essential for 400 Hz input avionics applications

Miscellaneous

Several other important enhancements have been implemented in the UC3854A/B. A V_{CC} supply voltage clamp at 20 V allows the controller to be current fed if desired. The lower startup supply current (250 mA typical), substantially reduces the power requirements of an offline startup resistor. The 10.5 V/10 V UVLO option (UC3854B) enables the controller to be powered off of an auxiliary 12 V supply.

The VREF GOOD comparator guarantees that the MOSFET driver output remains low if the supply of the 7.5 V reference are not yet up. This improvement eliminates the need for external Schottky diodes on the PKLMT and Mult Out pins that some UC3854 designs require. The propagation delay of the disable feature has been improved to 300 ns typical. This delay was proportional to the size of the VREF capacitor on the UC3854, and is typically several orders of magnitude slower.

TYPICAL CHARACTERISTICS

GATE DRIVE TIMING
vs
LOAD CAPACITANCE

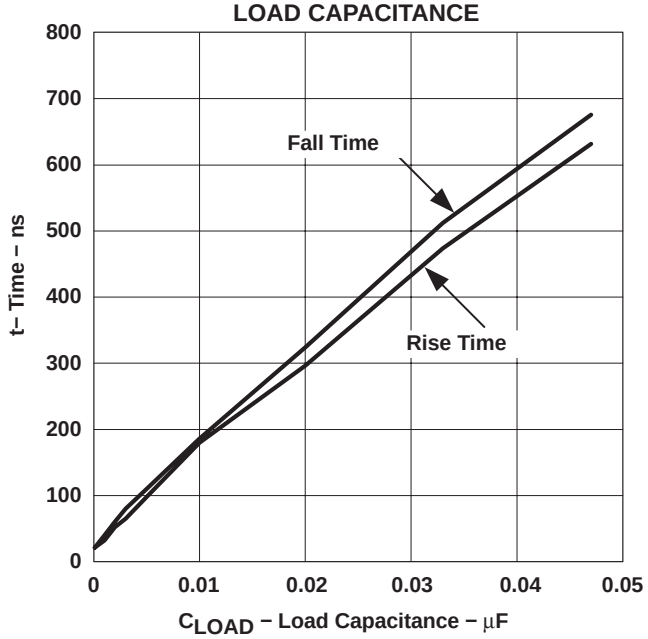


Figure 1

GATE DRIVE MAXIMUM DUTY CYCLE
vs
OSCILLATOR CHARGING RESISTANCE

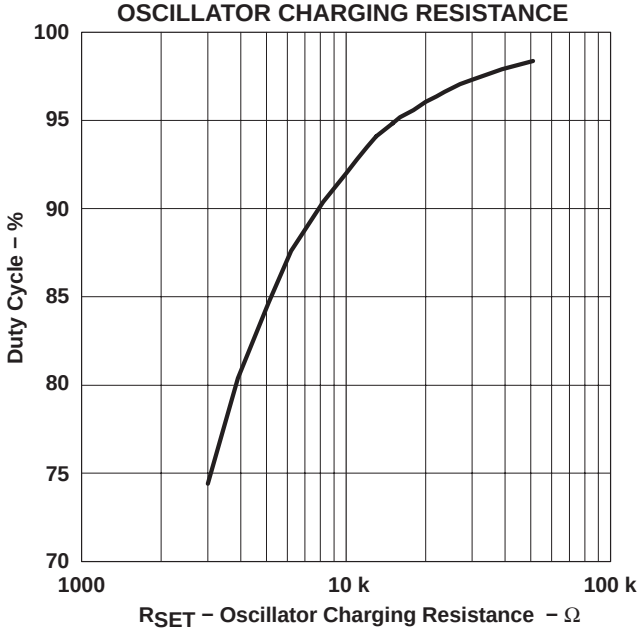


Figure 2

MULTIPLIER GAIN CONSTANT
vs
SUPPLY CURRENT

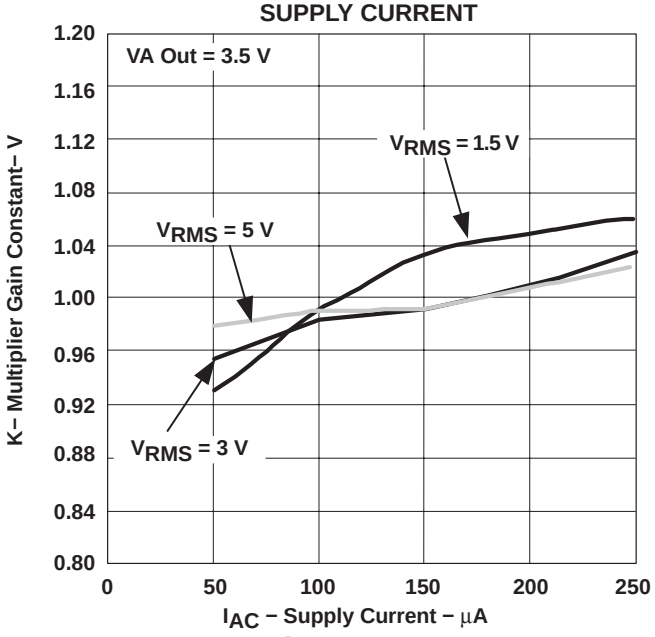


Figure 3

MULTIPLIER GAIN CONSTANT
vs
SUPPLY CURRENT

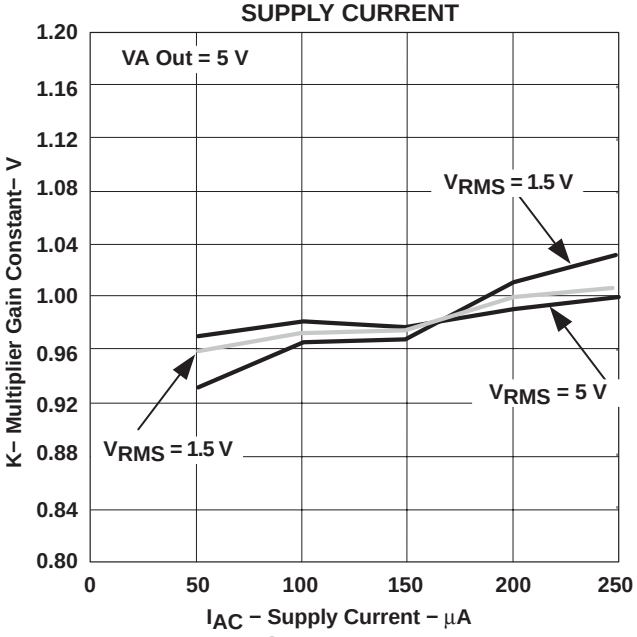


Figure 4

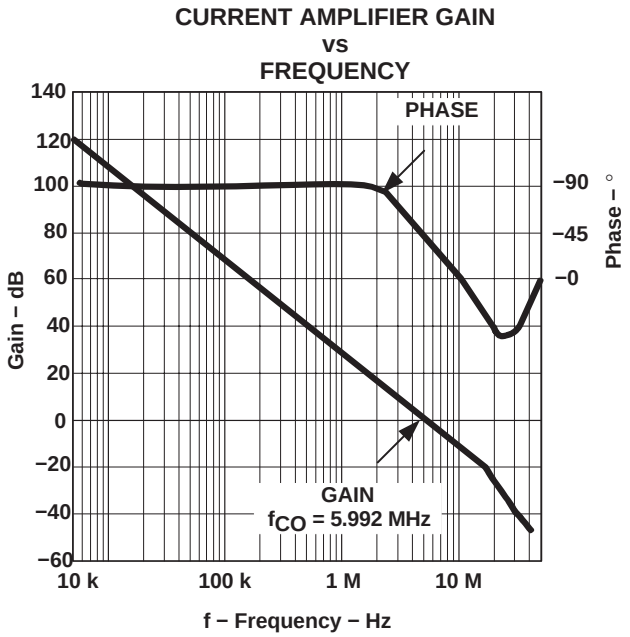


Figure 5

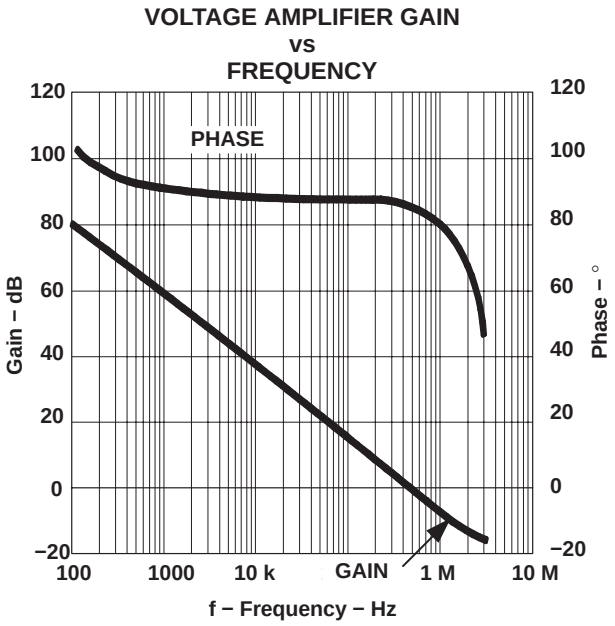


Figure 6

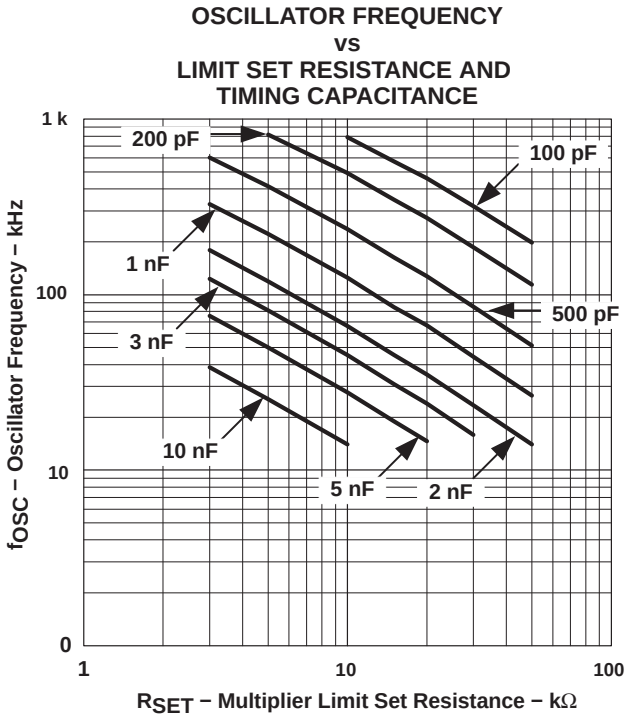
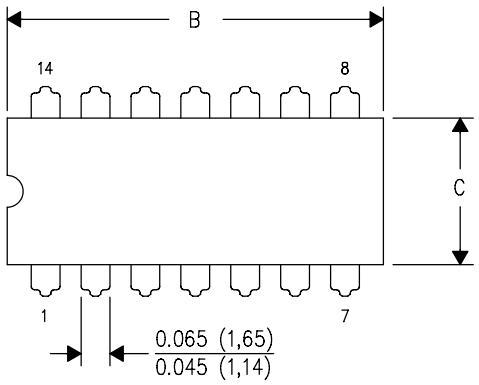


Figure 7

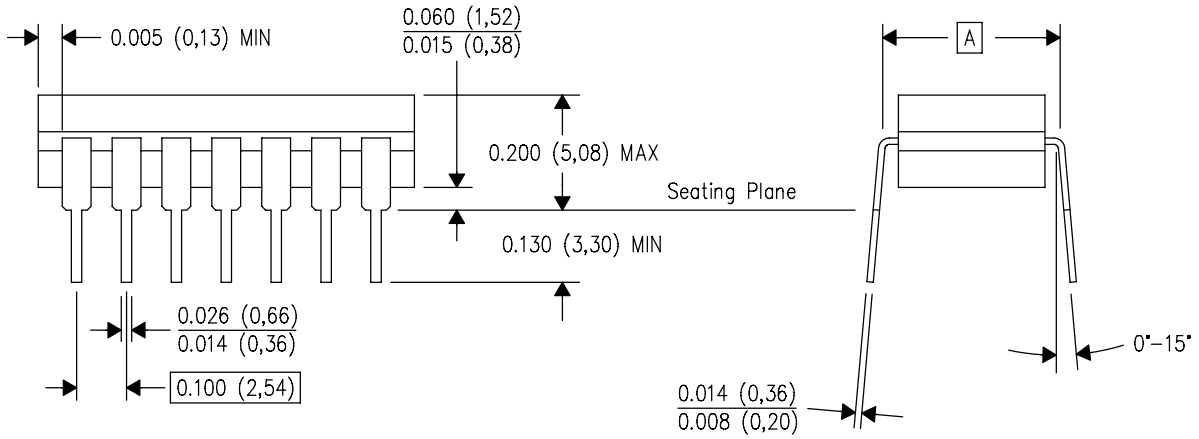
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

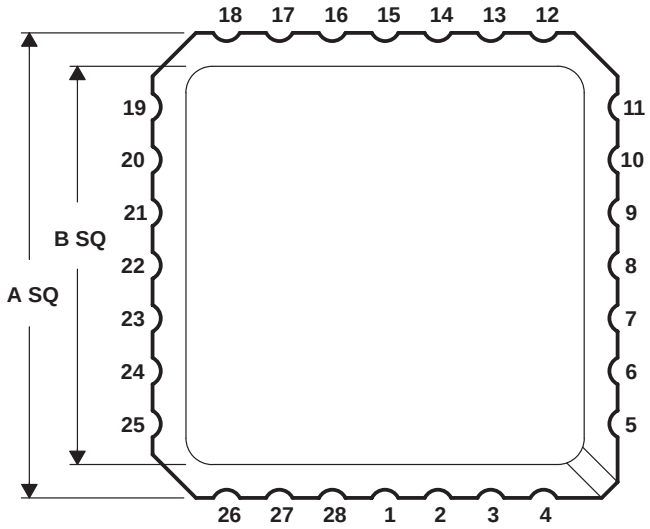


4040083/F 03/03

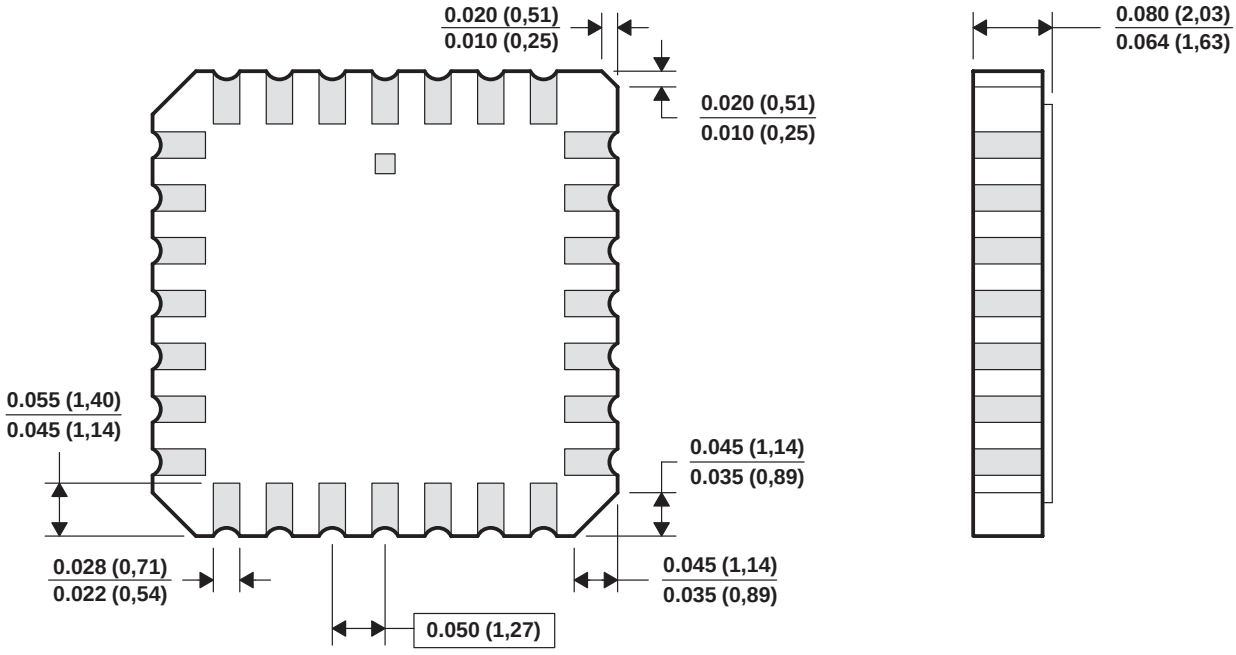
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



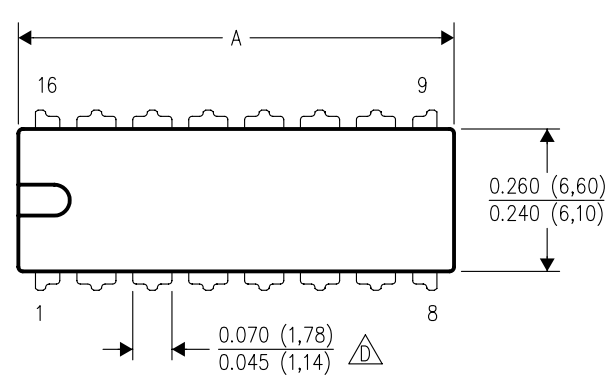
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

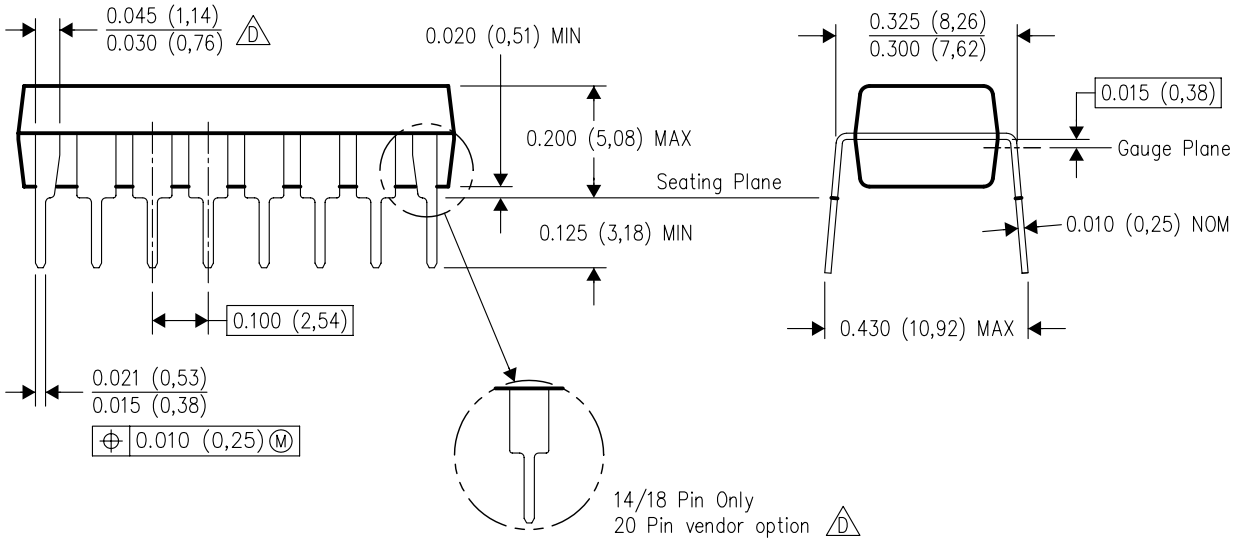
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

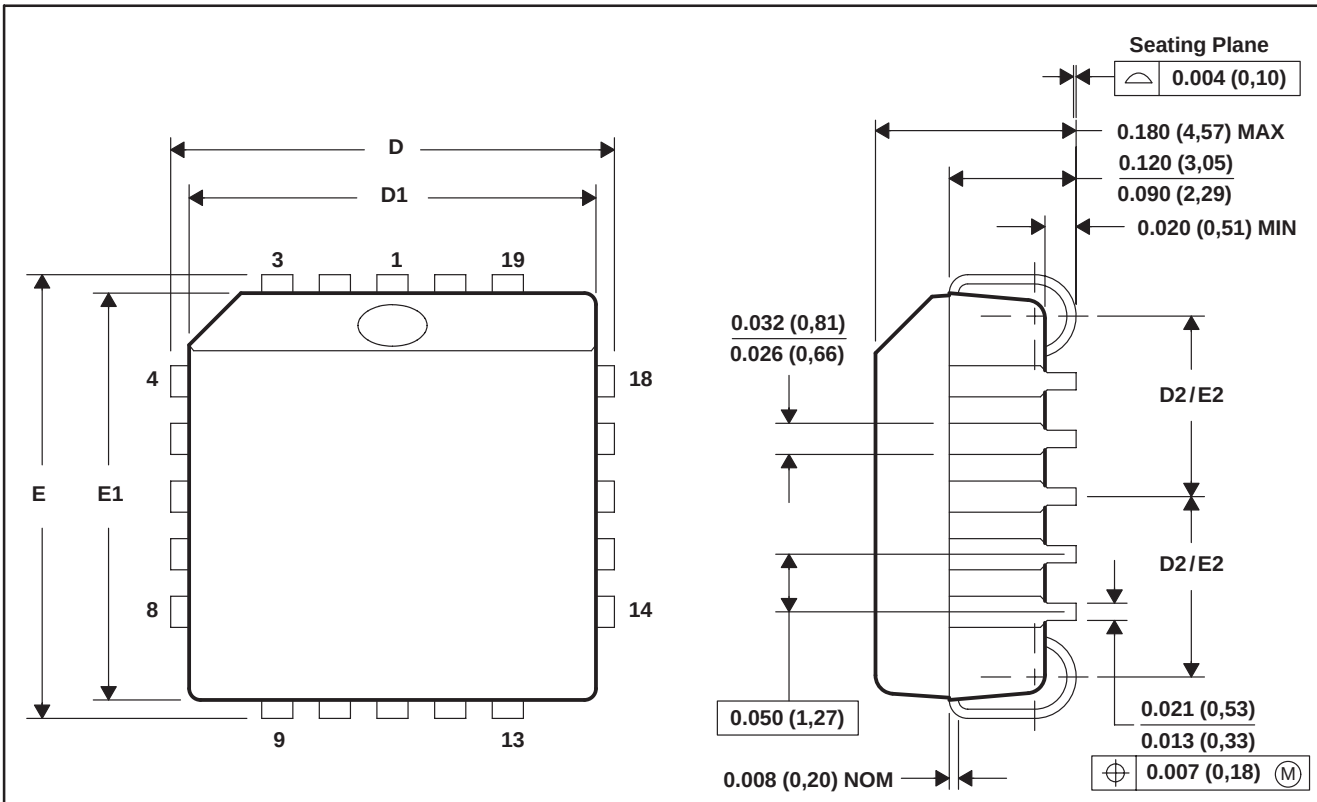
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN

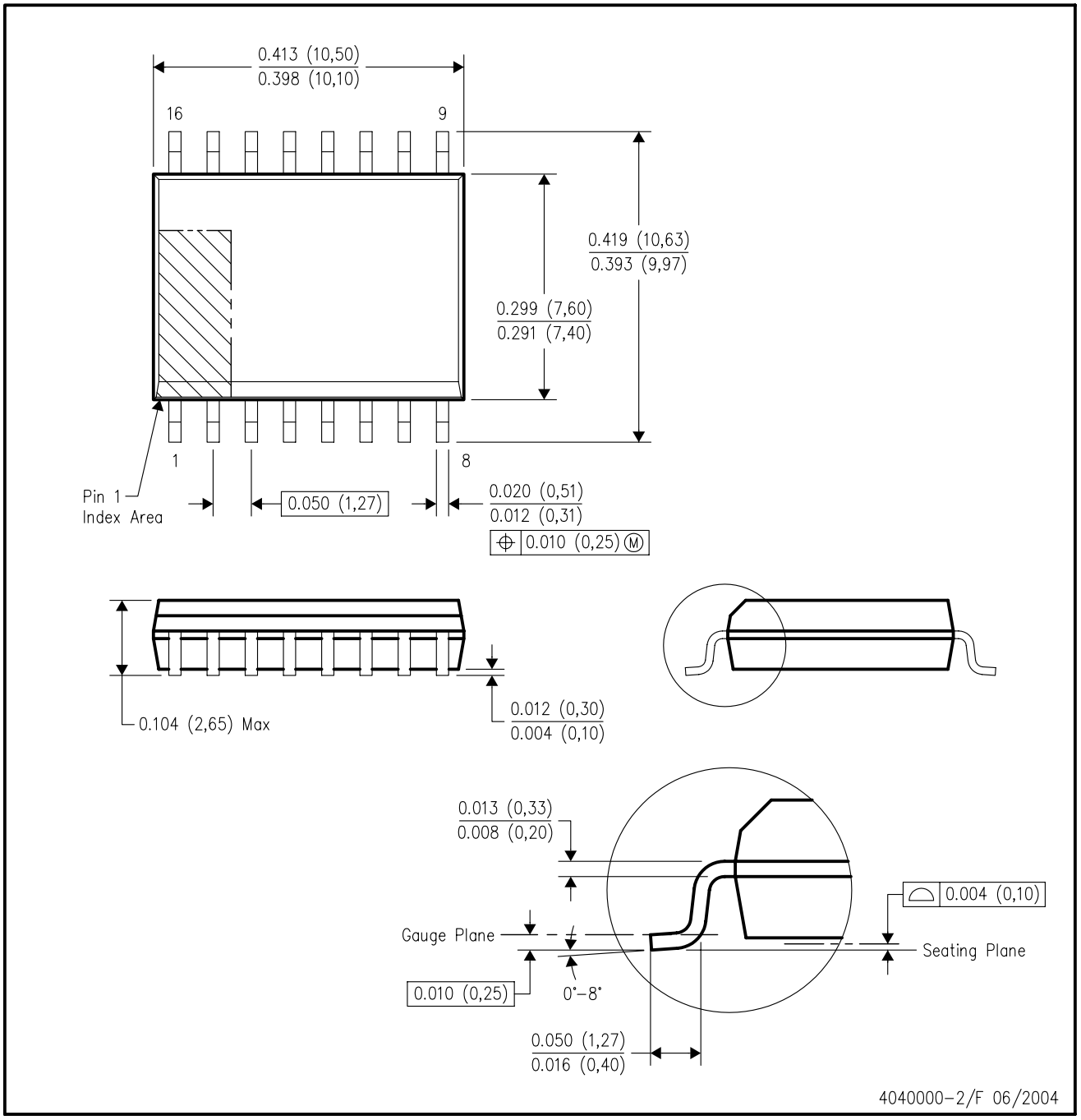


NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

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