Single Channel High-Speed, Low-Side Gate Driver (Based On CMOS Input Threshold with 4-A Peak Source and 4-A Peak Sink)

Check for Samples: UCC27518 , UCC27519

FEATURES

- **Low-Cost, Gate-Driver Device Offering Superior Replacement of NPN and PNP Discrete Solutions**
- **Pin-to-Pin Compatible With TI's TPS2828 and the TPS2829**
- **4-A Peak Source and 4-A Peak Sink Symmetrical Drive**
- **Fast Propagation Delays (17-ns typical)**
- **Fast Rise and Fall Times (8-ns and 7-ns typical)**
- **4.5-V to 18-V Single Supply Range**
- **Outputs Held Low During VDD UVLO (ensures glitch free operation at power-up and power-down)**
- **CMOS Input Logic Threshold (function of supply voltage with hysteresis)**
- **Hysteretic Logic Thresholds for High Noise Immunity**
- **EN Pin for Enable Function (allowed to be no connect)**
- **Output Held Low when Input Pins are Floating**
- **Input Pin Absolute Maximum Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage**
- **Operating Temperature Range of -40°C to 140°C**
- **5-Pin DBV Package (SOT-23)**

APPLICATIONS

- **Switch-Mode Power Supplies**
- **DC-to-DC Converters**
- **Companion Gate Driver Devices for Digital Power Controllers**
- **Solar Power, Motor Control, UPS**
- **Gate Driver for Emerging Wide Band-Gap Power Devices (such as GaN)**

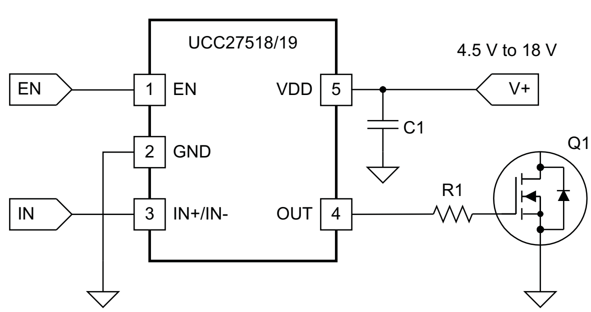
DESCRIPTION

The UCC27518 and UCC27519 single-channel, high-speed, low-side gate driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, UCC27518 and UCC27519 are capable of sourcing and sinking high, peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay typically 17 ns.

The UCC27518 and UCC27519 provide 4-A source, 4-A sink (symmetrical drive) peak-drive current capability at VDD = 12 V.

The UCC27518 and UCC27519 are designed to operate over a wide VDD range of 4.5 V to 18 V and wide temperature range of -40°C to 140°C. Internal Under Voltage Lockout (UVLO) circuitry on VDD pin holds output low outside VDD operating range. The capability to operate at low voltage levels such as below 5 V, along with best in class switching characteristics, is especially suited for driving emerging wide band-gap power switching devices such as GaN power semiconductor devices.

Typical Application Diagrams



DESCRIPTION (CONT.)

The input pin threshold of the UCC27518 and UCC27519 are based on CMOS logic where the threshold voltage is a function of the VDD supply voltage. Typically Input High Threshold (V_{IN-H}) is 55% V_{DD} and Input Low Threshold (V_{IN-L}) is 39% V_{DD}. Wide hysteresis (16% V_{DD} typically) between the high and low thresholds offers excellent noise immunity and allows users to introduce delays using RC circuits between the input PWM signal and the INx pin of the device.

The UCC27518 and UCC27519 also feature a floatable enable function on the EN pin. The EN pin can be left in a no connect condition, which allows pin-to-pin compatibility between the UCC27518, UCC27519 and the TPS2828, TPS2829 respectively. Enable pin threshold is a fixed voltage threshold and does not vary based on V_{DD} pin bias voltage. Typically Enable High Threshold (V_{EN-H}) is 2.1 V and Enable Low Threshold (V_{EN-L}) is 1.25 V.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE/SINK)	INPUT THRESHOLD LOGIC	OPERATING TEMPERATURE RANGE, T_A
UCC27518DBV	SOT-23 5-pin	4-A/4-A (Symmetrical Drive)	Inverting CMOS Logic (follows VDD bias voltage)	-40°C to 140°C
UCC27519DBV			Non-Inverting CMOS Logic (follows VDD bias voltage)	

(1) For the most current package and ordering information, see Package Option Addendum at the end of this document.
(2) All packages use Pb-Free lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations. DRS package is rated MSL level 2.

Table 1. UCC2751x Product Family Summary

PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE/SINK)	INPUT THRESHOLD LOGIC
UCC27511DBV(1)	SOT-23, 6 pin	4-A/8-A (Asymmetrical Drive)	CMOS/TTL-Compatible (low voltage, independent of VDD bias voltage)
UCC27512DRS (1)	3 mm x 3 mm WSON, 6 pin		
UCC27516DRS (1)	3 mm x 3 mm WSON, 6 pin	4-A/4-A (Symmetrical Drive)	
UCC27517DBV (1)	SOT-23, 5 pin		
UCC27518DBV	SOT-23, 5 pin		CMOS (follows VDD bias voltage)
UCC27519DBV	SOT-23, 5 pin		

(1) Visit www.ti.com for the latest product datasheet.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VDD	-0.3	20	V
OUT voltage		-0.3	VDD + 0.3	V
Output continuous current	I_{OUT_DC} (source/sink)		0.3	A
Output pulsed current (0.5 µs)	I_{OUT_pulsed}(source/sink)		4	
IN+, IN-(4), EN		-0.3	20	V
ESD	Human Body Model, HBM		2000	V
ESD	Charged Device Model, CDM SOT-23		500	V
Operating virtual junction temperature range, T_J		-40	150	°C
Storage temperature range, T_{STG}		-65	150	°C
Lead temperature	Soldering, 10 sec.		300	°C
Lead temperature	Reflow		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(4) Maximum voltage on input pins is not restricted by the voltage on the VDD pin.

THERMAL INFORMATION

THERMAL METRIC		UCC27518 SOT-23 DBV 5 PINS	UCC27519 SOT-23 DBV(1) 5 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	217.6	217.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	85.8	85.8	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	44.0	44.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	4.0	4.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	43.2	43.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	4.5	12	18	V
Operating junction temperature range	-40		140	°C
Input voltage, (IN+ and IN-) and Enable (EN)	0		18	V

ELECTRICAL CHARACTERISTICS

VDD = 12 V, $T_A = T_J$ = -40°C to 140°C, 1-µF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNITS
BIAS Currents							
$I_{DD(off)}$	Startup current	VDD = 3.4 V	IN+ = VDD (UCC27519), IN- = GND (UCC27518)	51	85	123	µA
			IN+ = GND (UCC27519), IN- = VDD (UCC27518)	51	70	103	
Under Voltage Lockout (UVLO)							
V_{ON}	Supply start threshold	T_A = 25°C		3.85	4.20	4.57	V
		T_A = -40°C to 140°C		3.80	4.20	4.67	
V_{OFF}	Minimum operating voltage after supply start			3.45	3.9	4.35	
V_{DD_H}	Supply voltage hysteresis			0.19	0.3	0.45	
INPUTS (IN+, IN-)							
V_{IN_H}	Input signal high threshold	VDD = 4.5 V			55	62	%VDD
V_{IN_L}	Input signal low threshold			31	39		
V_{IN_HYS}	Input signal hysteresis				16		
V_{IN_H}	Input signal high threshold	VDD = 12 V			55	59	
V_{IN_L}	Input signal low threshold			31	39		
V_{IN_HYS}	Input signal hysteresis				16		
V_{IN_H}	Input signal high threshold	VDD = 18 V			55	58	
V_{IN_L}	Input signal low threshold			35	38		
V_{IN_HYS}	Input signal hysteresis				17		
ENABLE (EN)							
V_{EN_H}	Enable signal high threshold	VDD = 12 V			2.1	2.3	V
V_{EN_L}	Enable signal low threshold			1.00	1.25		
V_{EN_HYS}	Enable hysteresis				0.86		

ELECTRICAL CHARACTERISTICS (continued)

VDD = 12 V, T_A = T_J = -40°C to 140°C, 1-µF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Source/Sink Current						
$I_{SRC/SNK}$	Source/sink peak current(1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		-4/+4		A
Outputs (OUT)						
V_{DD}-V_{OH}	High output voltage	VDD = 12 V I_{OUT} = -10 mA		50	90	mV
		VDD = 4.5 V I_{OUT} = -10 mA		60	130	
V_{OL}	Low output voltage	VDD = 12 I_{OUT} = 10 mA		5	11	
		VDD = 4.5 V I_{OUT} = 10 mA		6	12	
R_{OH}	Output pull-up resistance(2)	VDD = 12 V I_{OUT} = -10 mA		5.0	7.5	Ω
		VDD = 4.5 V I_{OUT} = -10 mA		5.0	11.0	
R_{OL}	Output pull-down resistance	VDD = 12 V I_{OUT} = 10 mA		0.5	1.0	
		VDD = 4.5 V I_{OUT} = 10 mA		0.6	1.2	
Switching Time						
t_R	Rise time(3)	C_{LOAD} = 1.8 nF		8	12	ns
t_F	Fall time(3)	C_{LOAD} = 1.8 nF		7	11	
t_{D1}	IN+ to output propagation delay(3)	VDD = 10 V 7-V input pulse, C_{LOAD} = 1.8 nF	6	17	25	
t_{D2}	IN- to output propagation delay(3)	VDD = 10 V 7-V input pulse, C_{LOAD} = 1.8 nF	6	17	24	
t_{D3}	EN to output high propagation delay(3)	C_{LOAD} = 1.8 nF, 5-V enable pulse	4	12	16	
t_{D4}	EN to output low propagation delay(3)	C_{LOAD} = 1.8 nF, 5-V enable pulse	4	12	19	

(1) Ensured by Design.
(2) R_{OH} represents on-resistance of P-Channel MOSFET in pull-up structure of the UCC27518 and UCC27519's output stage.
(3) See timing diagrams in Figure 1, Figure 2, Figure 3 and Figure 4.

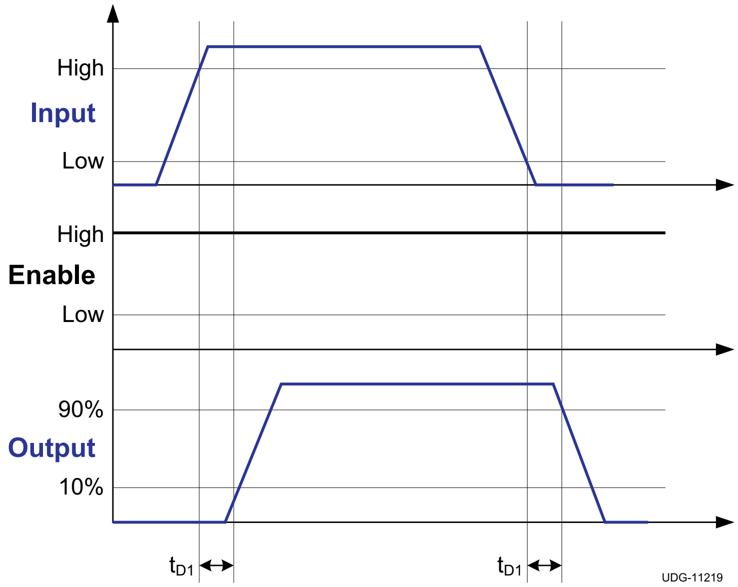


Figure 1. Non-Inverting Configuration (IN+ pin, UCC27519)

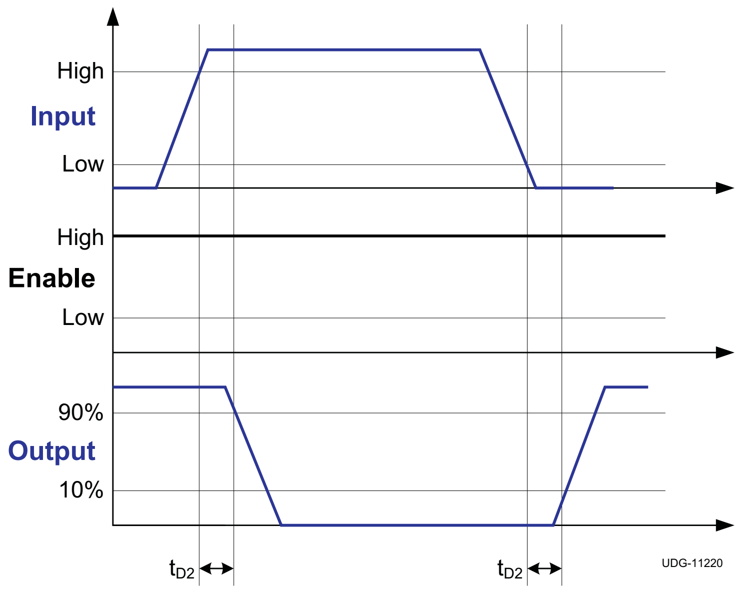


Figure 2. Inverting Configuration (IN- pin, UCC27518)

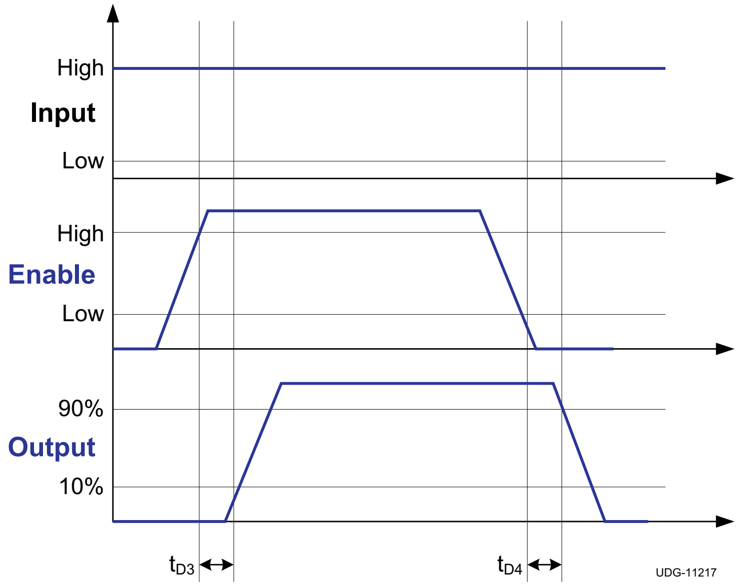


Figure 3. Enable and Disable Function (non-inverting configuration, UCC27519)

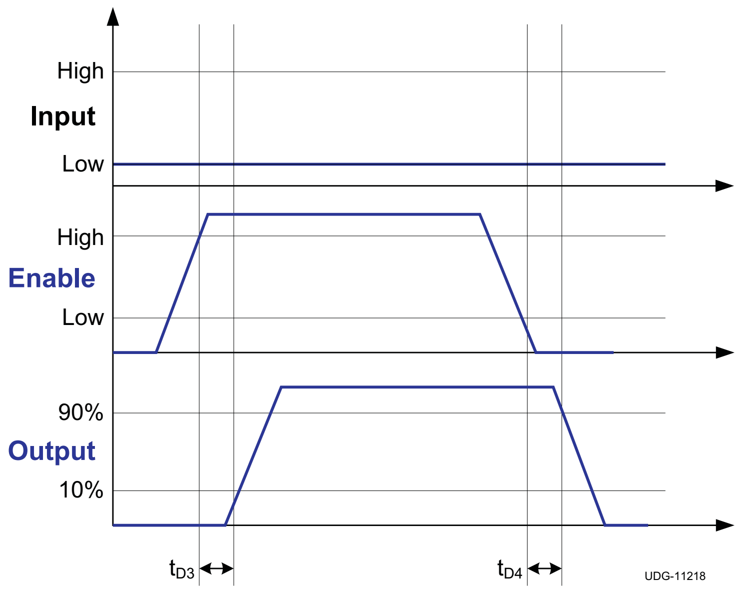
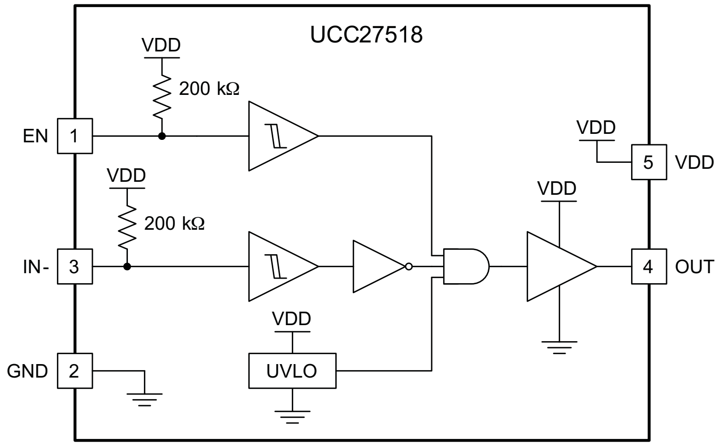


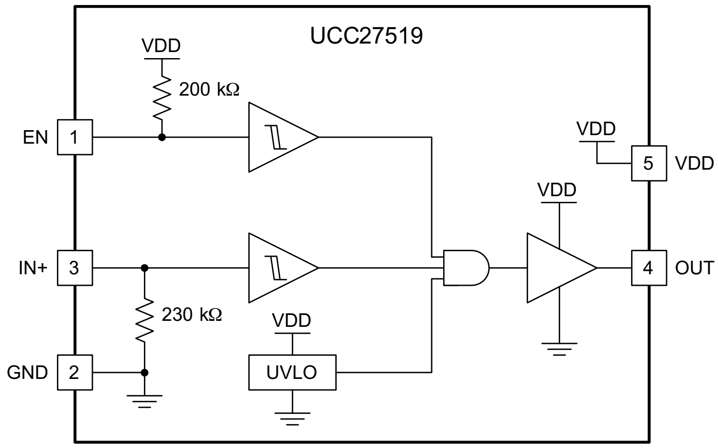
Figure 4. Enable and Disable Function (inverting configuration, UCC27518)

DEVICE INFORMATION

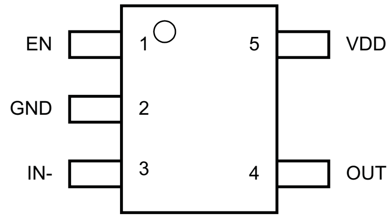
UCC27518 Functional Block Diagram



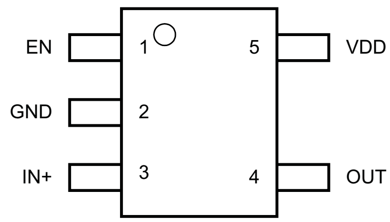
UCC27519 Functional Block Diagram



UCC27518
SOT-23 DBV
(Top View)



UCC27519
SOT-23 DBV
(Top View)



TERMINAL FUNCTIONS

TERMINAL		I/O	FUNCTION
PIN NUMBER	NAME		
1	EN	I	**Enable input:** (EN biased LOW disables output regardless of Input state, EN biased high or floating enables output, EN is allowed to float hence it is pin-to-pin compatible with TPS282X N/C pin)
2	GND	-	**Ground:** All signals referenced to this pin.
3	IN-	I	**Input:** Inverting input in the UCC27518, output held LOW if IN- is unbiased or floating
	IN+	I	**Input:** Non-inverting input in the UCC27519, output held LOW if IN+ is unbiased or floating
4	OUT	O	**Sourcing and sinking current output of driver**.
5	VDD	i	**Supply input.**

Table 2. Device Logic Table

EN	UCC27518		UCC27519	
	IN- PIN	OUT PIN	IN+ PIN	OUT PIN
H	L	H	L	L
H	H	L	H	H
L	Any	L	Any	L
Any	x(1)	L	x(1)	L
x(1)	L	H	L	L
x(1)	H	L	H	H

(1) x = Floating Condition

TYPICAL CHARACTERISTICS

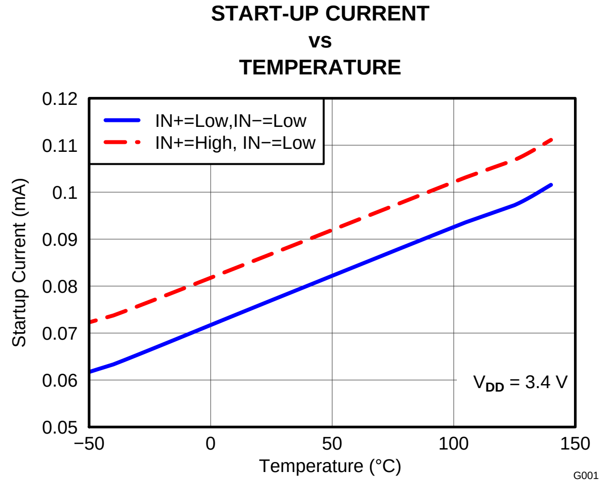


Figure 5.

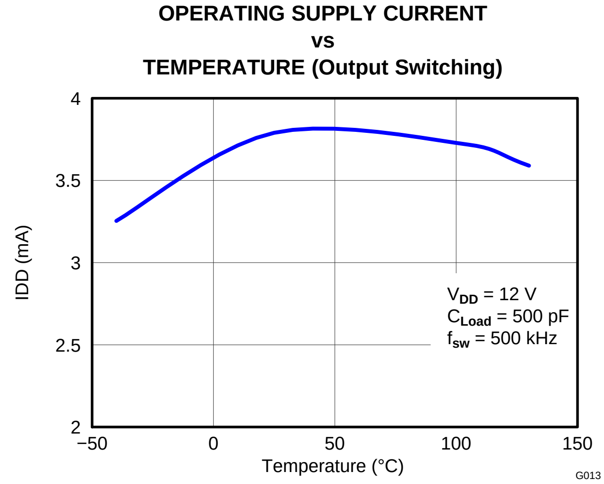


Figure 6.

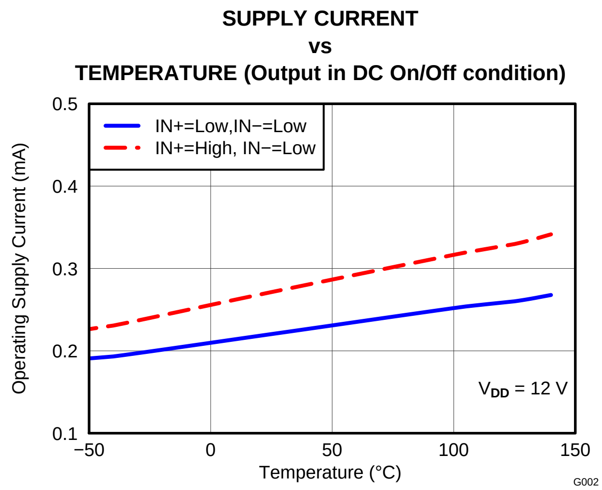


Figure 7.

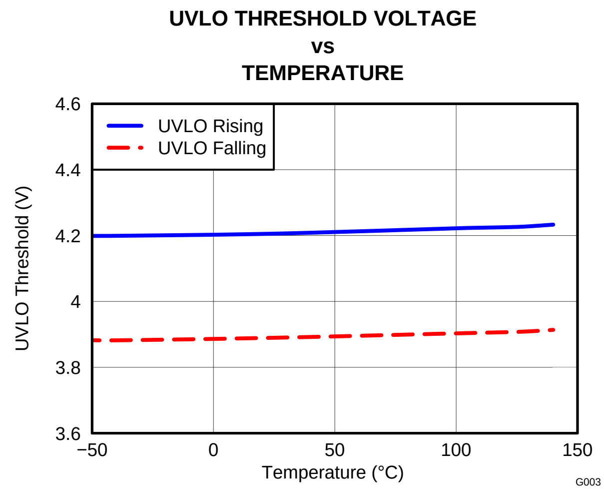


Figure 8.

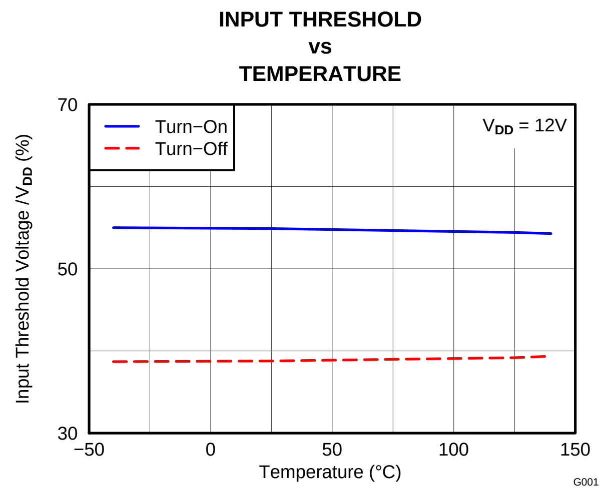


Figure 9.

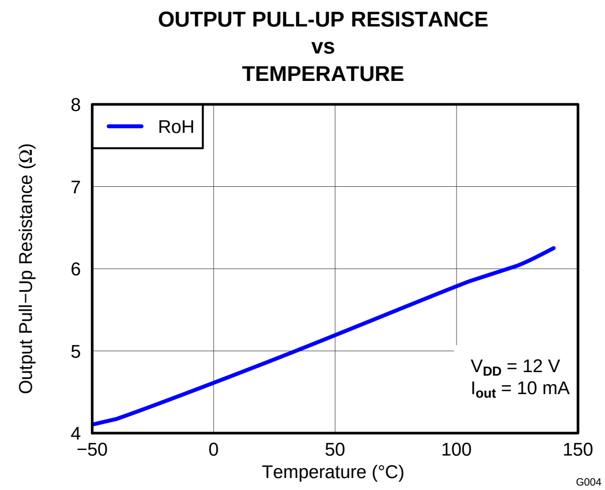


Figure 10.

TYPICAL CHARACTERISTICS (continued)

OUTPUT PULL-DOWN RESISTANCE vs TEMPERATURE

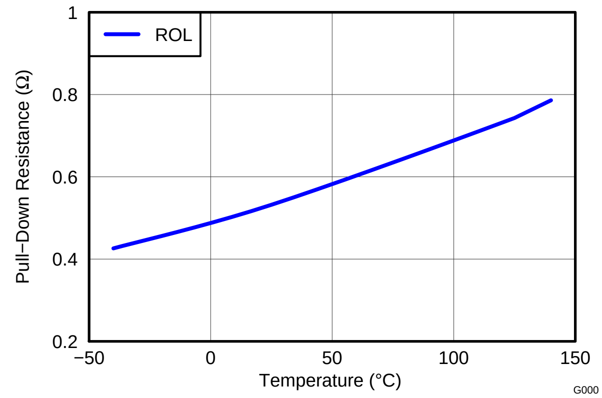


Figure 11.

RISE TIME vs TEMPERATURE

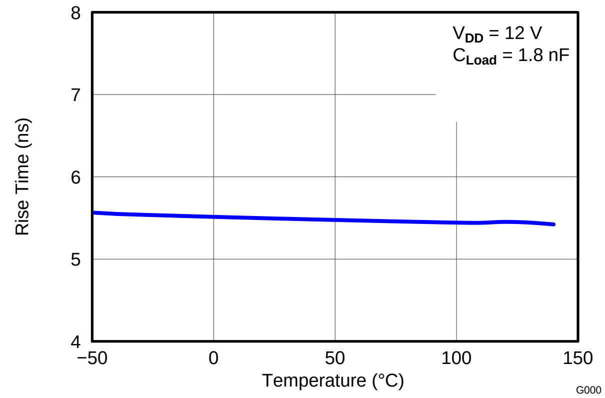


Figure 12.

FALL TIME vs TEMPERATURE

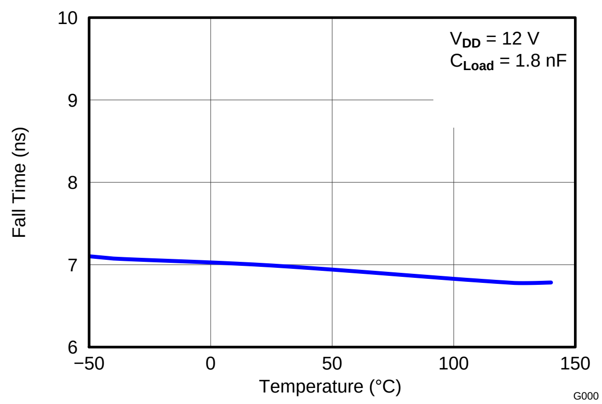


Figure 13.

INPUT TO OUTPUT PROPAGATION DELAY vs TEMPERATURE

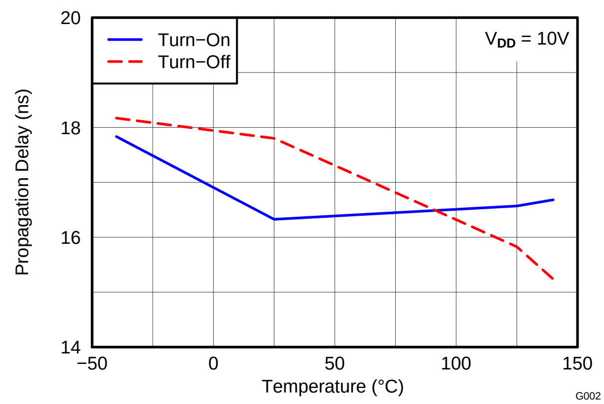


Figure 14.

OPERATING SUPPLY CURRENT vs FREQUENCY

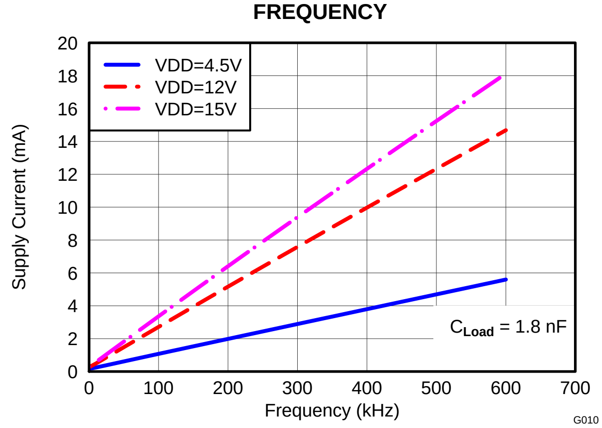


Figure 15.

RISE TIME vs SUPPLY VOLTAGE

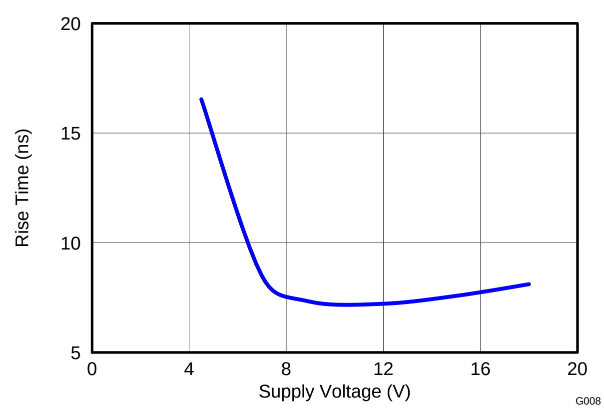


Figure 16.

TYPICAL CHARACTERISTICS (continued)

FALL TIME vs SUPPLY VOLTAGE

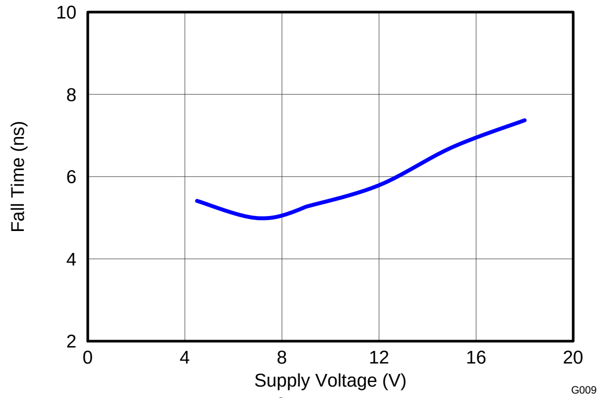


Figure 17.

APPLICATION INFORMATION

Introduction

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers and the gates of the power semiconductor devices. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself. Finally, emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

UCC2751x Product Family

The UCC2751x family of gate driver products (Table 3) represent Texas Instruments' latest generation of single-channel, low-side high-speed gate driver devices featuring high-source/sink current capability, industry best-in-class switching characteristics and a host of other features (Table 4) all of which combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

Table 3. UCC2751x Product Family Summary

PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE/SINK)	INPUT THRESHOLD LOGIC
UCC27511DBV (1)	SOT-23, 6 pin	4-A/8-A (Asymmetrical Drive)	CMOS/TTL-Compatible (low voltage, independent of VDD bias voltage)
UCC27512DRS (1)	3 mm x 3 mm WSON, 6 pin		
UCC27516DRS (1)	3 mm x 3 mm WSON, 6 pin	4-A/4-A (Symmetrical Drive)	
UCC27517DBV (1)	SOT-23, 5 pin		
UCC27518DBV	SOT-23, 5 pin		CMOS (follows VDD bias voltage)
UCC27519DBV	SOT-23, 5 pin		

(1) Visit www.ti.com for the latest product datasheet.

Table 4. UCC2751x Family of Features and Benefits

FEATURE	BENEFIT
High Source/Sink Current Capability 4 A/8 A (Asymmetrical) – UCC27511/2 4 A/4 A (Symmetrical) – UCC27516/7	High current capability offers flexibility in employing UCC2751x family of devices to drive a variety of power switching devices at varying speeds
Best-in-class 13-ns (typ) Propagation delay	Extremely low pulse transmission distortion
Expanded VDD Operating range of 4.5 V to 18 V	Flexibility in system design Low VDD operation ensures compatibility with emerging wide band-gap power devices such as GaN
Expanded Operating Temperature range of -40°C to 140°C (See Electrical Characteristics table)	
VDD UVLO Protection	Outputs are held low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down
Outputs held low when input pins (INx) in floating condition	Safety feature, especially useful in passing abnormal condition tests during safety certification
Ability of input pins (and enable pin in UCC27518/9) to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
Split output structure in UCC27511 (OUTH, OUTL)	Allows independent optimization of turn-on and turn-off speeds
Strong sink current (8 A) and low pull-down impedance (0.375 Ω) in UCC27511/2	High immunity to C x dV/dt Miller turn-on events
CMOS/TTL compatible input threshold logic with wide hysteresis in UCC27511/2/6/7	Enhanced noise immunity, while retaining compatibility with microcontroller logic level input signals (3.3 V, 5 V) optimized for digital power
CMOS input threshold logic in UCC27518/9 (VIN_H – 70% VDD, VIN_L – 30% VDD)	Well suited for slow input voltage signals, with flexibility to program delay circuits (RCD)

Typical Application Diagram

Typical application diagram of UCC27518 and UCC27519 devices is shown below.

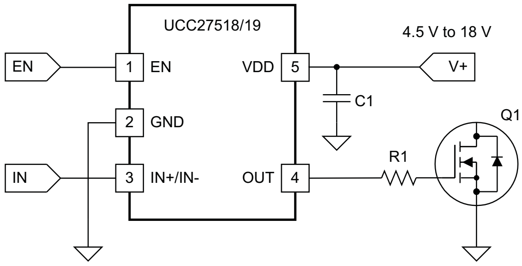


Figure 18. Typical Application Diagram

VDD and Undervoltage Lockout

The UCC2751x devices have internal Under Voltage LockOut (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition (i.e. when V_{DD} voltage less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide bandgap power semiconductor devices.

For example, at power up, the UCC2751x driver output remains LOW until the V_{DD} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. In the non-inverting device (PWM signal applied to IN+ pin) shown below, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting device (PWM signal applied to IN- pin) shown below the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input.

Since the driver draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-μF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate driver. In addition, a larger capacitor (such as 1 μF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

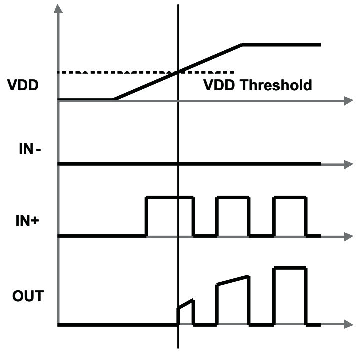


Figure 19. Power-Up (non-inverting drive)

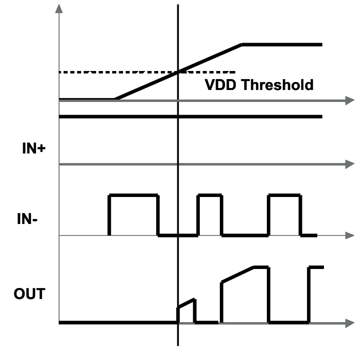


Figure 20. Power-Up (inverting drive)

Operating Supply Current

The UCC27518 and UCC27519 features very low quiescent I_{DD} currents. The typical operating supply current in Under Voltage LockOut (UVLO) state and fully-on state (under static and switching conditions) are summarized in Figure 5, Figure 6 and Figure 7. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, refer Figure 7) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current due to switching and finally any current related to pull-up resistors on the unused input pin. For example when the inverting input pin is pulled low additional current is drawn from VDD supply through the pull-up resistors (refer to DEVICE INFORMATION for the device Block Diagram). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the IDD current as a function of switching frequency at different VDD bias voltages under 1.8-nF switching load is provided in Figure 15. The strikingly linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

Input Stage

The input pins of UCC27518 and UCC27519 are based on CMOS input logic where the threshold voltage level is a function of the bias voltage applied on the VDD pin. Typically, the Input High Threshold (V_INH) is 55% VDD and Input Low Threshold (VIN_L) is 39% VDD. Hysteresis (typically 19% VDD) available on the input threshold offers noise immunity. With high VDD voltages resulting in wide hysteresis, slow dV/dt input signals are acceptable in the INx pins and RC circuits can be inserted between the input PWM signal and the INx pins of UCC27518/9, to program a delay between the input signal and output transition.

Enable Function

The Enable pin is based on a non-inverting configuration (active high operation). When EN pin is driven high the output is enabled and when EN pin is driven low the output is disabled. Unlike input pin, the enable pin threshold is based on a TTL/CMOS compatible input threshold logic that does not vary with the supply voltage. Typically, the Enable High Threshold (V_ENH) is 2.1 V and Enable Low Threshold (VEN_L) is 1.25 V. Thus the EN pin can be effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The EN pin is internally pulled up to VDD using pull-up resistor as a result of which the output of the device is enabled in the default state. Hence the EN pin can be left floating or Not Connected (N/C) for standard operation, when enable feature is not needed. Essentially, this allows the UCC27518/19 devices to be pin-to-pin compatible with TI's previous generation drivers TPS2828/9 respectively, where pins #1 is N/C pin.

Output Stage

The UCC27518 and UCC27519 are capable of delivering 4-A source, 4-A sink (symmetrical drive) at VDD = 12 V. The output stage of the UCC27518 and UCC27519 devices are illustrated in Figure 21. The UCC27518 and UCC27519 devices features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pull-up structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device is able to deliver a brief boost in the peak-sourcing current enabling fast turn on.

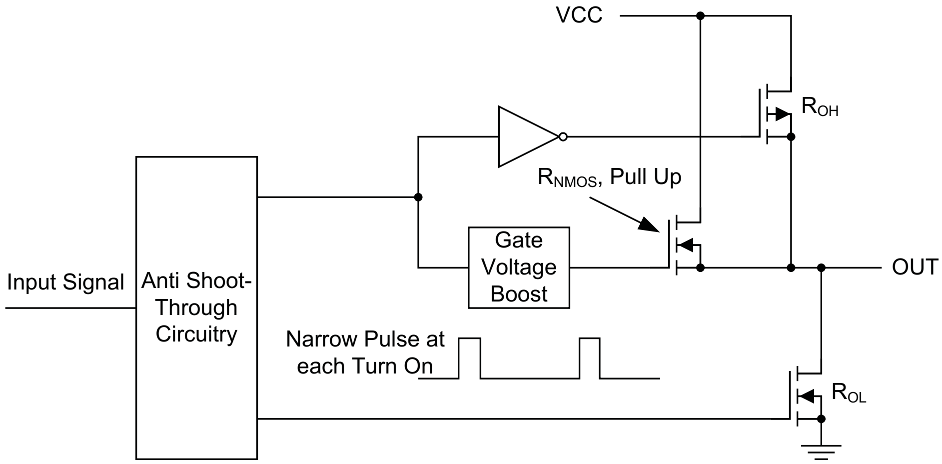


Figure 21. UCC2751x Gate Driver Output Structure

The R_{OH} parameter (see ELECTRICAL CHARACTERISTICS) is a DC measurement and it is representative of the on-resistance of the P-Channel device only, since the N-Channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pull-up stage is much lower than what is represented by R_{OH} parameter. The pull-down structure is composed of a N-Channel MOSFET only. The R_{OL} parameter (see ELECTRICAL CHARACTERISTICS), which is also a DC measurement, is representative of true impedance of the pull-down stage in the device. In UCC27518 and UCC27519, the effective resistance of the hybrid pull-up structure is approximately 1.4 x R_{OL}.

The driver output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \tag{1}$$

The DC portion of the power dissipation is P_{DC} = I_Q x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections etc and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through etc). The UCC27518 and UCC27519 features very low quiescent currents (less than 1 mA, refer Figure 7) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible.

The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out).
- Switching frequency.
- Use of external gate resistors.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{2}$$

Where C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver.

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} \tag{3}$$

where f_{SW} is the switching frequency.

The switching load presented by a power MOSFET/IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equation, Q_G = C_{LOAD} x V_{DD}, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \tag{4}$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = Q_G \times V_{DD} \times f_{SW} \times \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right) \tag{5}$$

where R_{OFF} = R_{OL} and R_{ON} (effective resistance of pull-up structure) = 1.4 x R_{OL}.

Low Propagation Delays

The UCC27518 and UCC27519 driver device features best-in-class input-to-output propagation delay of 17 ns (typ) at VDD = 12 V. This promises the lowest level of pulse transmission distortion available from industry standard gate driver devices for high-frequency switching applications. As seen in Figure 14, there is very little variation of the propagation delay with temperature and supply voltage as well, offering typically less than 20-ns propagation delays across the entire range of application conditions.

Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the Thermal Information section of the datasheet. For detailed information regarding the thermal information table, please refer to the Application Note from Texas Instruments entitled *IC Package Thermal Metrics* (Texas Instruments Literature Number SPRA953A).

PCB Layout

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC27518 and UCC27519 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak-current capability is even higher (4-A/4-A peak current is at VDD = 12 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turnon of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances – during turn-on and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCC27518DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27518DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27519DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27519DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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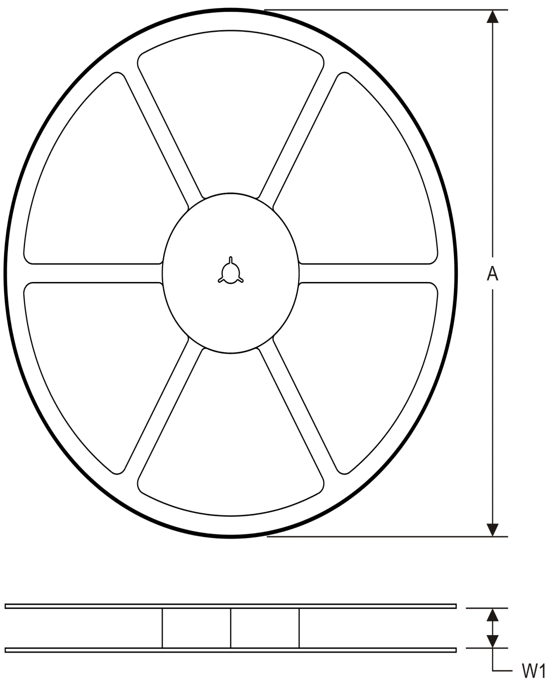
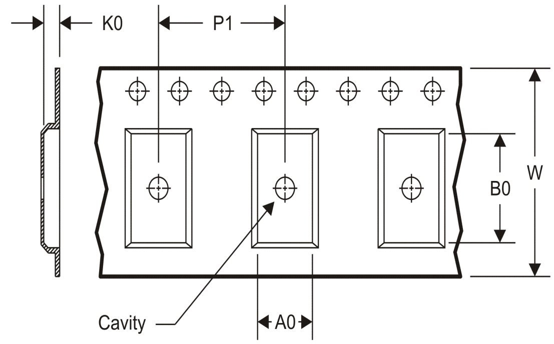
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



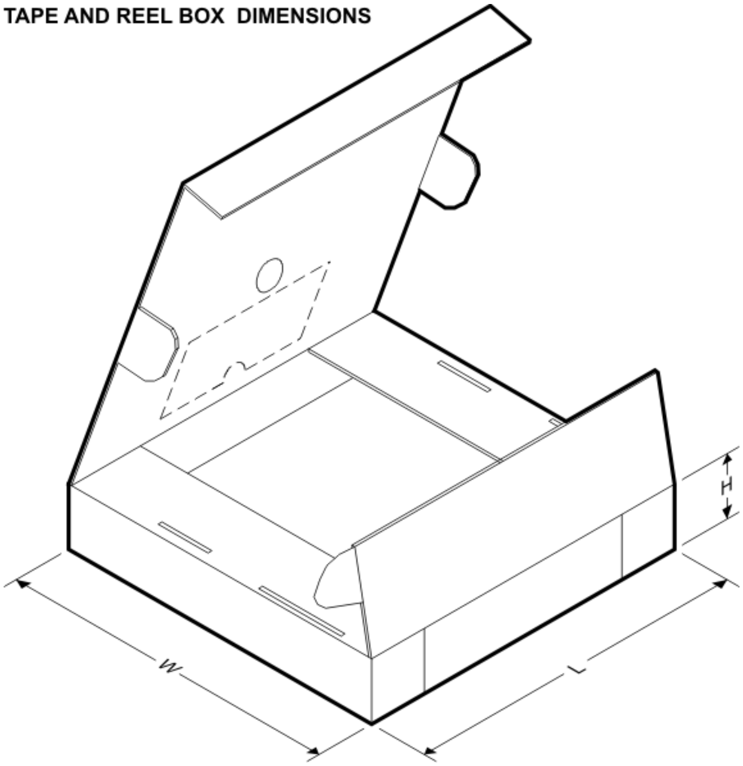
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27518DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27518DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27519DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27519DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

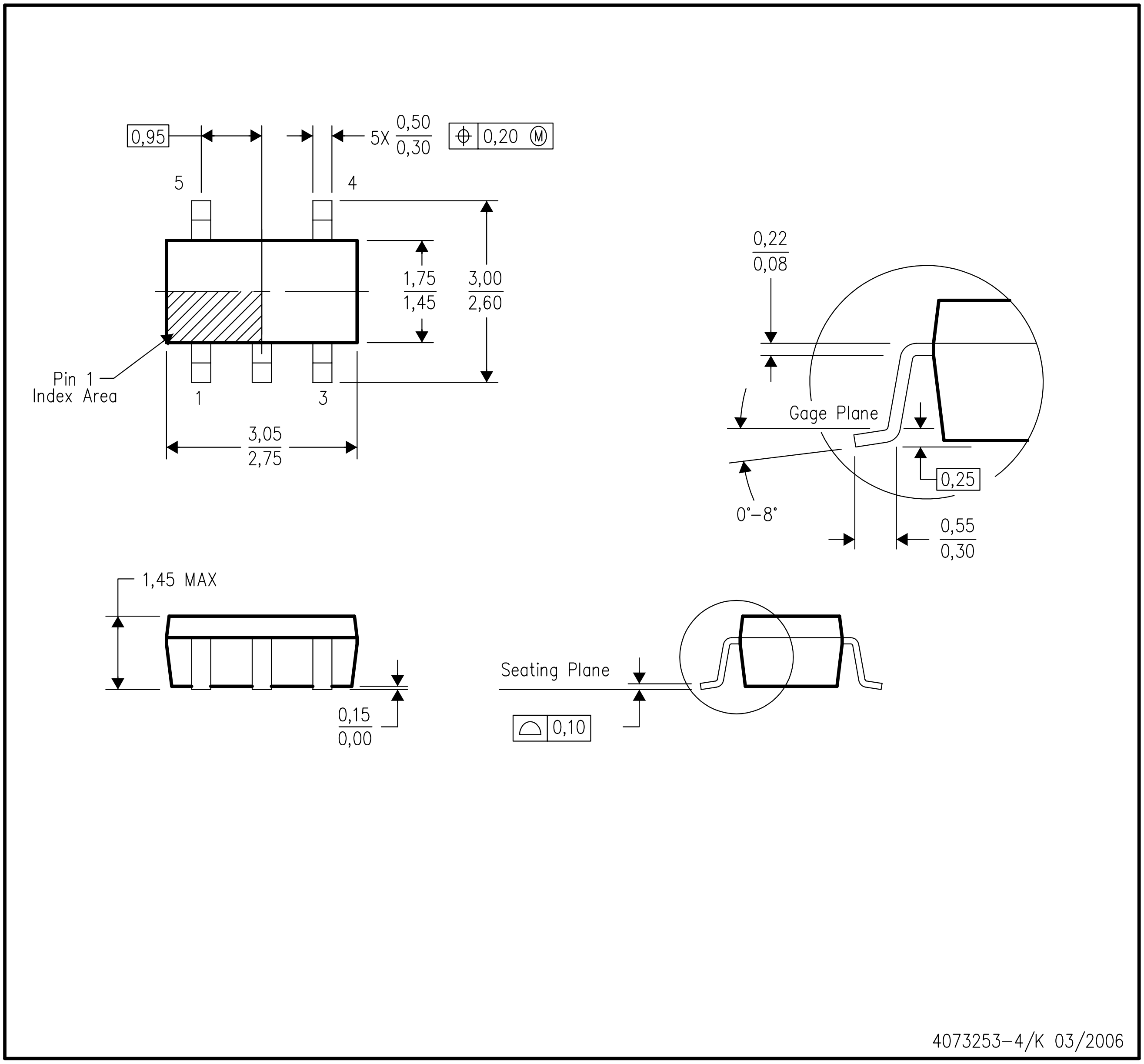
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

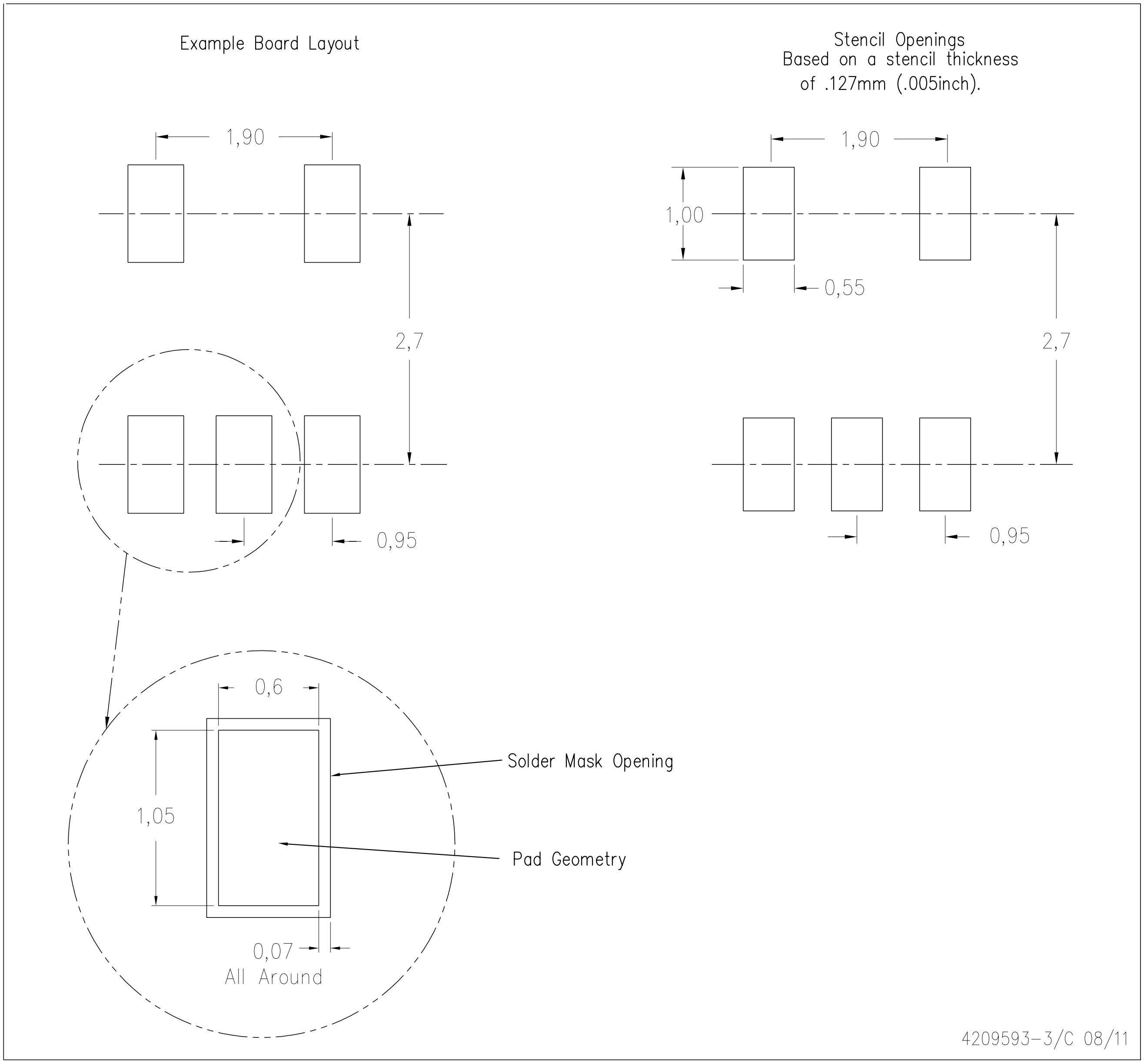
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27518DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
UCC27518DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
UCC27519DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
UCC27519DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.