

SN5410, SN54LS10, SN54S10, SN7410, SN74LS10, SN74S10 TRIPLE 3-INPUT POSITIVE-NAND GATES

SDLS035A – DECEMBER 1983 – REVISED APRIL 2003

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

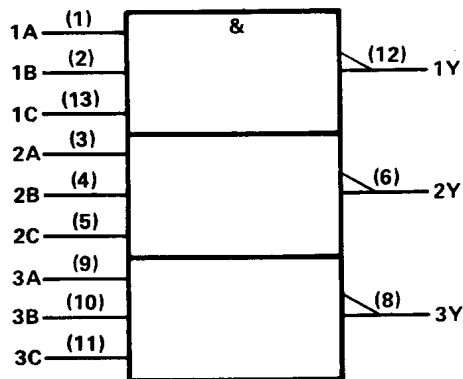
These devices contain three independent 3-input NAND gates.

The SN5410, SN54LS10, and SN54S10 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7410, SN74LS10, and SN74S10 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

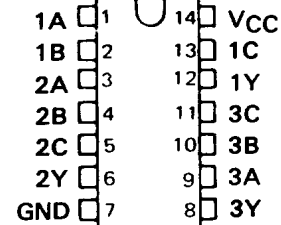
Pin numbers shown are for D, J, and N packages.

positive logic

$$Y = \overline{A \cdot B \cdot C} \text{ or } Y = \overline{A} + \overline{B} + \overline{C}$$

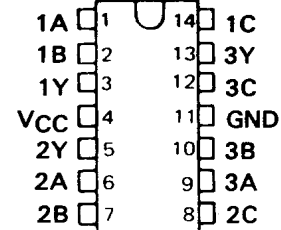
SN5410 . . . J PACKAGE
SN54LS10, SN54S10 . . . J OR W PACKAGE
SN7410 . . . N PACKAGE
SN74LS10, SN74S10 . . . D OR N PACKAGE

(TOP VIEW)



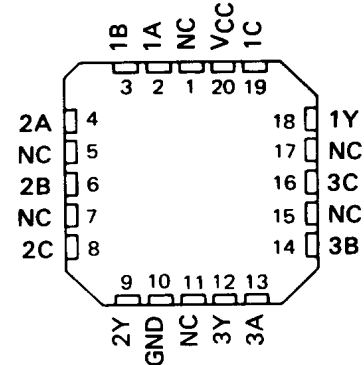
SN5410 . . . W PACKAGE

(TOP VIEW)



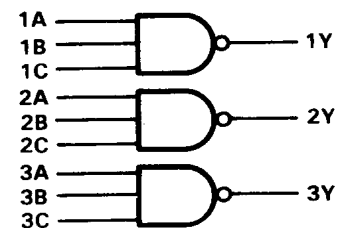
SN54LS10, SN54S10 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

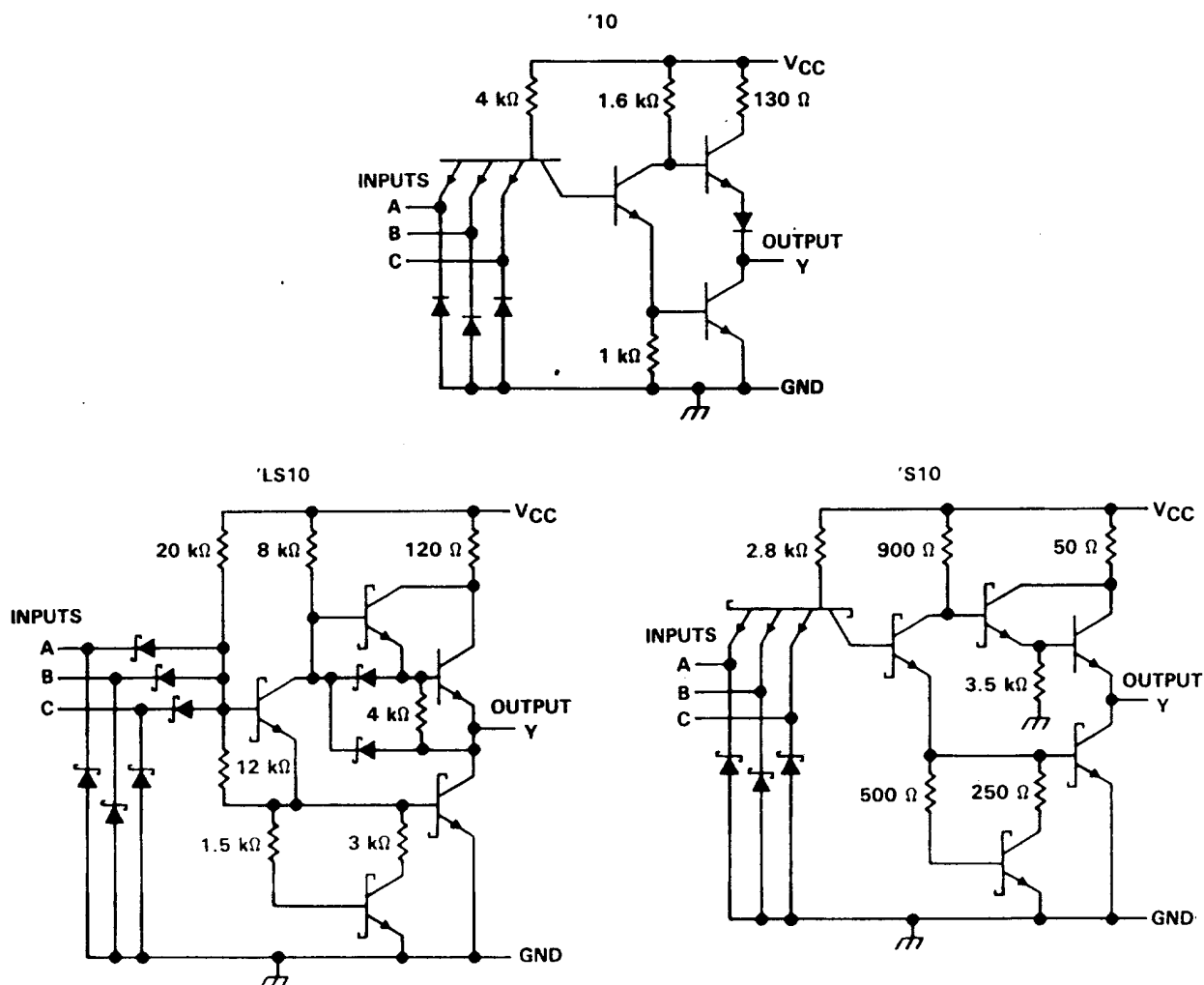
logic diagram (positive logic)



SN5410, SN54LS10, SN54S10, SN7410, SN74LS10, SN74S10 TRIPLE 3-INPUT POSITIVE-NAND GATES

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schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '10, 'S10	5.5 V
'LS10	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



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SN5410, SN7410, TRIPLE 3-INPUT POSITIVE-NAND GATES

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recommended operating conditions

	SN5410			SN7410			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-0.4			-0.4	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5410			SN7410			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}$, $V_I = 0 \text{ V}$		3	6		3	6	mA
I_{CCL}	$V_{CC} = \text{MAX}$, $V_I = 4.5 \text{ V}$		9	16.5		9	16.5	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B or C	Y	$R_L = 400 \Omega$, $C_L = 15 \text{ pF}$		11	22	ns
t_{PHL}					7	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN54LS10, SN74LS10, TRIPLE 3-INPUT POSITIVE-NAND GATES

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recommended operating conditions

	SN54LS10			SN74LS10			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			– 0.4			– 0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS10			SN74LS10			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			– 1.5			– 1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4			0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$					0.25	0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			– 0.4			– 0.4	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	– 20		– 100	– 20		– 100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		0.6	1.2		0.6	1.2	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		1.8	3.3		1.8	3.3	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B or C	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		9	15	ns
t_{PHL}					10	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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SN54S10, SN74S10, TRIPLE 3-INPUT POSITIVE-NAND GATES

SDLS035 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

	SN54S10			SN74S10			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			– 1			– 1	mA
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S10			SN74S10			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = –18 mA			–1.2			–1.2	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = –1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50			50	µA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			–2			–2	mA
I _{OS} §	V _{CC} = MAX	–40		–100	–40		–100	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		7.5	12		7.5	12	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		15	27		15	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A, B or C	Y	R _L = 280 Ω, C _L = 15 pF		3	4.5	ns
t _{PHL}					3	5	ns
t _{PLH}			R _L = 280 Ω, C _L = 50 pF		4.5		ns
t _{PHL}					5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
JM38510/00103BCA	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
JM38510/00103BDA	OBSOLETE	CFP	W	14		None	Call TI	Call TI
JM38510/07005BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/07005BDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
JM38510/30005B2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
JM38510/30005BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/30005BDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
JM38510/30005SCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/30005SDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SN5410J	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
SN54LS10J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN54S10J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN7410N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN7410N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74LS10D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS10DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS10N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS10N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74LS10NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74S10D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74S10N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S10N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74S10NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ5410J	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
SNJ5410W	OBSOLETE	CFP	W	14		None	Call TI	Call TI
SNJ5410WA	OBSOLETE	CFP	WA	14		None	Call TI	Call TI
SNJ54LS10FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54LS10J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ54LS10W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SNJ54S10FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54S10J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ54S10W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/F 07/2004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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