

2-BIT UNIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR

Check for Samples: [SN74AVC2T244](#)

FEATURES

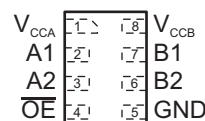
- Wide Operating V_{CC} Range of 0.9 V to 3.6 V
- Low Static-Power Consumption, 6- μ A Max I_{CC}
- Output Enable Feature Allows User to Disable Outputs to Reduce Power Consumption
- ± 24 -mA Output Drive at 3.0 V
- I_{off} Supports Partial Power-Down-Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input
- Maximum Data Rates
 - 380 Mbps (1.8-V to 3.3-V Translation)
 - 200 Mbps (<1.8-V to 3.3-V Translation)
 - 200 Mbps (Translate to 2.5 V or 1.8 V)
 - 150 Mbps (Translate to 1.5 V)
 - 100 Mbps (Translate to 1.2 V)

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 5000-V Human-Body Model (A114-A)

APPLICATIONS

- Handset, Smartphone, Tablet, Server

DQE/DQM PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 2-bit unidirectional translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 0.9 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 0.9 V to 3.6 V. This allows for low-voltage translation between 0.9-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.6-V voltage nodes. For the SN74AVC2T244, when the output-enable ($\overline{OE}$) input is high, all outputs are placed in the high-impedance state. The SN74AVC2T244 is designed so that the $\overline{OE}$ input circuit is referenced to V_{CCA} . This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	DQE – MicroQFN	SN74AVC2T244DQER	VA
	DQM – MicroQFN	SN74AVC2T244DQMR	VAH

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

PIN DESCRIPTION

PIN	FUNCTION
VCCA	Input Port DC Power Supply
VCCB	Output Port DC Power Supply
GND	Ground
An	Input Port
Bn	Output Port
OE	Output Enable

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Voltage	DC Supply voltage, V_{CCA} , V_{CCB}		–0.5	4.6	V
	DC Input voltage, V_I	A_n	–0.5	4.6	V
	Control Input, V_C	$\overline{OE}$	–0.5	4.6	V
	DC Output voltage, V_O , $V_{CCA} = V_{CCB} = 0$	(Power Down) B_n	–0.5	4.6	V
		(Active Mode) B_n	–0.5	4.6	
		3-State Mode B_n	–0.5	4.6	
	DC Input Diode current, I_{IK}	$V_I < GND$		–20	mA
	DC Output Diode current, I_{OK}	$V_O < GND$		–50	mA
	DC Output Source/Sink current, I_O			±50	mA
	DC Supply current per supply pin, I_{CCA} , I_{CCB}			±100	mA
I_{GND}	DC Ground current per ground pin			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CCA} , V_{CCB}	Positive DC Supply voltage		0.9	3.6	V
V_I	Bus input voltage		GND	3.6	V
V_I	Input voltage		GND	3.6	V
V_C	Control input	$\overline{OE}$	GND	3.6	V
V_O	Bus output voltage	(Power Down Mode) B_n	GND	3.6	V
		(Active Mode) B_n	GND	V_{CCB}	V
		3-State Mode B_n	GND	3.6	V
T_A	Operating free-air temperature		–40	85	°C
$\Delta t/\Delta v$	Input transition rise or fall rate V_I from 30% to 70% of V_{CC} ; $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		0	10	nS

ELECTRICAL CHARACTERISTICS^{(1) (2)}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA} (V)	V _{CCB} (V)	–40°C to 85°C		UNIT
					MIN	MAX	
V _{IH}	Input HIGH Voltage (An, $\overline{OE}$)		2.7 – 3.6	0.9 – 3.6	2.0	–	V
			2.3 – 2.7		1.6	–	
			1.4 – 2.3		0.65 × V _{CCA}	–	
			0.9 – 1.4		0.9 × V _{CCA}	–	
V _{IL}	Input LOW voltage (An, $\overline{OE}$)		2.7 – 3.6	0.9 – 3.6	–	0.8	V
			2.3 – 2.7		–	0.7	
			1.4 – 2.3		–	0.35 × V _{CCA}	
			0.9 – 1.5		–	0.1 × V _{CCA}	
V _{OH}	Output HIGH voltage	I _{OH} = –100 µA; V _I = V _H	0.9 – 3.6	0.9 – 3.6	V _{CCB} – 0.2	–	V
		I _{OH} = –0.5 mA; V _I = V _H	0.9	0.9	0.75 × V _{CCB}	–	
		I _{OH} = –2 mA; V _I = V _H	1.4	1.4	1.05	–	
		I _{OH} = –6 mA; V _I = V _H	1.65	1.65	1.25	–	
			2.3	2.3	2.0	–	
		I _{OH} = –12 mA; V _I = V _H	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I _{OH} = –18 mA; V _I = V _H	2.3	2.3	1.7	–	
			3.0	3.0	2.4	–	
V _{OL}	Output LOW voltage	I _{OH} = –24 mA; V _I = V _H	3.0	3.0	2.2	–	V
		I _{OH} = 100 µA; V _I = V _H	0.9 – 3.6	0.9 – 3.6	–	0.2	
		I _{OH} = 0.5 mA; V _I = V _H	1.1	1.1	–	0.3	
		I _{OH} = 2 mA; V _I = V _H	1.4	1.4	–	0.35	
		I _{OH} = 6 mA; V _I = V _H	1.65	1.65	–	0.3	
			2.3	2.3	–	0.4	
		I _{OH} = 12 mA; V _I = V _H	2.7	2.7	–	0.4	
			2.3	2.3	–	0.6	
		I _{OH} = 18 mA; V _I = V _H	3.0	3.0	–	0.4	
I _I	Input Leakage Current	V _I = V _{CCA} or GND	0.9 – 3.6	0.9 – 3.6	–1.0	1.5	µA
			0	0.9 – 3.6	–1.0	1.3	
I _{OFF}	Power-Off Leakage Current	$\overline{OE}$ = 0V	0.9 – 3.6	0	–1.0	1.5	µA
			0	0.9 – 3.6	–1.0	1.5	
I _{CCA}	Quiescent Supply Current	V _I = V _{CCA} or GND; I _O = 0	0.9 – 3.6	0.9 – 3.6	–	3.0	µA
I _{CCB}	Quiescent Supply Current	V _I = V _{CCA} or GND; I _O = 0	0.9 – 3.6	0.9 – 3.6	–	3.0	µA
I _{CCA} + I _{CCB}	Quiescent Supply Current	V _I = V _{CCA} or GND; I _O = 0	0.9 – 3.6	0.9 – 3.6	–	6.0	µA
ΔI _{CCA}	Increase in I _{CC} per Input Voltage, Other inputs at V _{CCA} or GND	V _I = V _{CCA} – 0.3 V; V _I = V _{CCA} or GND	3.6	3.6	–	5.0	µA

(1) V_{CCO} is the V_{CC} associated with the output port.

(2) V_{CCI} is the V_{CC} associated with the input port.

ELECTRICAL CHARACTERISTICS^{(1) (2)} (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA} (V)	V _{CCB} (V)	–40°C to 85°C		UNIT
					MIN	MAX	
ΔI_{CCB}	Increase in I_{CC} per Input Voltage, Other inputs at V _{CCA} or GND	V _I = V _{CCA} – 0.3 V; V _I = V _{CCA} or GND	3.6	3.6	–	5.0	μA
I _{OZ}	I/O Tri-State Output Leakage Current	TA = 25°C, $\overline{OE}$ = 0 V	0.9 – 3.6	0.9 – 3.6	–1.0	1.0	μA

AC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	V _{CCA} (V)	V _{CCB} (V)	MIN	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation Delay, A _n to B _n	0.9 – 3.6	0.9 – 3.6		20	nS
		1.2 – 3.6	1.2 – 3.6		7	
		1.8 – 3.6	1.8 – 3.6		3.5	
t _{PZH} , t _{PZL}	Output Enable, $\overline{OE}$ to B _n	0.9 – 3.6	0.9 – 3.6		23	nS
		1.2 – 3.6	1.2 – 3.6		6.5	
		1.8 – 3.6	1.8 – 3.6		4.1	
t _{PHZ} , t _{PLZ}	Output Disable, $\overline{OE}$ to B _n	0.9 – 3.6	0.9 – 3.6		17	nS
		1.2 – 3.6	1.2 – 3.6		7	
		1.8 – 3.6	1.8 – 3.6		4.3	
t _{OSHL} , t _{OSLH}	Output to Output Skew, Time	0.9 – 3.6	0.9 – 3.6		0.15	nS
		1.2 – 3.6	1.2 – 3.6		0.15	
		1.8 – 3.6	1.8 – 3.6		0.15	

Table 1. CAPACITANCE⁽¹⁾

Symbol	Parameter	Test Conditions	TYP ⁽²⁾	Unit
C _{IN}	Control Pin Input Capacitance	V _{CCA} = V _{CCB} = 3.3 V, V _I = 0 V or V _{CCA/B}	3.5	pF
C _{I/O}	I/O Pin Input capacitance	V _{CCA} = V _{CCB} = 3.3 V, V _I = 0 V or V _{CCA/B}	5.0	pF
C _{PD}	Power Dissipation Capacitance	V _{CCA} = V _{CCB} = 3.3 V, V _I = 0 V or V _{CCA/B} , f = 10 MHz	33	pF

- (1) C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: I_{CC(operating)} ≈ C_{PD} × V_{CC} × f_{IN} × N_{SW} where I_{CC} = I_{CCA} + I_{CCB} and N_{SW} = total number of outputs switching.
- (2) Typical values are at TA = +25°C.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AVC2T244DQER	ACTIVE	X2SON	DQE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVC2T244DQMR	ACTIVE	X2SON	DQM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

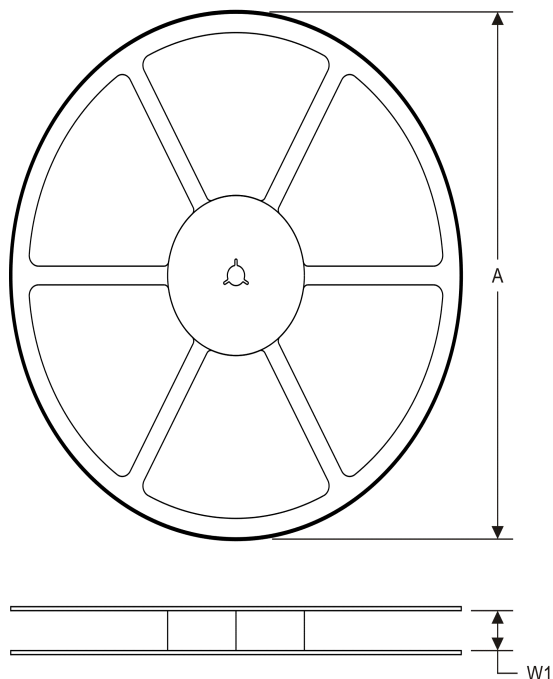
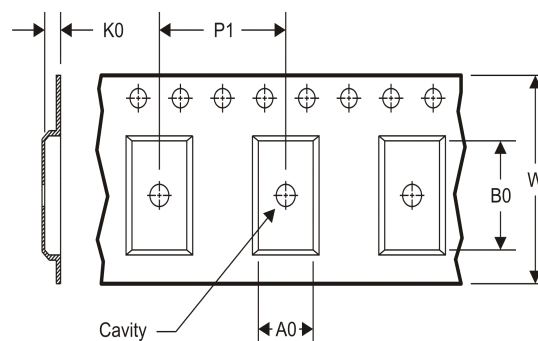
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


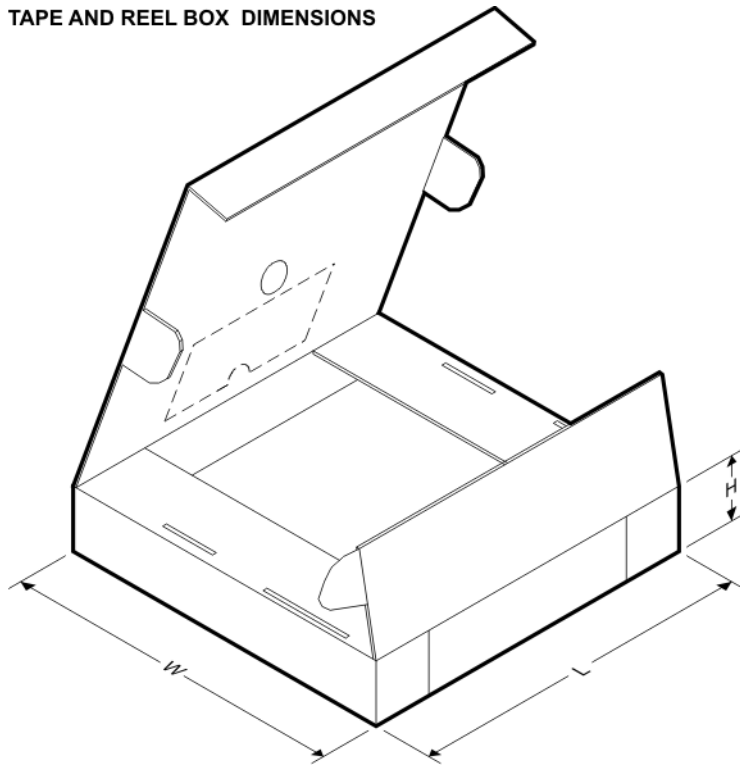
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC2T244DQER	X2SON	DQE	8	5000	180.0	8.4	1.17	1.67	0.73	4.0	8.0	Q1
SN74AVC2T244DQMR	X2SON	DQM	8	3000	180.0	8.4	1.57	2.21	0.59	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

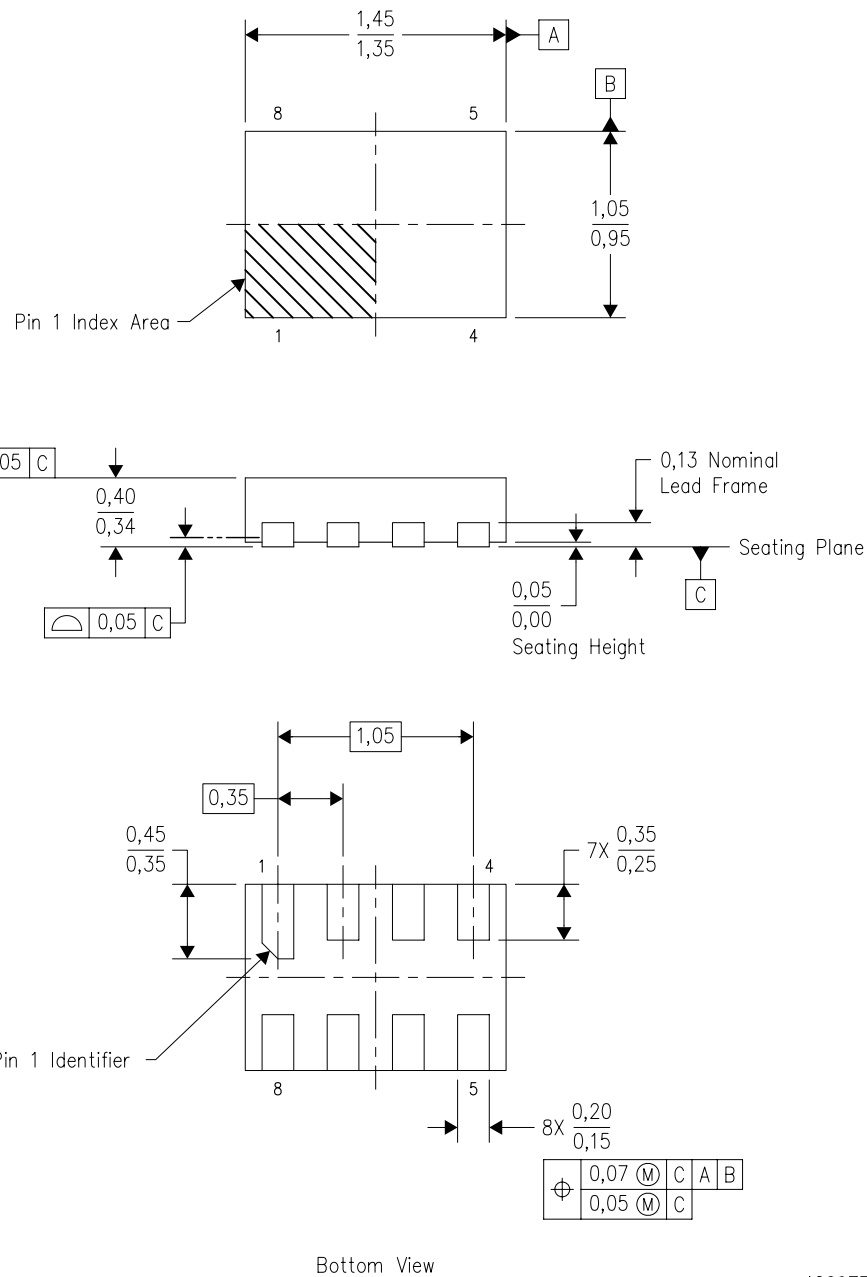


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC2T244DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AVC2T244DQMR	X2SON	DQM	8	3000	202.0	201.0	28.0

DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



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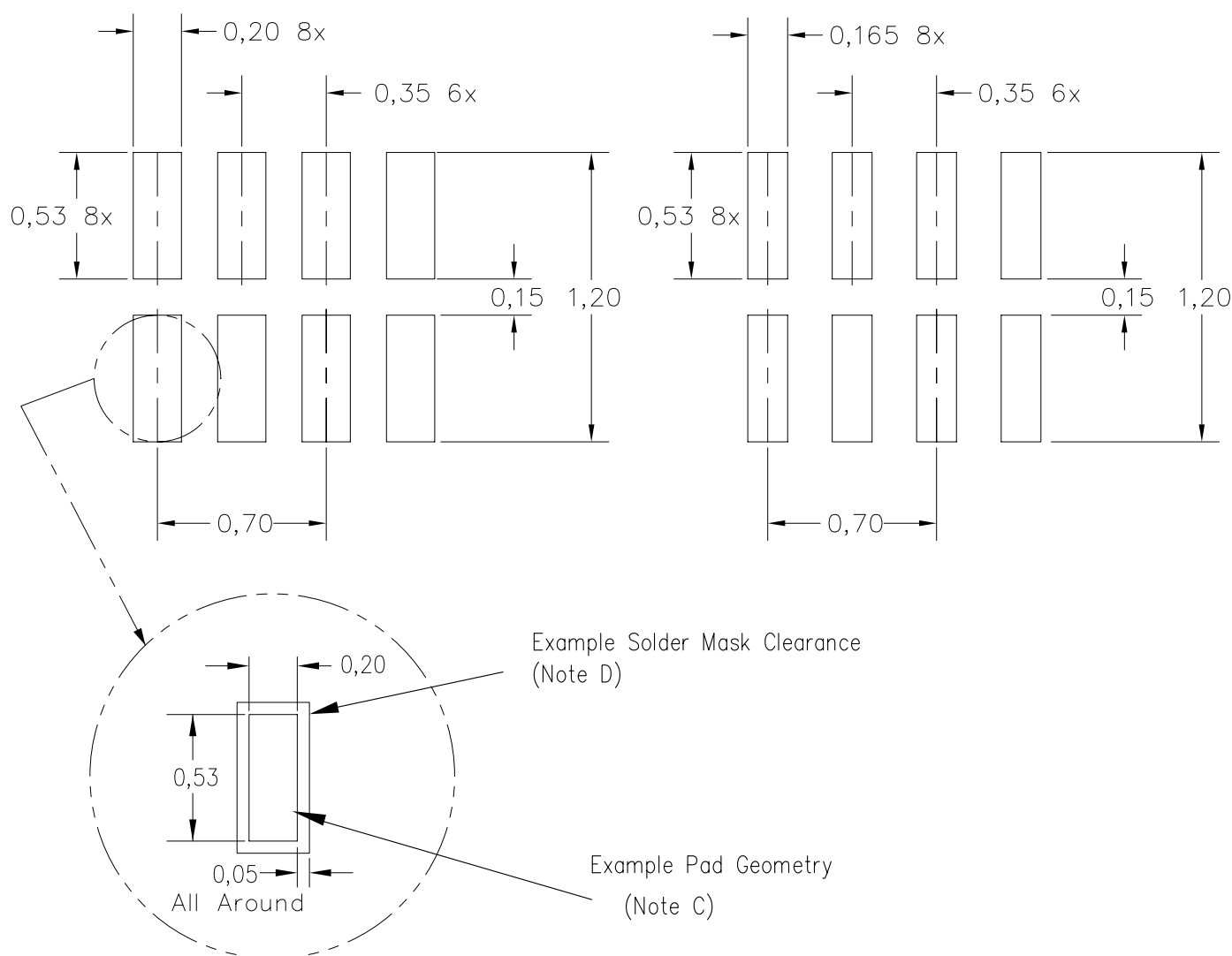
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - D. This package complies to JEDEC MO-287 variation X2EAF.

DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout

Example Stencil Design
(Note E)

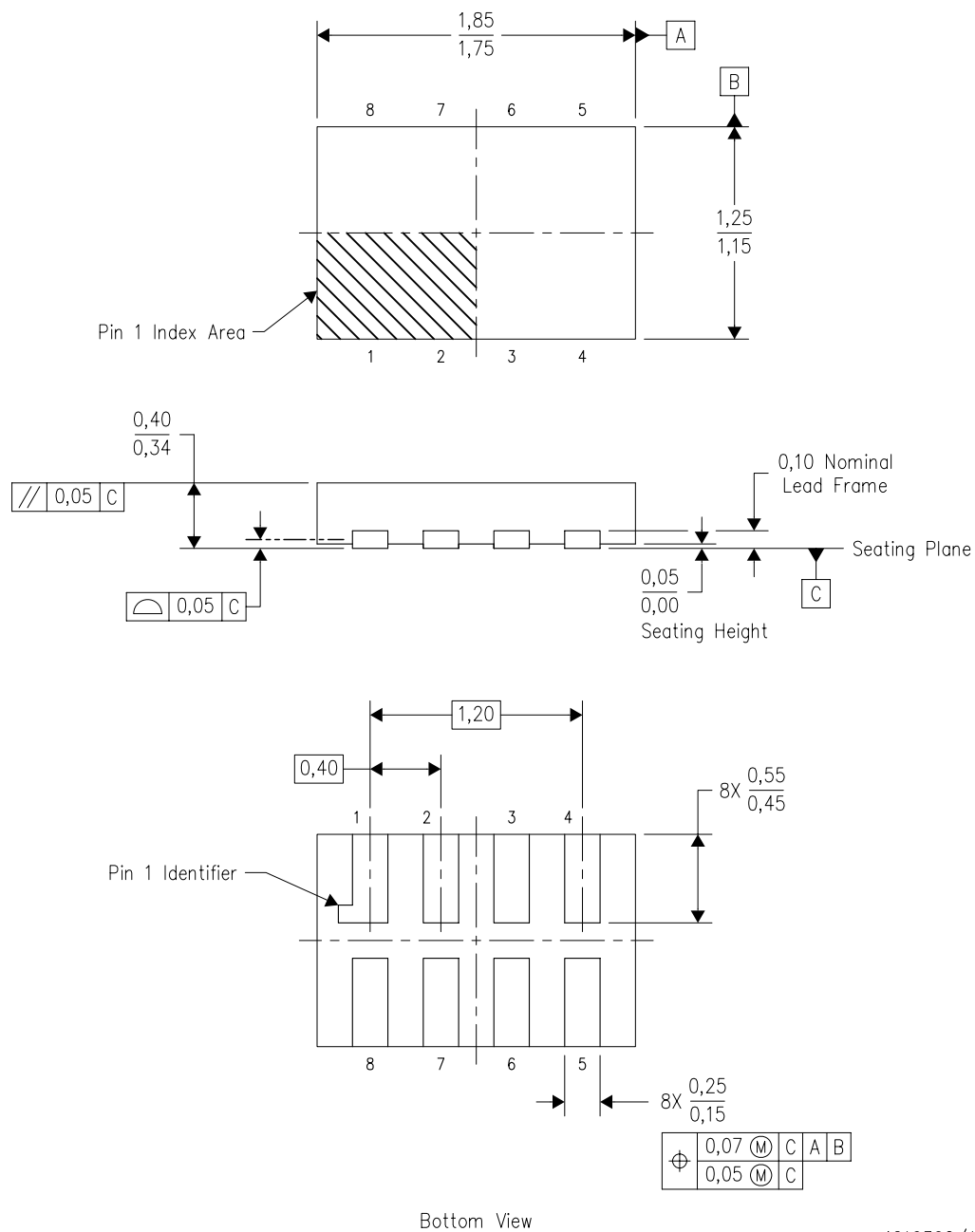


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- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 - Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Over-printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
 - Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 - Component placement force should be minimized to prevent excessive paste block deformation.

DQM (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4210302/A 06/2009

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.

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