Hysteretic PFET Buck Controller

Check for Samples: LM3485

FEATURES

- Easy to Use Control Methodology
- No Control Loop Compensation Required
- 4.5V to 35V Wide Input Range
- 1.242V to V_{IN} Adjustable Output Range
- High Efficiency 93%
- ±1.3% (±2% Over Temp) Internal Reference
- 100% Duty Cycle
- Maximum Operating Frequency > 1MHz
- Current Limit Protection
- VSSOP-8

APPLICATIONS

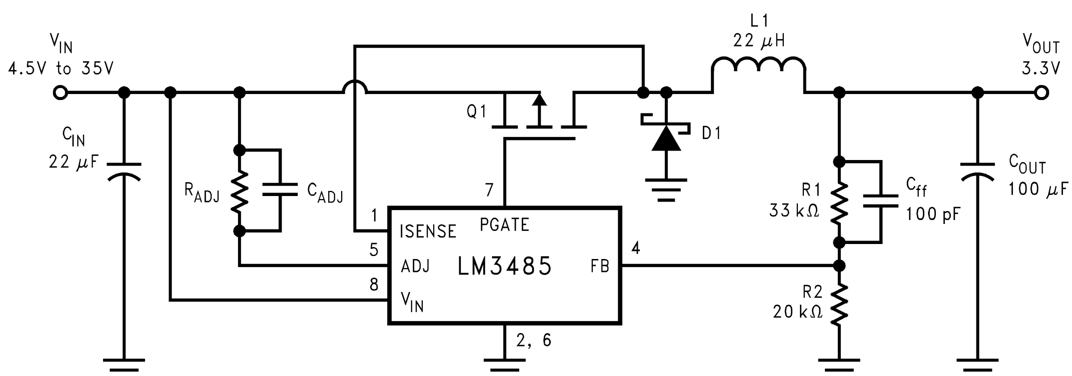
- Set-Top Box
- DSL or Cable Modem
- PC/IA
- Auto PC
- TFT Monitor
- Battery Powered Portable Applications
- Distributed Power Systems
- Always On Power

DESCRIPTION

The LM3485 is a high efficiency PFET switching regulator controller that can be used to quickly and easily develop a small, low cost, switching buck regulator for a wide range of applications. The hysteretic control architecture provides for simple design without any control loop stability concerns using a wide variety of external components. The PFET architecture also allows for low component count as well as ultra-low dropout, 100% duty cycle operation. Another benefit is high efficiency operation at light loads without an increase in output ripple.

Current limit protection is provided by measuring the voltage across the PFET's $R_{DS(ON)}$, thus eliminating the need for a sense resistor. The cycle-by-cycle current limit can be adjusted with a single resistor, ensuring safe operation over a range of output currents.

Typical Application Circuit



Connection Diagram

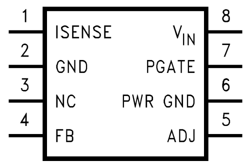


Figure 1. Top View
8-Lead Plastic VSSOP-8
Package Number DGK (S-PDSO-G8)

PIN DESCRIPTIONS

Pin Name	Pin No.	Description
ISENSE	1	The current sense input pin. This pin should be connected to Drain node of the external PFET.
GND	2	Signal ground.
NC	3	No connection.
FB	4	The feedback input. Connect the FB to a resistor voltage divider between the output and GND for an adjustable output voltage.
ADJ	5	Current limit threshold adjustment. It connects to an internal 5.5µA current source. A resistor is connected between this pin and the input Power Supply. The voltage across this resistor is compared with the V_{DS} of the external PFET to determine if an over-current condition has occurred.
PWR GND	6	Power ground.
PGATE	7	Gate Drive output for the external PFET. PGATE swings between V_{IN} and V_{IN}-5V.
VIN	8	Power supply input pin.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [(1)]

VIN Voltage		−0.3V to 36V
PGATE Voltage		−0.3V to 36V
FB Voltage		−0.3V to 5V
ISENSE Voltage		−1.0V to 36V
ADJ Voltage		−0.3V to 36V
Maximum Junction Temperature		150°C
Power Dissipation		417mW at T_A = 25°C
ESD Susceptibility	Human Body Model [(2)]	2kV
Lead Temperature	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Storage Temperature		−65°C to 150°C

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For specifications and test conditions, see the Electrical Characteristics.
(2) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

Operating Ratings [(1)]

Supply Voltage	4.5V to 35V
Operating Junction Temperature	−40°C to +125°C

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Specifications in Standard type face are for T_J = 25°C, and in **bold type face** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Unless otherwise specified, V_{IN} = 12V, V_{ISNS} = V_{IN} − 1V, and V_{ADJ} = V_{IN} − 1.1V. Datasheet min/max specification limits are specified by design, test, or statistical analysis.

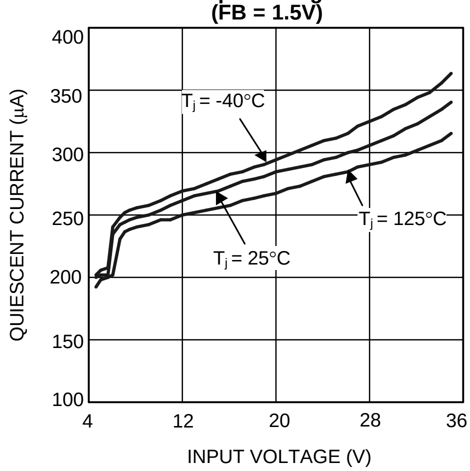
Symbol	Parameter	Test Conditions	Min (1)	Typ (2)	Max (1)	Unit
I_Q	Quiescent Current at ground pin	FB = 1.5V (Not Switching)		250	**400**	µA
V_{FB}	Feedback Voltage (3)		1.226 **1.217**	1.242	1.258 **1.267**	V
V_{HYST}	Comparator Hysteresis			10 **14**	15 **20**	mV
V_{CL} (4)	Current limit comparator trip voltage	R_{ADJ} = 20kΩ		110		mV
		R_{ADJ} = 160kΩ		880		
V_{CL_OFFSET}	Current limit comparator offset	V_{FB} = 1.5V	**−20**	0	**+20**	mV
I_{CL_ADJ}	Current limit ADJ current source	V_{FB} = 1.5V	**3.0**	5.5	**7.0**	µA
T_{CL}	Current limit one shot off time	V_{ADJ} = 11.5V V_{ISNS} = 11.0V V_{FB} = 1.0V	**6**	9	**14**	µs
R_{PGATE}	Driver resistance	Source I_{SOURCE} = 100mA		5.5		Ω
		Sink I_{Sink} = 100mA		8.5		
I_{PGATE}	Driver Output current	Source V_{IN} = 7V, P_{GATE} = 3.5V		0.44		A
		Sink V_{IN} = 7V, P_{GATE} = 3.5V		0.32		
I_{FB}	FB pin Bias Current (5)	V_{FB} = 1.0V		300	**750**	nA
T_{ONMIN_NOR}	Minimum on time in normal operation	V_{ISNS} = V_{ADJ}+0.1V C_{load} on OUT = 1000pF (6)		100		ns
T_{ONMIN_CL}	Minimum on time in current limit	V_{ISNS} = V_{ADJ}+0.1V V_{FB} = 1.0V C_{load} on OUT = 1000pF (6)		175		ns
$\%V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	4.5 ≤ V_{IN} ≤ 35V		0.010		%/V

(1) All limits are specified at room temperature (standard type face) and at **temperature extremes (bold type face)**. All room temperature limits are 100% tested. All limits at **temperature extremes** are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) The V_{FB} is the trip voltage at the FB pin when PGATE switches from high to low.
(4) $V_{CL} = I_{CL\_ADJ} * R_{ADJ}$
(5) Bias current flows out from the FB pin.
(6) A 1000pF capacitor is connected between V_{IN} and PGATE.

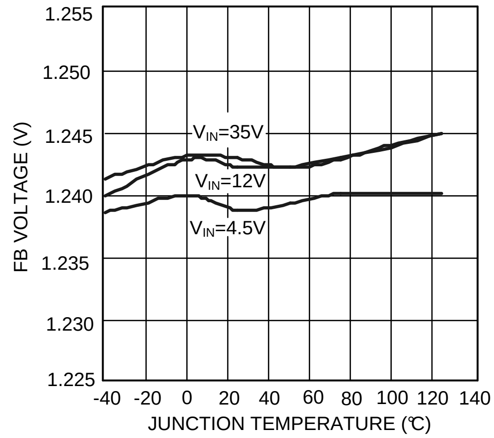
Typical Performance Characteristics

Unless otherwise specified, T_J = 25°C

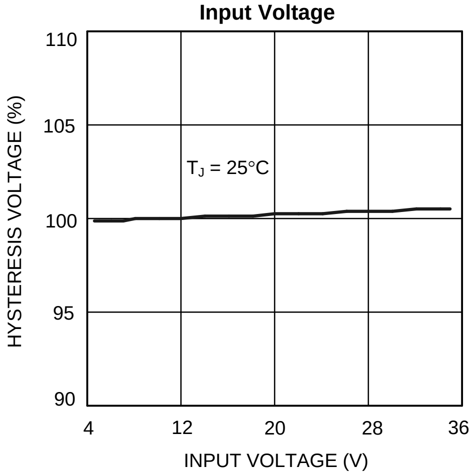
Quiescent Current vs Input Voltage (FB = 1.5V)



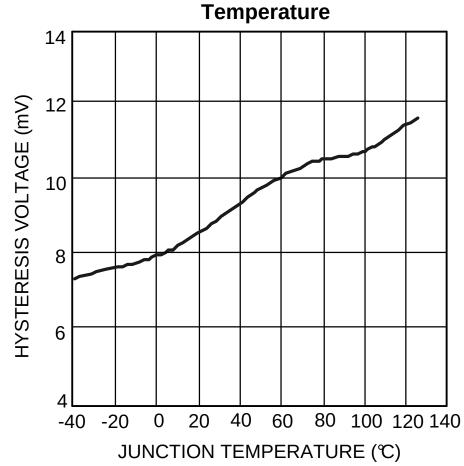
Feedback Voltage vs Temperature



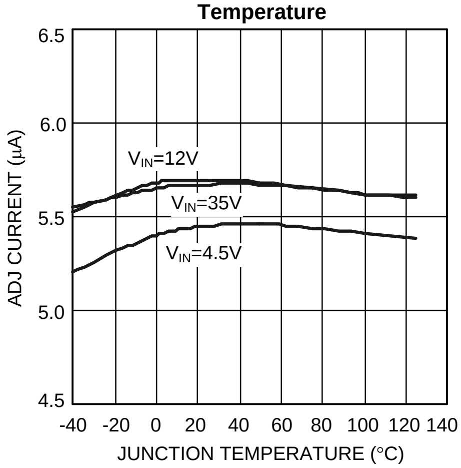
Hysteresis Voltage vs Input Voltage



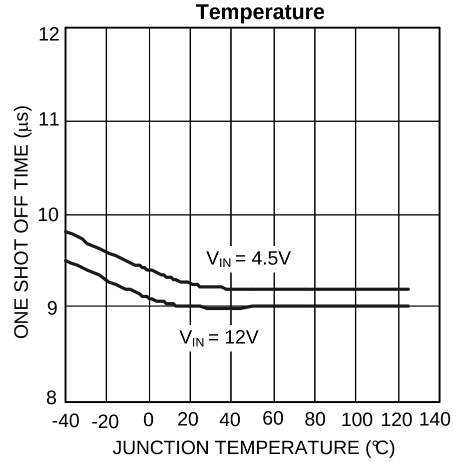
Hysteresis Voltage vs Temperature



Current Limit ADJ Current vs Temperature



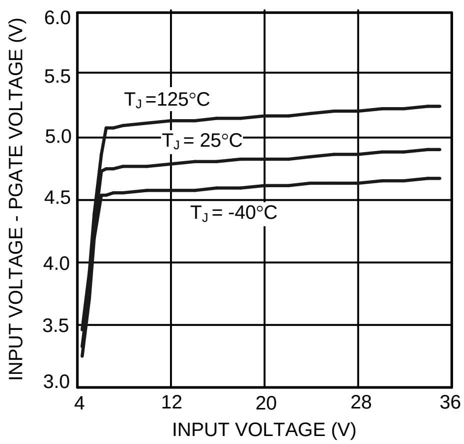
Current Limit One Shot OFF Time vs Temperature



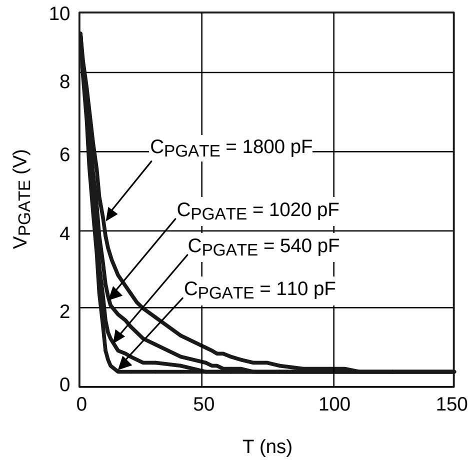
Typical Performance Characteristics (continued)

Unless otherwise specified, T_J = 25°C

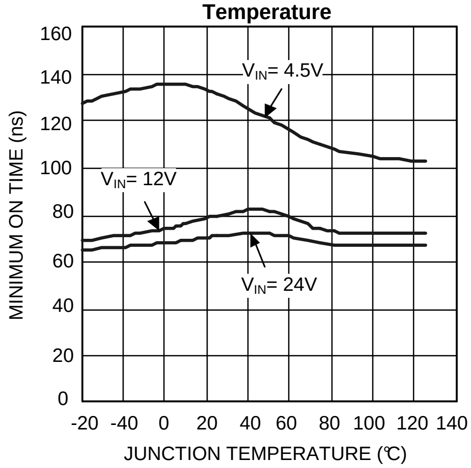
PGATE Voltage vs Input Voltage



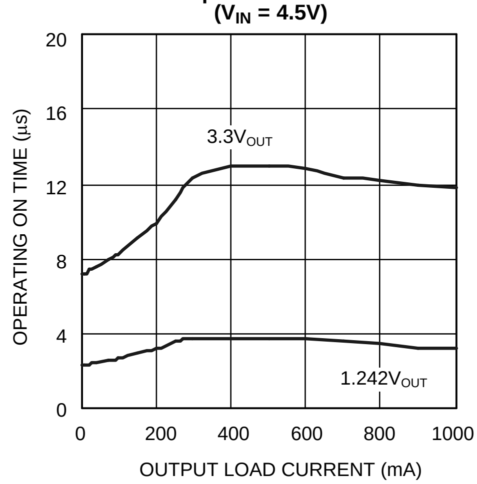
Typical V_{PGATE} vs Time V_{IN} = 9V



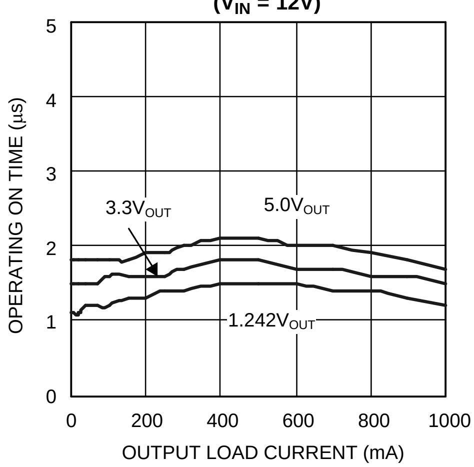
Minimum ON Time vs Temperature



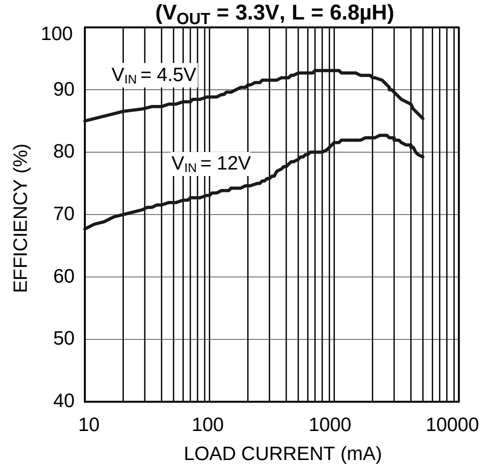
Operating ON Time vs Output Load Current (V_{IN} = 4.5V)



Operating ON Time vs Output Load Current (V_{IN} = 12V)



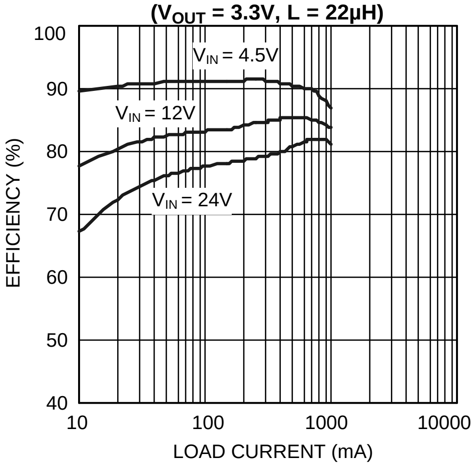
Efficiency vs Load Current (V_{OUT} = 3.3V, L = 6.8µH)



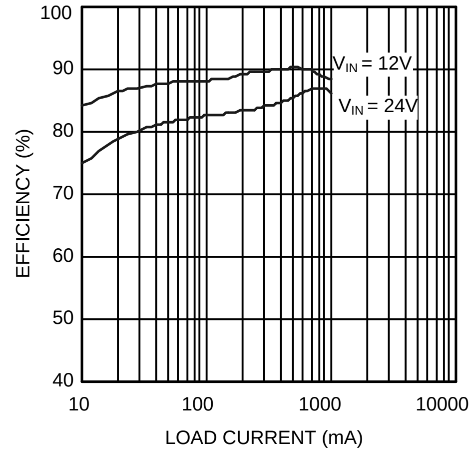
Typical Performance Characteristics (continued)

Unless otherwise specified, T_J = 25°C

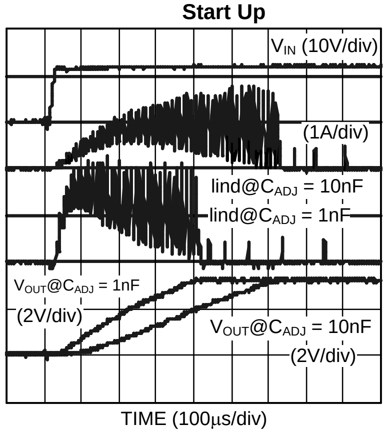
Efficiency vs Load Current (V_{OUT} = 3.3V, L = 22µH)



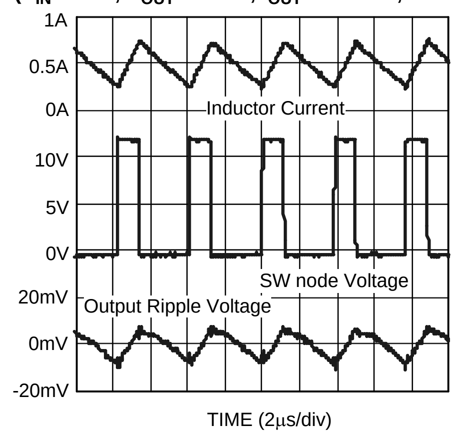
Efficiency vs Load Current (V_{OUT} = 5.0V, L = 22µH)



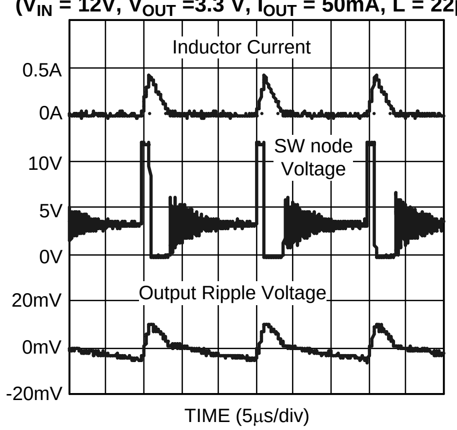
Start Up



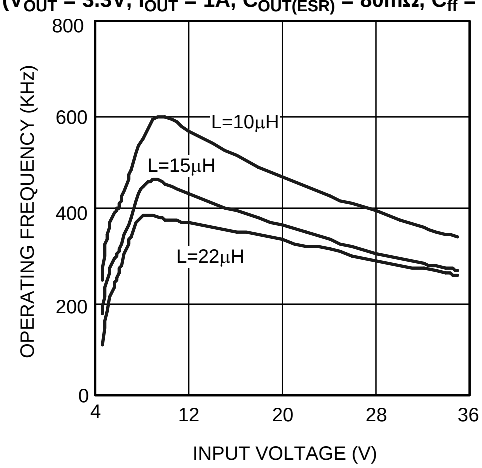
Continuous Mode Operation (V_{IN} = 12V, V_{OUT} = 3.3 V, I_{OUT} = 500mA, L = 22µH)



Discontinuous Mode Operation (V_{IN} = 12V, V_{OUT} =3.3 V, I_{OUT} = 50mA, L = 22µH)



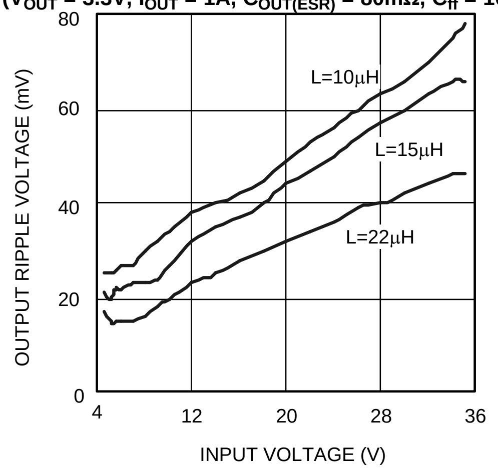
Operating Frequency vs Input Voltage (V_{OUT} = 3.3V, I_{OUT} = 1A, $C_{OUT(ESR)}$ = 80mΩ, C_{ff} = 100pF)



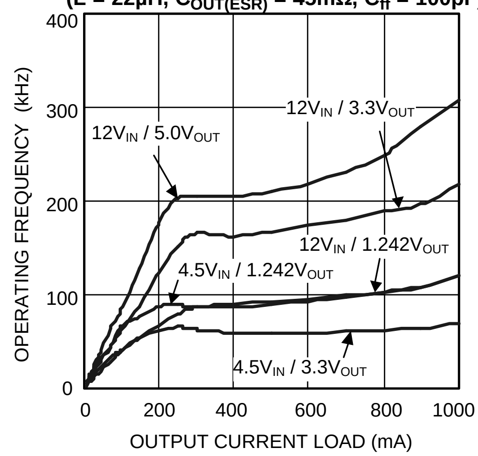
Typical Performance Characteristics (continued)

Unless otherwise specified, T_J = 25°C

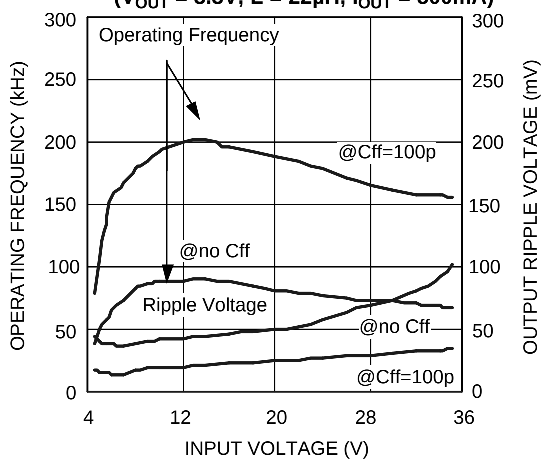
Output Ripple Voltage vs Input Voltage (V_{OUT} = 3.3V, I_{OUT} = 1A, $C_{OUT(ESR)}$ = 80mΩ, C_{ff} = 100pF)



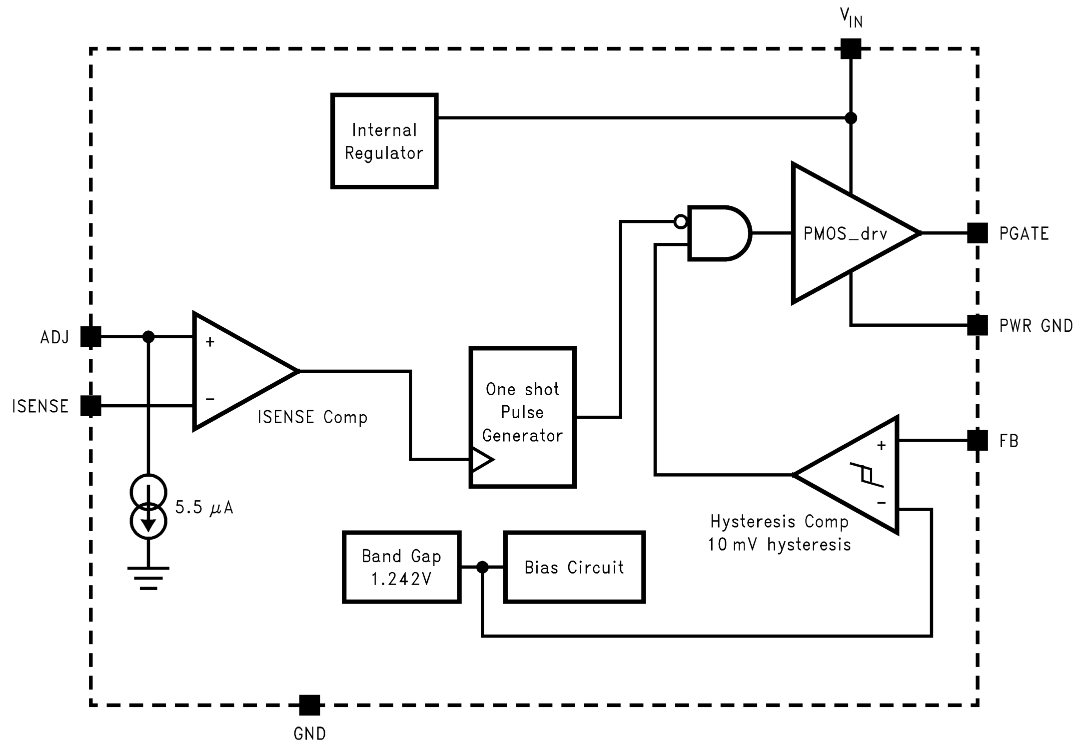
Operating Frequency vs Output Load Current (L = 22µH, $C_{OUT(ESR)}$ = 45mΩ, C_{ff} = 100pF)



Feed-Forward Capacitor (Cff) Effect (V_{OUT} = 3.3V, L = 22µH, I_{OUT} = 500mA)



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

OVERVIEW

The LM3485 is buck (step-down) DC-DC controller that uses a hysteretic control scheme. The comparator is designed with approximately 10mV of hysteresis. In response to the voltage at the FB pin, the gate drive (PGATE pin) turns the external PFET on or off. When the inductor current is too high, the current limit protection circuit engages and turns the PFET off for approximately 9µs.

Hysteretic control does not require an internal oscillator. Switching frequency depends on the external components and operating conditions. Operating frequency reduces at light loads resulting in excellent efficiency compared to other architectures.

2 external resistors can easily program the output voltage. The output can be set in a wide range from 1.242V (typical) to V_{IN}.

HYSTERETIC CONTROL CIRCUIT

The LM3485 uses a comparator based voltage control loop. The feedback is compared to a 1.242V reference and a 10mV hysteresis is designed into the comparator to ensure noise free operation.

When the FB input to the comparator falls below the reference voltage, the output of the comparator moves to a low state. This results in the driver output, PGATE, pulling the gate of the PFET low and turning on the PFET. With the PFET on, the input supply charges Cout and supplies current to the load via the series path through the PFET and the inductor. Current through the Inductor ramps up linearly and the output voltage increases. As the FB voltage reaches the upper threshold, which is the internal reference voltage plus 10mV, the output of the comparator changes from low to high, and the PGATE responds by turning the PFET off. As the PFET turns off, the inductor voltage reverses, the catch diode turns on, and the current through the inductor ramps down. Then, as the output voltage reaches the internal reference voltage again, the next cycle starts.

The LM3485 operates in discontinuous conduction mode at light load current or continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the inductor starts at zero and ramps up to the peak, then ramps down to zero. Next cycle starts when the FB voltage reaches the internal voltage. Until then, the inductor current remains zero. Operating frequency is lower and switching losses reduce. In continuous conduction mode, current always flows through the inductor and never ramps down to zero.

The output voltage (V_{OUT}) can be programmed by 2 external resistors. It can be calculated as follows:

$$V_{OUT} = 1.242 * (R1 + R2) / R2 \quad (1)$$

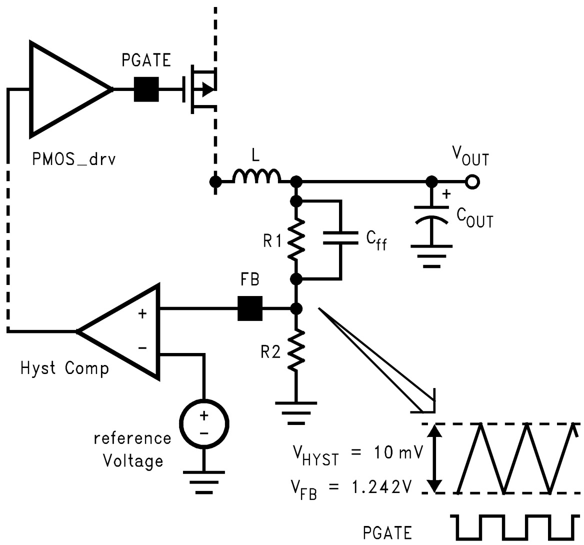


Figure 2. Hysteretic Window

The minimum output voltage ripple (V_{OUT_PP}) can be calculated in the same way.

$$V_{OUT\_PP} = V_{HYST} (R1 + R2) / R2 \quad (2)$$

For example, with V_{OUT} set to 3.3V, V_{OUT_PP} is 26.6mV

$$V_{OUT\_PP} = 0.01 * (33K + 20K) / 20K = 0.0266V \quad (3)$$

Operating frequency (F) is determined by knowing the input voltage, output voltage, inductor, V_{HYST}, ESR (Equivalent Series Resistance) of output capacitor, and the delay. It can be approximately calculated using the formula:

$$F = \frac{V_{OUT}}{V_{IN}} * \frac{(V_{IN} - V_{OUT}) * ESR}{(V_{HYST} * \alpha * L) + (V_{IN} * delay * ESR)} \quad (4)$$

where:

α: (R1 + R2) / R2

delay: It includes the LM3485 propagation delay time and the PFET delay time. The propagation delay is 90ns typically (see Figure 3).

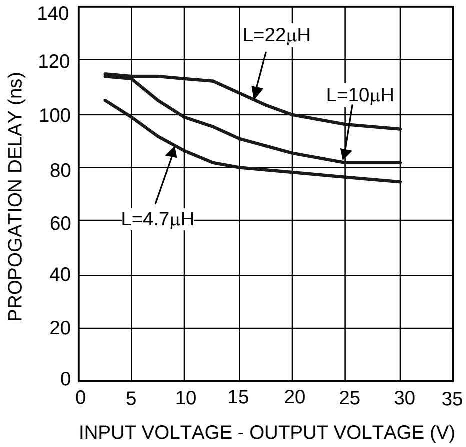


Figure 3. Propagation Delay

The operating frequency and output ripple voltage can also be significantly influenced by the speed up capacitor (Cff). Cff is connected in parallel with the high side feedback resistor, R1. The location of this capacitor is similar to where a feed forward capacitor would be located in a PWM control scheme. However it's effect on hysteretic operation is much different. The output ripple causes a current to be sourced or sunk through this capacitor. This current is essentially a square wave. Since the input to the feedback pin, FB, is a high impedance node, the current flows through R2. The end result is a reduction in output ripple and an increase in operating frequency. When adding Cff, calculate the formula above with α = 1. The value of Cff depend on the desired operating frequency and the value of R2. A good starting point is 470pF ceramic at 100kHz decreasing linearly with increased operating frequency. Also note that as the output voltage is programmed below 2.5V, the effect of Cff will decrease significantly.

CURRENT LIMIT OPERATION

The LM3485 has a cycle-by-cycle current limit. Current limit is sensed across the V_{DS} of the PFET or across an additional sense resistor. When current limit is activated, the LM3485 turns off the external PFET for a period of 9µs(typical). The current limit is adjusted by an external resistor, R_{ADJ}.

The current limit circuit is composed of the ISENSE comparator and the one-shot pulse generator. The positive input of the ISENSE comparator is the ADJ pin. An internal 5.5µA current sink creates a voltage across the external R_{ADJ} resistor. This voltage is compared to the voltage across the PFET or sense resistor. The ADJ voltage can be calculated as follows:

$$V_{ADJ} = V_{IN} - (R_{ADJ} * 3.0\mu A) \quad (5)$$

Where 3.0µA is the minimum $I_{CL\text{-}ADJ}$ value.

The negative input of the ISENSE comparator is the ISENSE pin that should be connected to the drain of the external PFET. The inductor current is determined by sensing the V_{DS}. It can be calculated as follows.

$$V_{ISENSE} = V_{IN} - (R_{DSON} * I_{IND\_PEAK}) = V_{IN} - V_{DS} \quad (6)$$

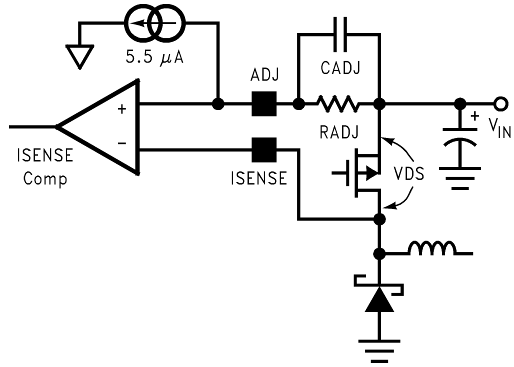


Figure 4. Current Sensing by V_{DS}

The current limit is activated when the voltage at the ADJ pin exceeds the voltage at the I_{SENSE} pin. The ISENSE comparator triggers the 9µs one shot pulse generator forcing the driver to turn the PFET off. The driver turns the PFET back on after 9µs. If the current has not reduced below the set threshold, the cycle will repeat continuously.

A filter capacitor, C_{ADJ}, should be placed as shown in Figure 4. C_{ADJ} filters unwanted noise so that the ISENSE comparator will not be accidentally triggered. A value of 100pF to 1nF is recommended in most applications. Higher values can be used to create a soft-start function (see START UP).

The current limit comparator has approximately 100ns of blanking time. This ensures that the PFET is fully on when the current is sensed. However, under extreme conditions such as cold temperature, some PFETs may not fully turn on within the blanking time. In this case, the current limit threshold must be increased. If the current limit function is used, the on time must be greater than 100ns. Under low duty cycle operation, the maximum operating frequency will be limited by this minimum on time.

During current limit operation, the output voltage will drop significantly as will operating frequency. As the load current is reduced, the output will return to the programmed voltage. However, there is a current limit fold back phenomenon inherent in this current limit architecture. See Figure 5.

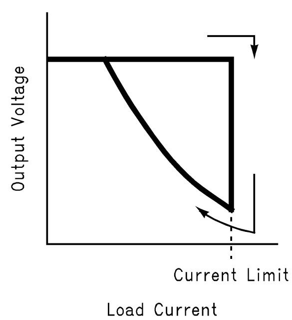


Figure 5. Current Limit Fold Back Phenomenon

At high input voltages (>28V) increased undershoot at the switch node can cause an increase in the current limit threshold. To avoid this problem, a low Vf Schottky catch diode must be used (see CATCH DIODE SELECTION (D1)). Additionally, a resistor can be placed between the ISENSE pin and the switch node. Any value up to approximately 600Ω is recommended.

START UP

The current limit circuit is active during start-up. During start-up the PFET will stay on until either the current limit or the feedback comparator is tripped

If the current limit comparator is tripped first then the fold back characteristic should be taken into account. Start-up into full load may require a higher current limit set point or the load must be applied after start-up.

One problem with selecting a higher current limit is inrush current during start-up. Increasing the capacitance (C_{ADJ}) in parallel with R_{ADJ} results in soft-start. C_{ADJ} and R_{ADJ} create an RC time constant forcing current limit to activate at a lower current. The output voltage will ramp more slowly when using the soft-start functionality. There are example start-up plots for C_{ADJ} equal to 1nF and 10nF in the Typical Performance Characteristics. Lower values for C_{ADJ} will have little to no effect on soft-start.

EXTERNAL SENSE RESISTOR

The V_{DS} of a PFET will tend to vary significantly over temperature. This will result an equivalent variation in current limit. To improve current limit accuracy an external sense resistor can be connected from V_{IN} to the source of the PFET, as shown in Figure 6.

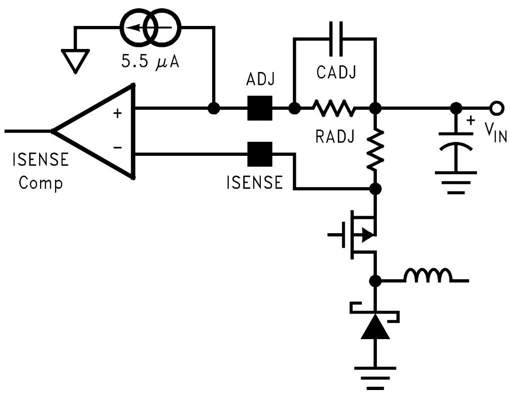


Figure 6. Current Sensing by External Resistor

PGATE

When switching, the PGATE pin swings from VIN (off) to some voltage below VIN (on). How far the PGATE will swing depends on several factors including the capacitance, on time, and input voltage.

As shown in the Typical Performance Characteristics, PGATE voltage swing will increase with decreasing gate capacitance. Although PGATE voltage will typically be around VIN-5V, with every small gate capacitances, this value can increase to a typical maximum of VIN-8.3V.

Additionally, PGATE swing voltage will increase as on time increases. During long on times, such as when operating at 100% duty cycle, the PGATE voltage will eventually fall to its maximum voltage of VIN-8.3V (typical) regardless of the PFET gate capacitance.

The PGATE voltage will not fall below 0.4V (typical). Therefore, when the input voltage falls below approximately 9V, the PGATE swing voltage range will be reduced. At an input voltage of 7V, for instance, PGATE will swing from 7V to a minimum of 0.4V.

DESIGN INFORMATION

Hysteretic control is a simple control scheme. However the operating frequency and other performance characteristics highly depend on external conditions and components. If either the inductance, output capacitance, ESR, V_{IN}, or Cff is changed, there will be a change in the operating frequency and output ripple. The best approach is to determine what operating frequency is desirable in the application and then begin with the selection of the inductor and C_{OUT} ESR.

INDUCTOR SELECTION (L1)

The important parameters for the inductor are the inductance and the current rating. The LM3485 operates over a wide frequency range and can use a wide range of inductance values. A good rule of thumb is to use the equations used for **Simple Switchers**®. The equation for inductor ripple (Δi) as a function of output current (I_{OUT}) is:

for I_{out} < 2.0Amps

$\Delta i \leq I_{out} * 0.386827 * I_{out}^{-0.366726}$

for $I_{out} > 2.0$Amps

$\Delta i \leq I_{out} * 0.3$

The inductance can be calculated based upon the desired operating frequency where:

$$L = \frac{V_{IN} - V_{DS} - V_{OUT}}{\Delta i} \bullet \frac{D}{f} \tag{7}$$

And

$$D = \frac{V_{OUT} + V_D}{V_{IN} - V_{DS} + V_D} \tag{8}$$

where D is the duty cycle, V_D is the diode forward voltage, and V_{DS} is the voltage drop across the PFET.

The inductor should be rated to the following:

$$Ipk = (Iout+\Delta i/2)*1.1 \tag{9}$$

$$I_{RMS} = \sqrt{iout^2 + \frac{\Delta i^2}{3}} \tag{10}$$

The inductance value and the resulting ripple is one of the key parameters controlling operating frequency. The second is the ESR.

OUTPUT CAPACITOR SELECTION (C_{OUT})

The ESR of the output capacitor times the inductor ripple current is equal to the output ripple of the regulator. However, the V_{HYST} sets the first order value of this ripple. As ESR is increased with a given inductance, then operating frequency increases as well. If ESR is reduced then the operating frequency reduces.

The use of ceramic capacitors has become a common desire of many power supply designers. However, ceramic capacitors have a very low ESR resulting in a 90° phase shift of the output voltage ripple. This results in low operating frequency and increased output ripple. To fix this problem a low value resistor should be added in series with the ceramic output capacitor. Although counter intuitive, this combination of a ceramic capacitor and external series resistance provide highly accurate control over the output voltage ripple. The other types capacitor, such as Sanyo POS CAP and OS-CON, Panasonic SP CAP, Nichicon "NA" series, are also recommended and may be used without additional series resistance.

For all practical purposes, any type of output capacitor may be used with proper circuit verification.

INPUT CAPACITOR SELECTION (C_{IN})

A bypass capacitor is required between the input source and ground. It must be located near the source pin of the external PFET. The input capacitor prevents large voltage transients at the input and provides the instantaneous current when the PFET turns on.

The important parameters for the input capacitor are the voltage rating and the RMS current rating. Follow the manufacturer's recommended voltage derating. For high input voltage application, low ESR electrolytic capacitor, the Nichicon "UD" series or the Panasonic "FK" series, is available. The RMS current in the input capacitor can be calculated.

$$I_{RMS\_CIN} = I_{OUT} * \frac{(V_{OUT} * (V_{IN} - V_{OUT}))^{1/2}}{V_{IN}} \tag{11}$$

The input capacitor power dissipation can be calculated as follows.

$$P_{D(CIN)} = I_{RMS\_CIN}^2 * ESR_{CIN} \tag{12}$$

The input capacitor must be able to handle the RMS current and the P_D. Several input capacitors may be connected in parallel to handle large RMS currents. In some cases it may be much cheaper to use multiple electrolytic capacitors than a single low ESR, high performance capacitor such as OS-CON or Tantalum. The capacitance value should be selected such that the ripple voltage created by the charge and discharge of the capacitance is less than 10% of the total ripple across the capacitor.

PROGRAMMING THE CURRENT LIMIT (R_{ADJ})

The current limit is determined by connecting a resistor (R_{ADJ}) between input voltage and the ADJ pin.

$$R_{ADJ} = I_{IND\_PEAK} * R_{DSON}/I_{CL\_ADJ} \quad (13)$$

where:

R_{DSON} : Drain-Source ON resistance of the external PFET

I_{CL_ADJ} : 3.0µA minimum

$I_{IND\_PEAK} = I_{LOAD} + I_{RIPPLE}/2$

Using the minimum value for I_{CL_ADJ} (3.0µA) ensures that the current limit threshold will be set higher than the peak inductor current.

The R_{ADJ} value must be selected to ensure that the voltage at the ADJ pin does not fall below 3.5V. With this in mind, $R_{ADJ\_MAX} = (V_{IN}\text{-}3.5)/7\mu A$. If a larger R_{ADJ} value is needed to set the desired current limit, either use a PFET with a lower R_{DSON}, or use a current sense resistor as shown in Figure 6.

The current limit function can be disabled by connecting the ADJ pin to ground and ISENSE to VIN.

CATCH DIODE SELECTION (D1)

The important parameters for the catch diode are the peak current, the peak reverse voltage, and the average power dissipation. The average current through the diode can be calculated as following.

$$I_{D\_AVE} = I_{OUT}{}^{*} (1 - D) \quad (14)$$

The off state voltage across the catch diode is approximately equal to the input voltage. The peak reverse voltage rating must be greater than input voltage. In nearly all cases a Schottky diode is recommended. In low output voltage applications a low forward voltage provides improved efficiency. For high temperature applications, diode leakage current may become significant and require a higher reverse voltage rating to achieve acceptable performance.

P-CHANNEL MOSFET SELECTION (Q1)

The important parameters for the PFET are the maximum Drain-Source voltage (V_{DS}), the on resistance (R_{DSON}), Current rating, and the input capacitance.

The voltage across the PFET when it is turned off is equal to the sum of the input voltage and the diode forward voltage. The V_{DS} must be selected to provide some margin beyond the input voltage.

PFET drain current, Id, must be rated higher than the peak inductor current, $I_{IND\text{-}PEAK}$.

Depending on operating conditions, the PGATE voltage may fall as low as V_{IN} - 8.3V. Therefore, a PFET must be selected with a V_{GS} greater than the maximum PGATE swing voltage.

As input voltage decreases below 9V, PGATE swing voltage may also decrease. At 5.0V input the PGATE will swing from V_{IN} to V_{IN} - 4.6V. To ensure that the PFET turns on quickly and completely, a low threshold PFET should be used when the input voltage is less than 7V.

However, PFET switching losses will increase as the V_{GS} threshold decreases. Therefore, whenever possible, a high threshold PFET should be selected. Total power loss in the FET can be approximated using the following equation:

$$PDswitch = R_{DSON}*I_{OUT}{}^{2}*D + F*I_{OUT}*V_{IN}*(t_{on} + t_{off})/2 \quad (15)$$

where:

t_{on} = FET turn on time

t_{off} = FET turn off time

A value of 10ns to 20ns is typical for ton and toff.

A PFET should be selected with a turn on rise time of less than 100ns. Slower rise times will degrade efficiency, can cause false current limiting, and in extreme cases may cause abnormal spiking at the PGATE pin.

The R_{DSON} is used in determining the current limit resistor value, R_{ADJ}. Note that the R_{DSON} has a positive temperature coefficient. At 100°C, the R_{DSON} may be as much as 150% higher than the 25°C value. This increase in R_{DSON} must be considered it when determining R_{ADJ} in wide temperature range applications. If the current limit is set based upon 25°C ratings, then false current limiting can occur at high temperature.

Keeping the gate capacitance below 2000pF is recommended to keep switching losses and transition times low. This will also help keep the PFET drive current low, which will improve efficiency and lower the power dissipation within the controller.

As gate capacitance increases, operating frequency should be reduced and as gate capacitance decreases operating frequency can be increased.

PCB Layout

The PC board layout is very important in all switching regulator designs. Poor layout can cause switching noise into the feedback signal and general EMI problems. For minimal inductance, the wires indicated by heavy lines should be as wide and short as possible. Keep the ground pin of the input capacitor as close as possible to the anode of the diode. This path carries a large AC current. The switching node, the node with the diode cathode, inductor, and FET drain, should be kept short. This node is one of the main sources for radiated EMI since it is an AC voltage at the switching frequency. It is always good practice to use a ground plane in the design, particularly at high currents.

The two ground pins, PWR GND and GND, should be connected by as short a trace as possible; they can be connected underneath the device. These pins are resistively connected internally by approximately 50Ω. The ground pins should be tied to the ground plane, or to a large ground trace in close proximity to both the FB divider and C_{OUT} grounds.

The gate pin of the external PFET should be located close to the PGATE pin. However, if a very small FET is used, a resistor may be required between PGATE and the gate of the FET to reduce high frequency ringing. Since this resistor will slow the PFET's rise time, the current limit blanking time should be taken into consideration (see CURRENT LIMIT OPERATION).

The feedback voltage signal line can be sensitive to noise. Avoid inductive coupling to the inductor or the switching node, by keeping the FB trace away from these areas.

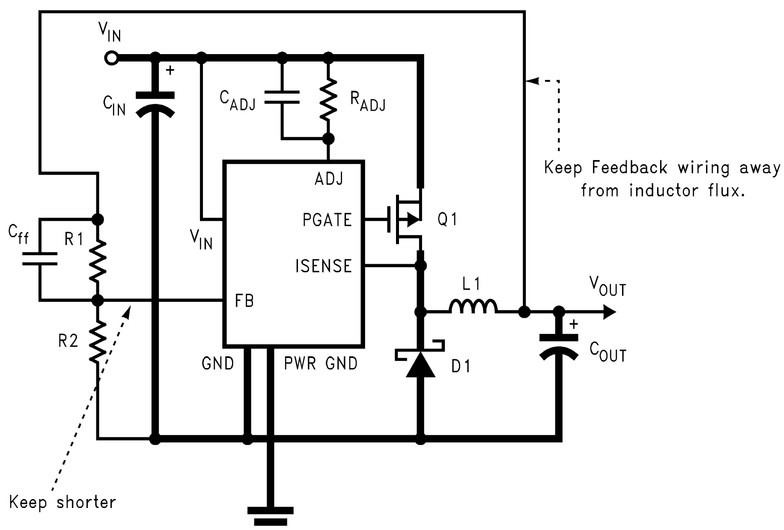


Figure 7. Typical PCB Layout Schematic (3.3V output)

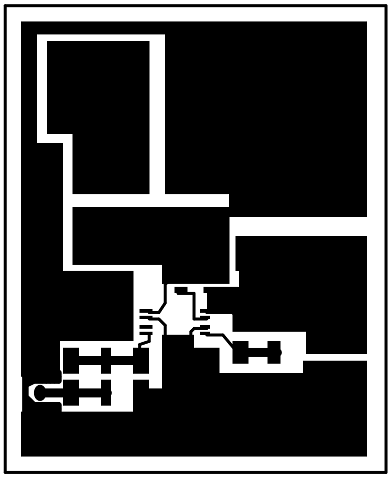


Figure 8. Top Layer, Typical PCB Layout (3.3V Output)

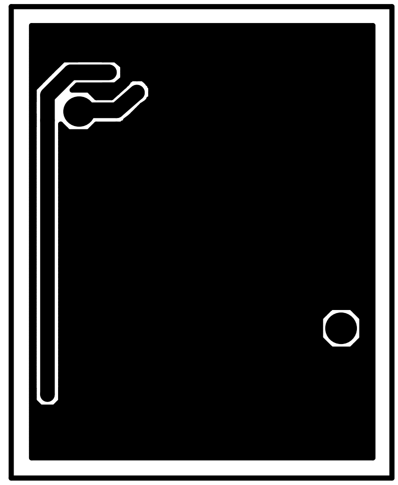


Figure 9. Bottom Layer, Typical PCB Layout (3.3V Output)

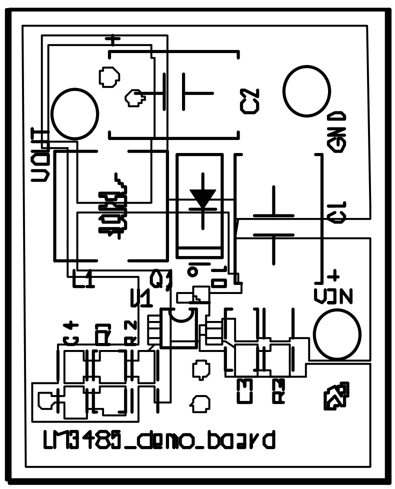


Figure 10. Silk Screen, Typical PCB Layout (3.3V Output)

C1: C_{IN} 22µF/35V EEJL1VD226R (Panasonic)

C2: C_{OUT} 100µF/6.3V 6TPC100M (Sanyo)

C3: C_{ADJ} 1nF Ceramic Chip Capacitor

C4: C_{FF} 100pF Ceramic Chip Capacitor

D1: 1A/40V MBRS140T3 (On Semiconductor)

L1: 22µH :QH66SN220M01L (Murata)

Q1: FDC5614P (Fairchild)

R1: 33kΩ Chip Resistor

R2: 20kΩ Chip Resistor

R3: R_{ADJ} 24kΩ Chip Resistor

REVISION HISTORY

Changes from Revision F (February 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3485MM	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	S29B	Samples
LM3485MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S29B	Samples
LM3485MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	S29B	Samples
LM3485MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S29B	Samples
LM3485Q1MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SVJB	Samples
LM3485Q1MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SVJB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF LM3485, LM3485-Q1 :

- Catalog: LM3485

- Automotive: LM3485-Q1

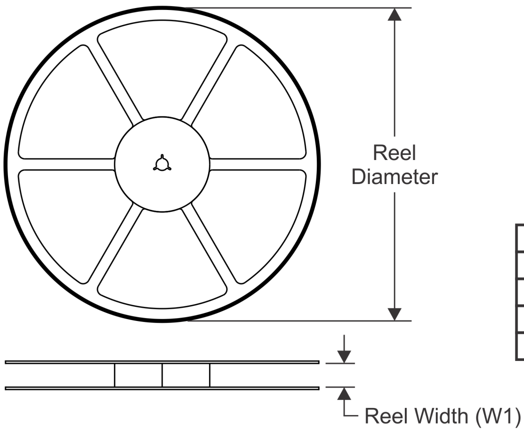
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

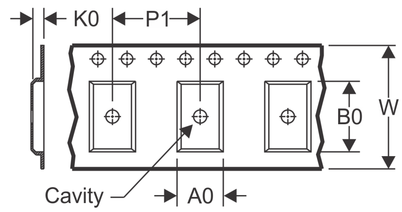
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

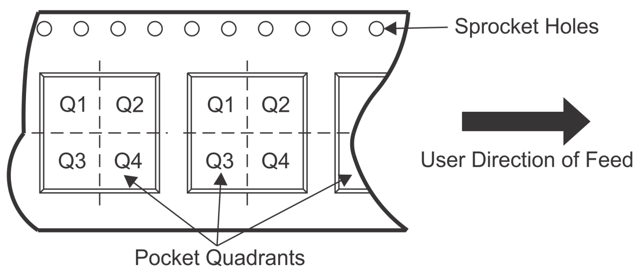


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

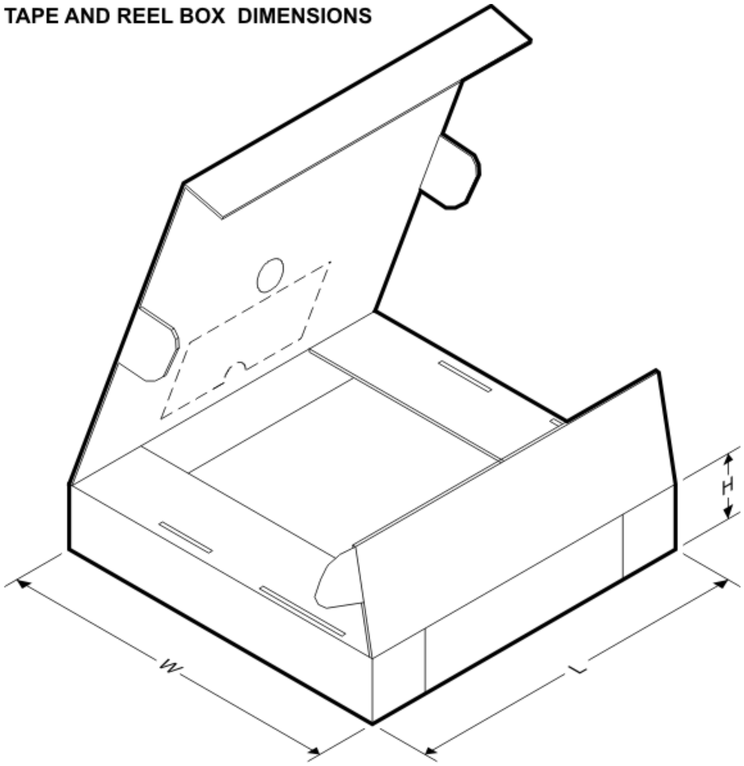
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3485MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3485MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3485MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3485MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3485Q1MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3485Q1MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

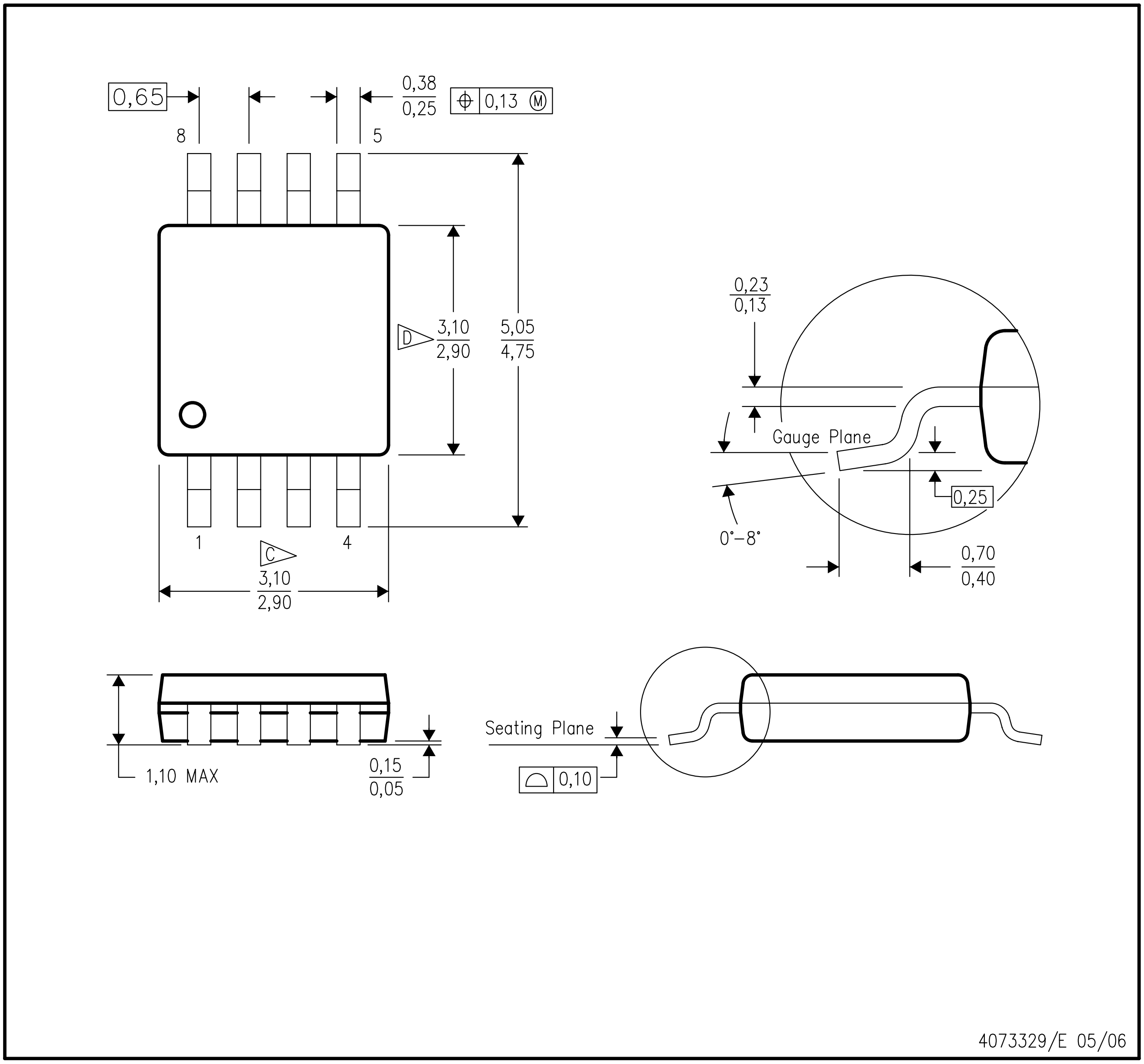
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3485MM	VSSOP	DGK	8	1000	203.0	190.0	41.0
LM3485MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LM3485MMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM3485MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM3485Q1MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LM3485Q1MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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