3.3-V RS-485 TRANSCEIVERS

FEATURES

- **Operates With a 3.3-V Supply**
- **Bus-Pin ESD Protection Exceeds 16 kV HBM**
- **1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)**
- **Optional Driver Output Transition Times for Signaling Rates† of 1 Mbps, 10 Mbps and 25 Mbps**
- **Meets or Exceeds the Requirements of ANSI TIA/EIA-485-A**
- **Bus-Pin Short Circuit Protection From –7 V to 12 V**
- **Low-Current Standby Mode . . . 1 μA Typical**
- **Open-Circuit, Idle-Bus, and Shorted-Bus Failsafe Receiver**
- **Thermal Shutdown Protection**
- **Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications**
- **SN75176 Footprint**

APPLICATIONS

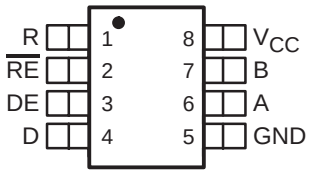
- **Digital Motor Control**
- **Utility Meters**
- **Chassis-to-Chassis Interconnects**
- **Electronic Security Stations**
- **Industrial Process Control**
- **Building Automation**
- **Point-of-Sale (POS) Terminals and Networks**

DESCRIPTION

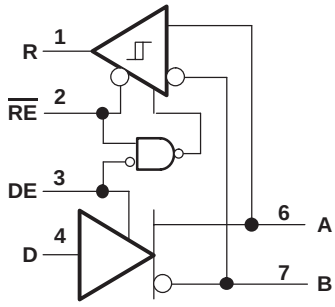
The SN65HVD10, SN75HVD10, SN65HVD11, SN75HVD11, SN65HVD12, and SN75HVD12 combine a 3-state differential line driver and differential input line receiver that operate with a single 3.3-V power supply. They are designed for balanced transmission lines and meet or exceed ANSI standard TIA/EIA-485-A and ISO 8482:1993. These differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. The drivers and receivers have active-high and active-low enables respectively, that can be externally connected together to function as direction control. Very low device standby supply current can be achieved by disabling the driver and the receiver.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/ output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These parts feature wide positive and negative common-mode voltage ranges, making them suitable for party-line applications.

D OR P PACKAGE
(TOP VIEW)



LOGIC DIAGRAM
(POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

SIGNALING RATE	UNIT LOADS	T_A	PACKAGE		SOIC MARKING
			SOIC(1)	PDIP	
25 Mbps	1/2	−40°C to 85°C	SN65HVD10D	SN65HVD10P	VP10
10 Mbps	1/8		SN65HVD11D	SN65HVD11P	VP11
1 Mbps	1/8		SN65HVD12D	SN65HVD12P	VP12
25 Mbps	1/2	−0°C to 70°C	SN75HVD10D	SN75HVD10P	VN10
10 Mbps	1/8		SN75HVD11D	SN75HVD11P	VN11
1 Mbps	1/8		SN75HVD12D	SN75HVD12P	VN12
25 Mbps	1/2	−40°C to 125°C	SN65HVD10QD	SN65HVD10QP	VP10Q
10 Mbps	1/8		SN65HVD11QD	SN65HVD11QP	VP11Q

(1) The D package is available taped and reeled. Add an R suffix to the part number (i.e., SN75HVD11DR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

			SN65HVD10, SN75HVD10 SN65HVD11, SN75HVD11 SN65HVD12, SN75HVD12
Supply voltage range, V_{CC}			−0.3 V to 6 V
Voltage range at A or B			−9 V to 14 V
Input voltage range at D, DE, R or $\overline{RE}$			−0.5 V to V_{CC} + 0.5 V
Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 11)			−50 V to 50 V
Electrostatic discharge	Human body model(3)	A, B and GND	16 kV
		All pins	4 kV
	Charged-device model(4)	All pins Charge	1 kV
Continuous total power dissipation			See Dissipation Rating Table
Junction temperature, T_J			170°C
Storage temperature range, T_{stg}			−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D(2)	597 mW	4.97 mW/°C	373 mW	298 mW	100 mW
D(3)	990 mW	8.26 mW/°C	620 mW	496 mW	165 mW
P	1290 mW	10.75 mW/°C	806 mW	645 mW	215 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51−3.
(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51−7.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3		3.6	V
Voltage at any bus terminal (separately or common mode) V_I or V_{IC}		−7(1)		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2		V_{CC}	V
Low-level input voltage, V_{IL}	D, DE, $\overline{RE}$	0		0.8	V
Differential input voltage, V_{ID} (see Figure 7)		−12		12	V
High-level output current, I_{OH}	Driver	−60			mA
	Receiver	−8			
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Differential load resistance, R_L		54	60		Ω
Differential load capacitance, C_L			50		pF
Signaling rate	HVD10			25	Mbps
	HVD11			10	
	HVD12			1	
Junction temperature, T_J(2)				145	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) See thermal characteristics table for information regarding this specification.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA		−1.5			V
$\lvert V_{OD}\rvert$	Differential output voltage(2)		I_O = 0		2		V_{CC}	V
			R_L = 54 Ω, See Figure 1		1.5			
			V_{test} = −7 V to 12 V, See Figure 2		1.5			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage		See Figure 1 and Figure 2		−0.2		0.2	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		See Figure 3			400		mV
$V_{OC(SS)}$	Steady-state common-mode output voltage				1.4		2.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				−0.05		0.05	V
I_{OZ}	High-impedance output current		See receiver input currents					
I_I	Input current	D			−100		0	μA
		DE			0		100	
I_{OS}	Short-circuit output current		−7 V ≤ V_O ≤ 12 V		−250		250	mA
$C_{(OD)}$	Differential output capacitance		V_{OD} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			16		pF
I_{CC}	Supply current		$\overline{RE}$ at V_{CC}, D & DE at V_{CC}, No load	Receiver disabled and driver enabled		9	15.5	mA
			$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	μA
			$\overline{RE}$ at 0 V, D & DE at V_{CC}, No load	Receiver enabled and driver enabled		9	15.5	mA

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) For T_A > 85°C, V_{CC} is ±5%.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD10	R_L = 54 Ω, C_L = 50 pF, See Figure 4	5	8.5	16	ns
		HVD11		18	25	40	
		HVD12		135	200	300	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD10		5	8.5	16	ns
		HVD11		18	25	40	
		HVD12		135	200	300	
t_r	Differential output signal rise time	HVD10		3	4.5	10	ns
		HVD11		10	20	30	
		HVD12		100	170	300	
t_f	Differential output signal fall time	HVD10		3	4.5	10	ns
		HVD11		10	20	30	
		HVD12		100	170	300	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD10				1.5	ns
		HVD11				2.5	
		HVD12				7	
$t_{sk(pp)}$(2)	Part-to-part skew	HVD10				6	ns
		HVD11				11	
		HVD12				100	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	HVD10	R_L = 110 Ω, $\overline{RE}$ at 0 V, See Figure 5			31	ns
		HVD11				55	
		HVD12				300	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD10				25	ns
		HVD11				55	
		HVD12				300	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	HVD10	R_L = 110 Ω, $\overline{RE}$ at 0 V, See Figure 6			26	ns
		HVD11				55	
		HVD12				300	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD10				26	ns
		HVD11				75	
		HVD12				400	
t_{PZH}	Propagation delay time, standby-to-high-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, See Figure 5			6	µs
t_{PZL}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, See Figure 6			6	µs

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = −8 mA					−0.01	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA			−0.2			V
V_{hys}	Hysteresis voltage (V_{IT+} − V_{IT-})					35		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA			−1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −8 mA,	See Figure 7	2.4			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA,	See Figure 7			0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 or V_{CC}	$\overline{RE}$ at V_{CC}		−1		1	μA
I_I	Bus input current	V_A or V_B = 12 V		HVD11, HVD12, Other input at 0 V		0.05	0.11	mA
		V_A or V_B = 12 V,	V_{CC} = 0 V			0.06	0.13	
		V_A or V_B = −7 V			−0.1	−0.05		
		V_A or V_B = −7 V,	V_{CC} = 0 V		−0.05	−0.04		
		V_A or V_B = 12 V		HVD10, Other input at 0 V		0.2	0.5	mA
		V_A or V_B = 12 V,	V_{CC} = 0 V			0.25	0.5	
		V_A or V_B = −7 V			−0.4	−0.2		
		V_A or V_B = −7 V,	V_{CC} = 0 V		−0.4	−0.15		
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2 V			−30		0	μA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.8 V			−30		0	μA
C_{ID}	Differential input capacitance	V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V				15		pF
I_{CC}	Supply current	$\overline{RE}$ at 0 V, D & DE at 0 V, No load	Receiver enabled and driver disabled			4	8	mA
		$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load	Receiver disabled and driver disabled (standby)			1	5	μA
		$\overline{RE}$ at 0 V, D & DE at V_{CC}, No load	Receiver enabled and driver enabled			9	15.5	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD10	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 8	12.5	20	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output	HVD10		12.5	20	25	
t_{PLH}	Propagation delay time, low-to-high-level output	HVD11 HVD12		30	55	70	ns
t_{PHL}	Propagation delay time, high-to-low-level output	HVD11 HVD12		30	55	70	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD10				1.5	ns
		HVD11				4	
		HVD12				4	
$t_{sk(pp)}$(2)	Part-to-part skew	HVD10				8	ns
		HVD11				15	
		HVD12				15	
t_r	Output signal rise time		C_L = 15 pF, See Figure 8	1	2	5	ns
t_f	Output signal fall time			1	2	5	
t_{PZH}(1)	Output enable time to high level		C_L = 15 pF, DE at 3 V, See Figure 9			15	ns
t_{PZL}(1)	Output enable time to low level					15	
t_{PHZ}	Output disable time from high level					20	
t_{PLZ}	Output disable time from low level					15	
t_{PZH}(2)	Propagation delay time, standby-to-high-level output		C_L = 15 pF, DE at 0, See Figure 10			6	µs
t_{PZL}(2)	Propagation delay time, standby-to-low-level output					6	

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

THERMAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
θ_{JA}	Junction−to−ambient thermal resistance(2)	High−K board(3), No airflow	D pkg		121		°C/W
		No airflow(4)	P pkg		93		
θ_{JB}	Junction−to−board thermal resistance	High−K board	D pkg		67		°C/W
		See Note (4)	P pkg		57		°C/W
θ_{JC}	Junction−to−case thermal resistance		D pkg		41		°C/W
			P pkg		55		
P_D	Device power dissipation	R_L= 60Ω, C_L = 50 pF, DE at V_{CC}, $\overline{RE}$ at 0 V, Input to D a 50% duty cycle square wave at indicated signaling rate	HVD10 (25 Mbps)		198	233	mW
			HVD11 (10 Mbps)		141	176	mW
			HVD12 (500 kbps)		133	161	mW
T_A	Ambient air temperature	High−K board, No airflow	D pkg	−40		116	°C
		No airflow(4)	P pkg	−40		123	
T_{JSD}	Thermal shutdown junction temperature				165		°C

(1) See *Application Information* section for an explanation of these parameters.

(2) The intent of θ_{JA} specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

(3) JSD51−7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

(4) JESD51−10, Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements.

PARAMETER MEASUREMENT INFORMATION

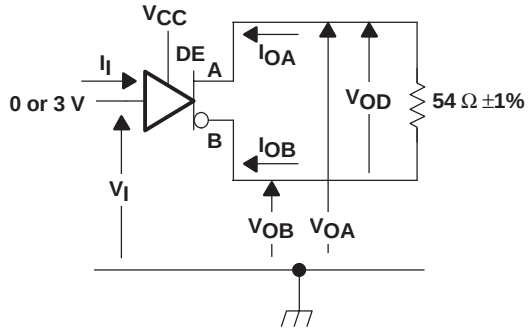


Figure 1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

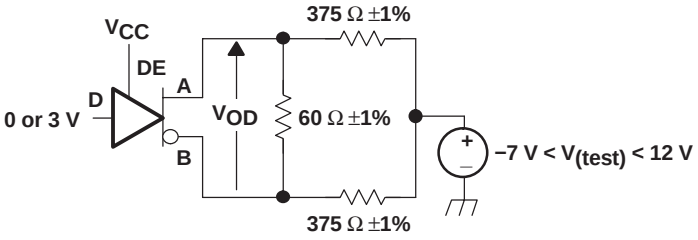
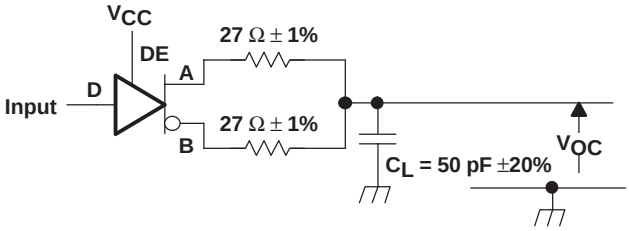
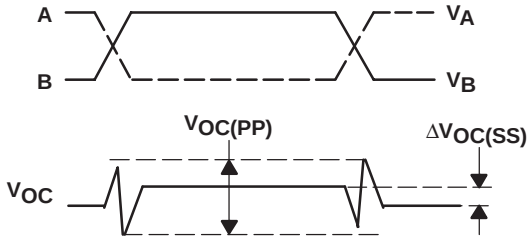


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit

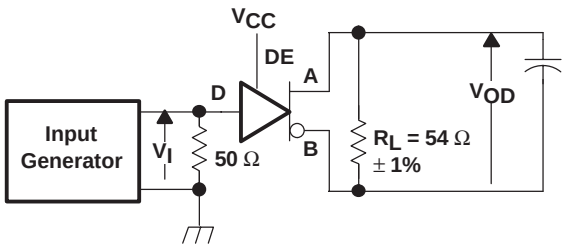


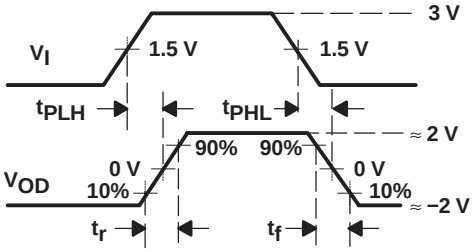
C_L Includes Fixture and Instrumentation Capacitance



Input: PRR = 500 kHz, 50% Duty Cycle, t_r<6ns, t_f<6ns, Z_O = 50 Ω

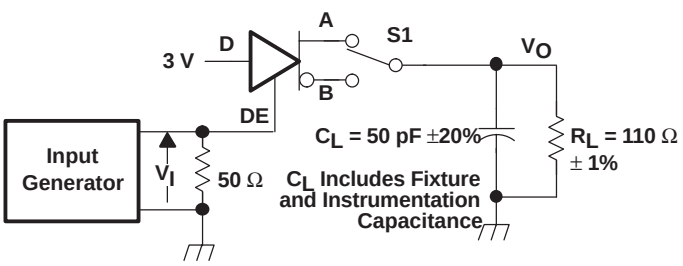
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

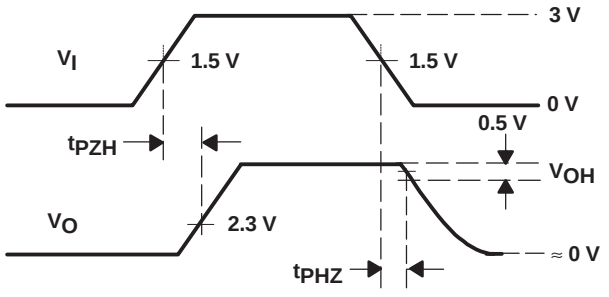




Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_O = 50 Ω

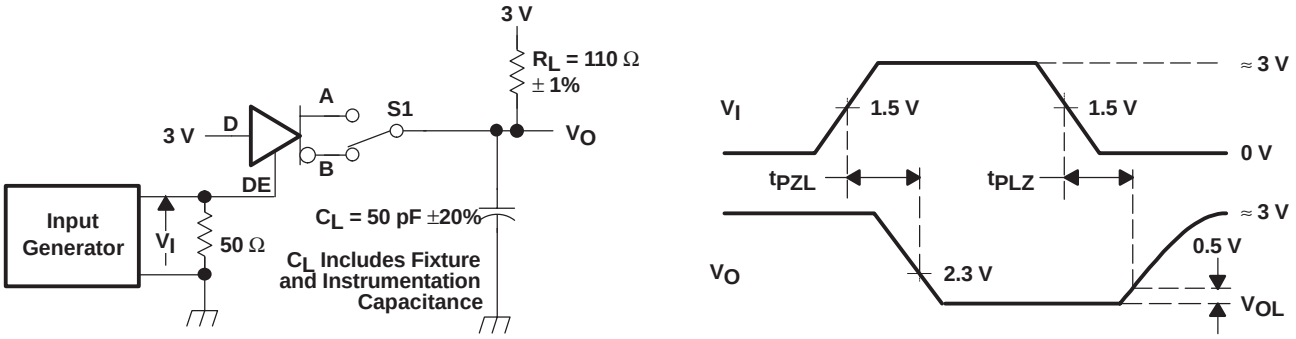
Figure 4. Driver Switching Test Circuit and Voltage Waveforms





Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_O = 50 Ω

Figure 5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_O = 50 Ω

Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

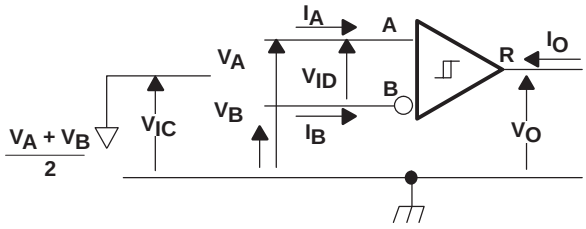
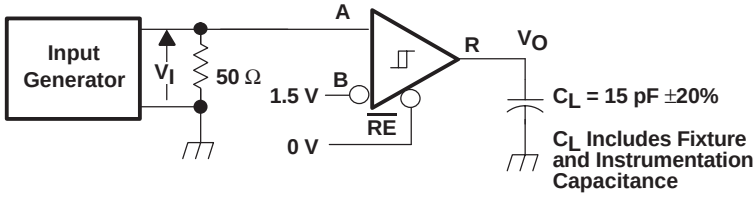


Figure 7. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_O = 50 Ω

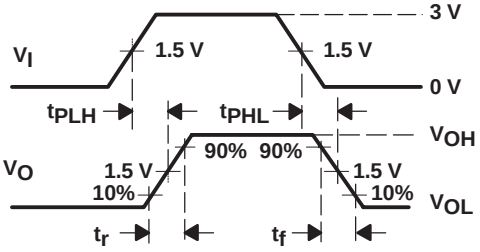


Figure 8. Receiver Switching Test Circuit and Voltage Waveforms

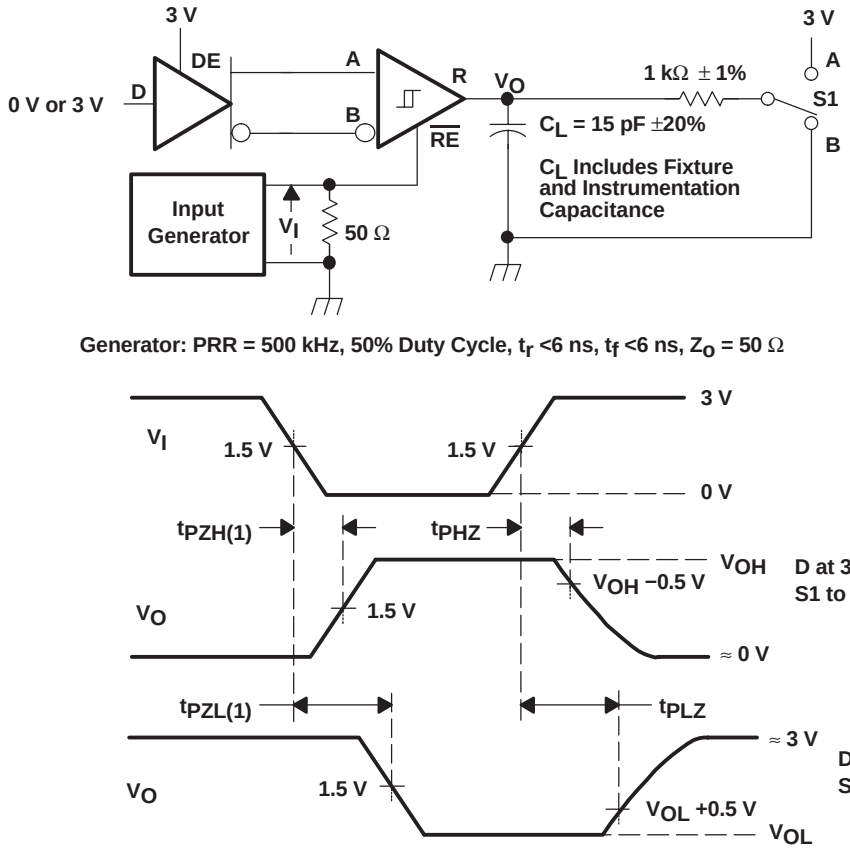
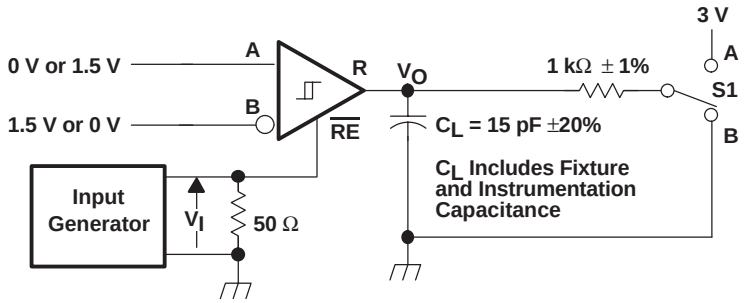


Figure 9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_O = 50 Ω

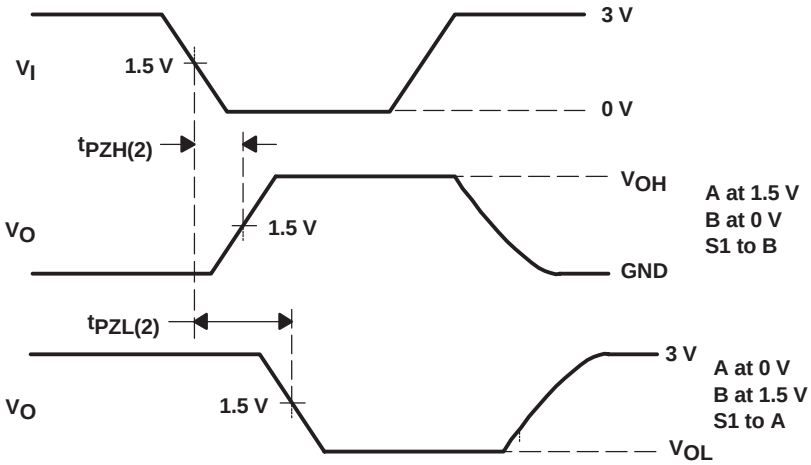
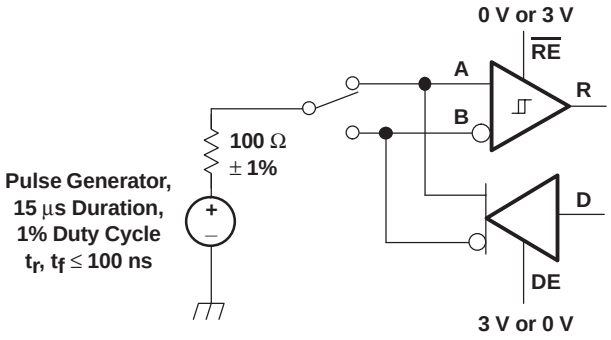


Figure 10. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 11. Test Circuit, Transient Over Voltage Test

Function Tables

DRIVER

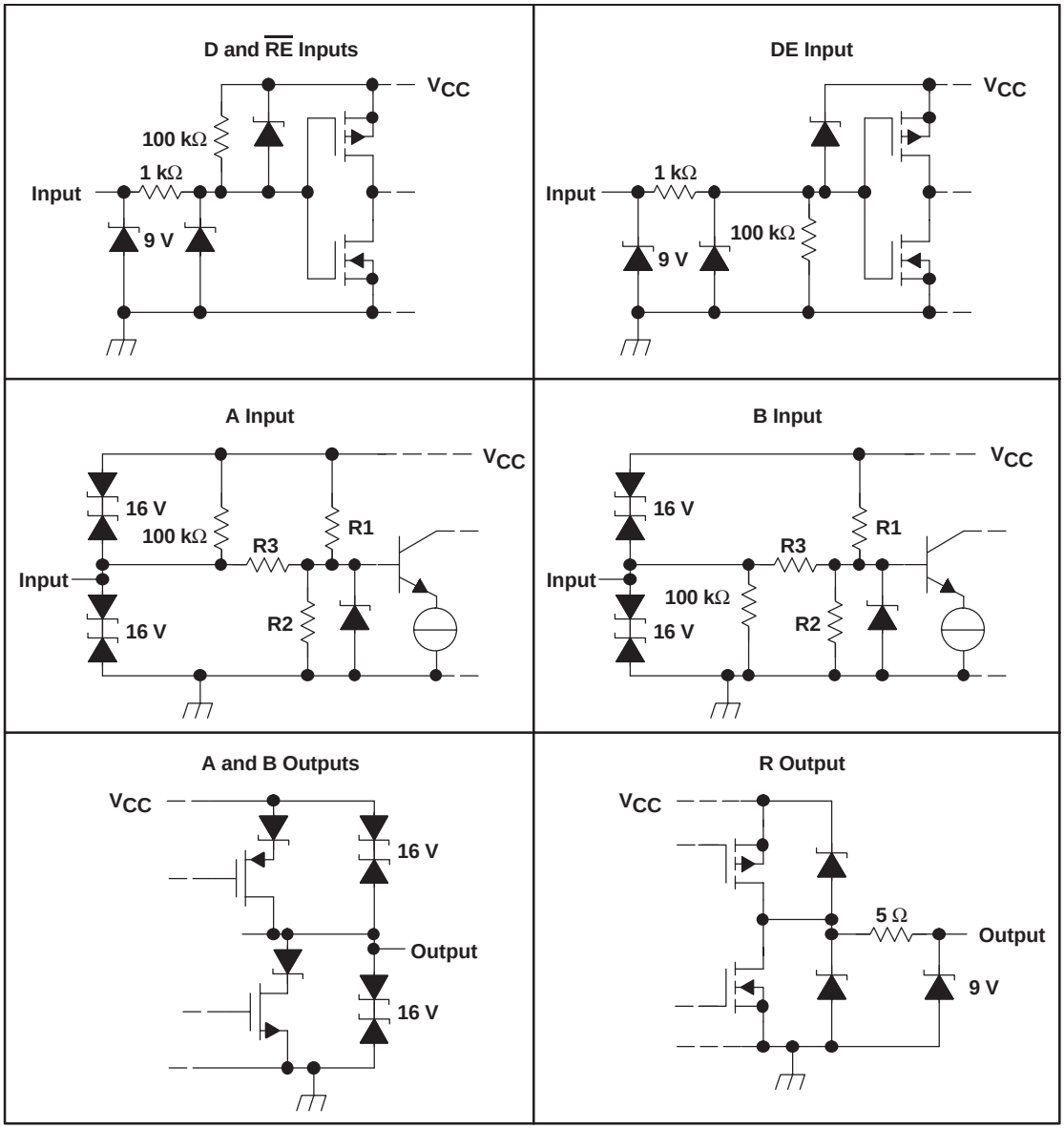
INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \le -0.2$ V	L	L
-0.2 V $< V_{ID} < -0.01$ V	L	?
-0.01 V $\le V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short Circuit	L	H

H = high level; L = low level; Z = high impedance; X = irrelevant;
? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD10	9 kΩ	45 kΩ
SN65HVD11	36 kΩ	180 kΩ
SN65HVD12	36 kΩ	180 kΩ

TYPICAL CHARACTERISTICS

HVD10 OR HVD12
RMS SUPPLY CURRENT
vs
SIGNALING RATE

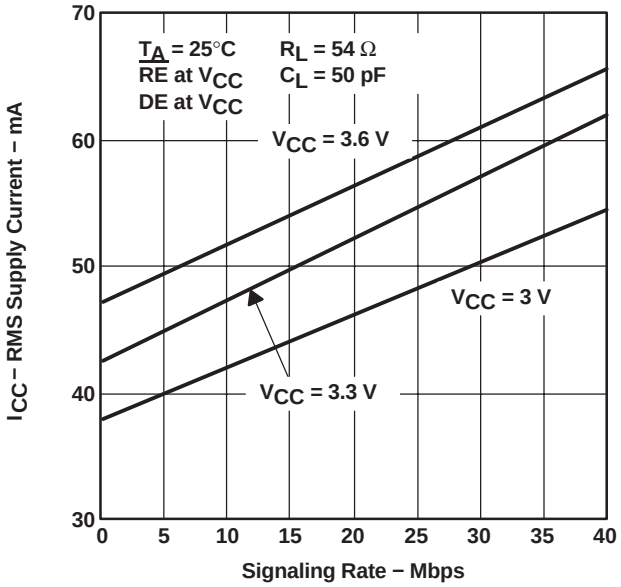


Figure 12

HVD11
RMS SUPPLY CURRENT
vs
SIGNALING RATE

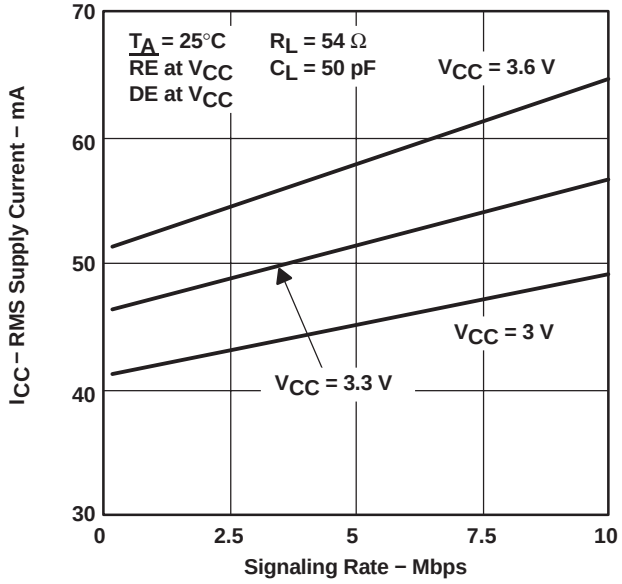


Figure 13

HVD12
RMS SUPPLY CURRENT
vs
SIGNALING RATE

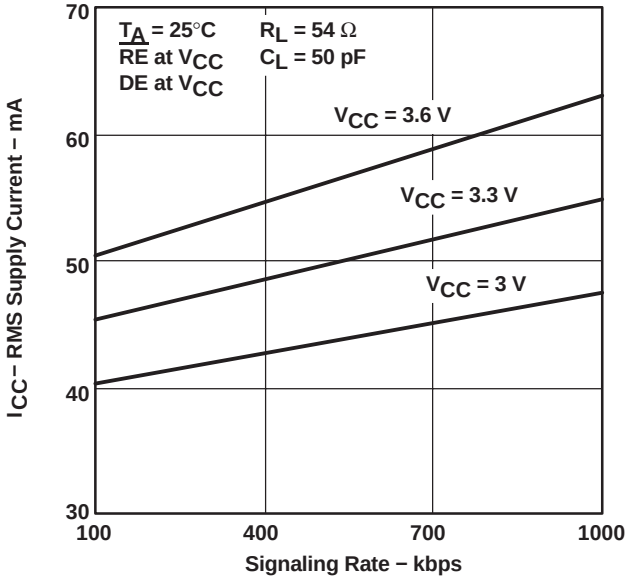


Figure 14

HVD10
BUS INPUT CURRENT
vs
BUS INPUT VOLTAGE

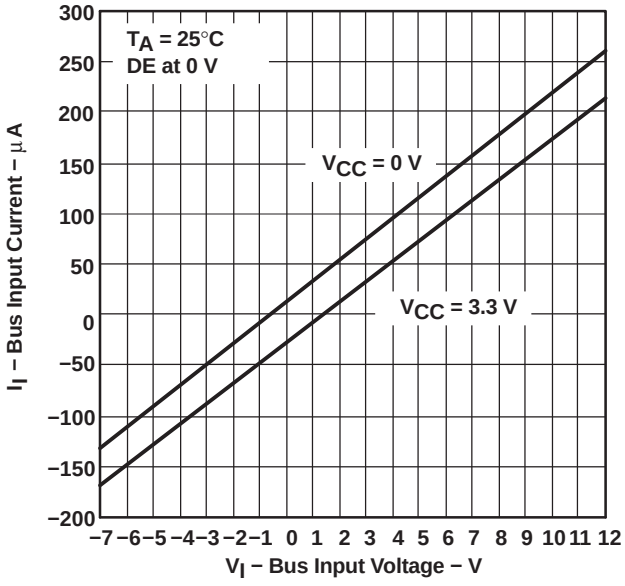


Figure 15

HVD11 OR HVD12
BUS INPUT CURRENT
vs
BUS INPUT VOLTAGE

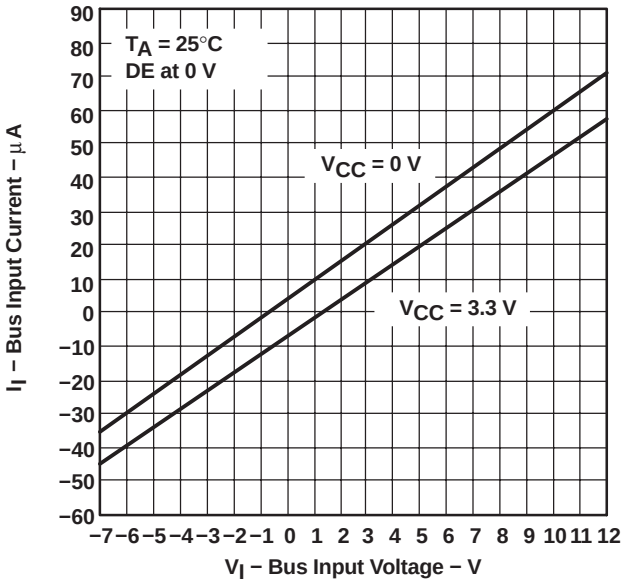


Figure 16

HIGH-LEVEL OUTPUT CURRENT
vs
DRIVER HIGH-LEVEL OUTPUT VOLTAGE

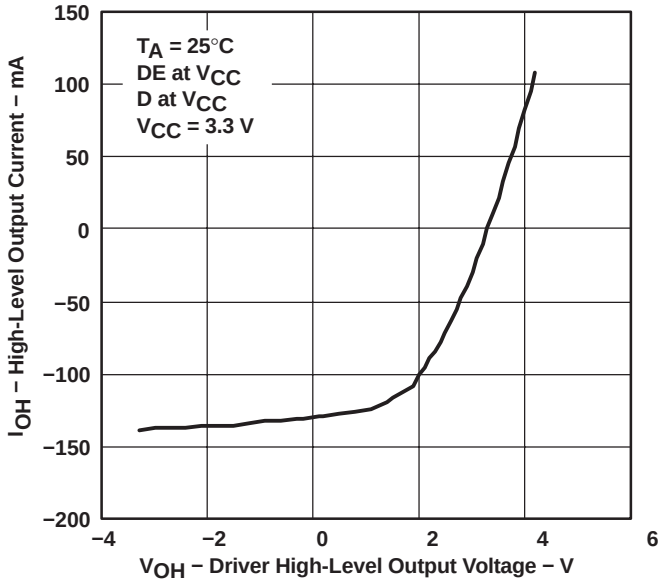


Figure 17

LOW-LEVEL OUTPUT CURRENT
vs
DRIVER LOW-LEVEL OUTPUT VOLTAGE

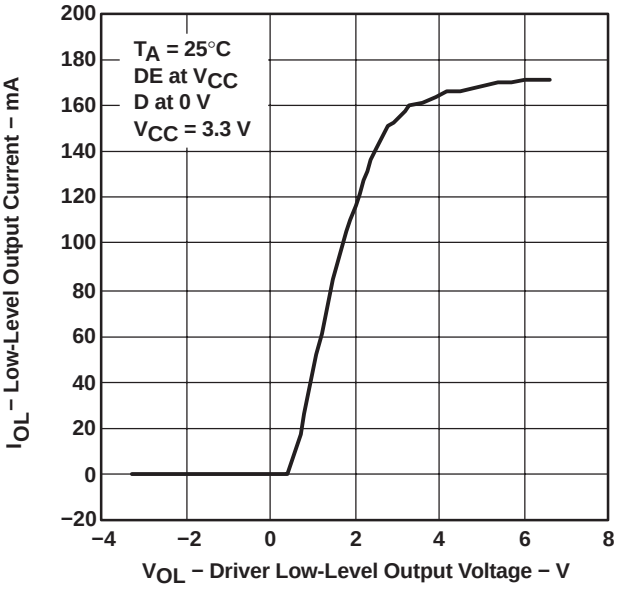


Figure 18

DRIVER DIFFERENTIAL OUTPUT
vs
FREE-AIR TEMPERATURE

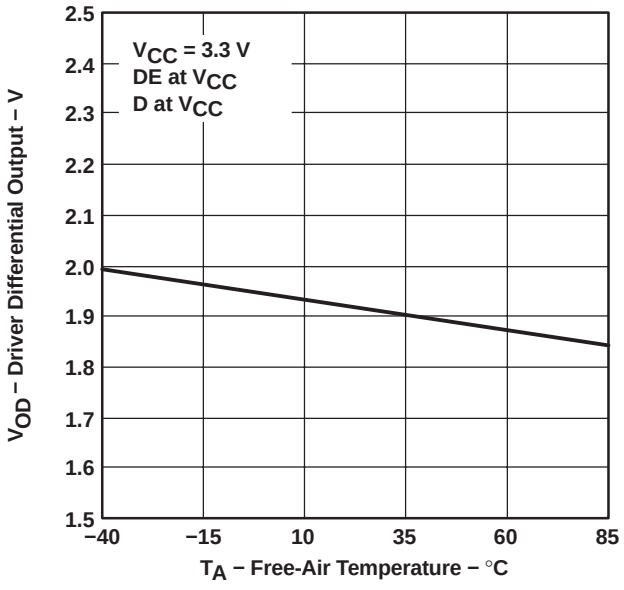


Figure 19

TYPICAL CHARACTERISTICS

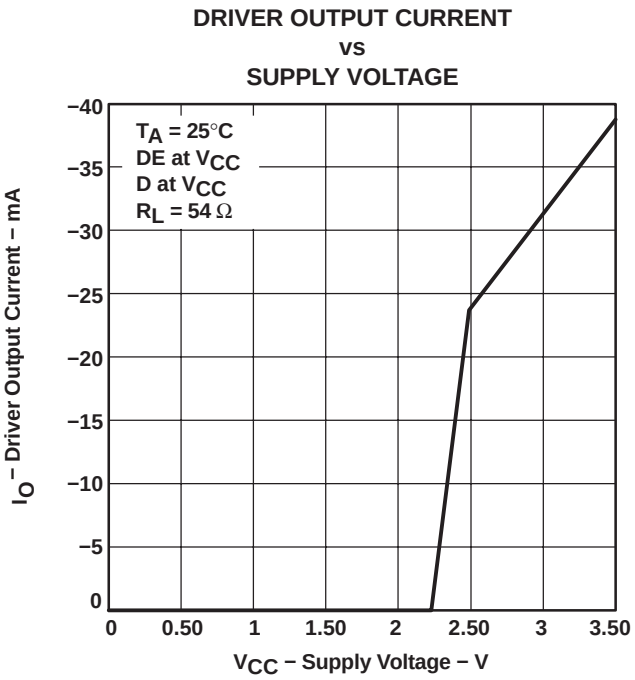
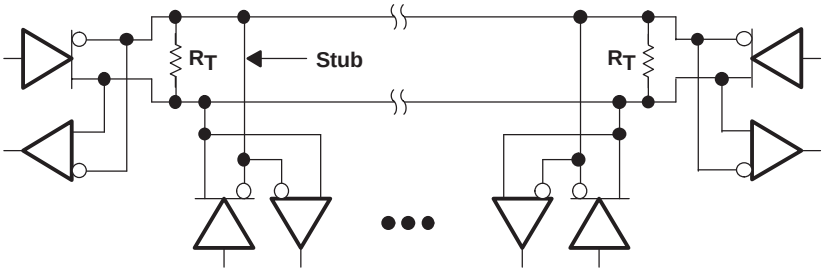


Figure 20

APPLICATION INFORMATION



Device	Number of Devices on Bus
HVD10	64
HVD11	256
HVD12	256

NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 21. Typical Application Circuit

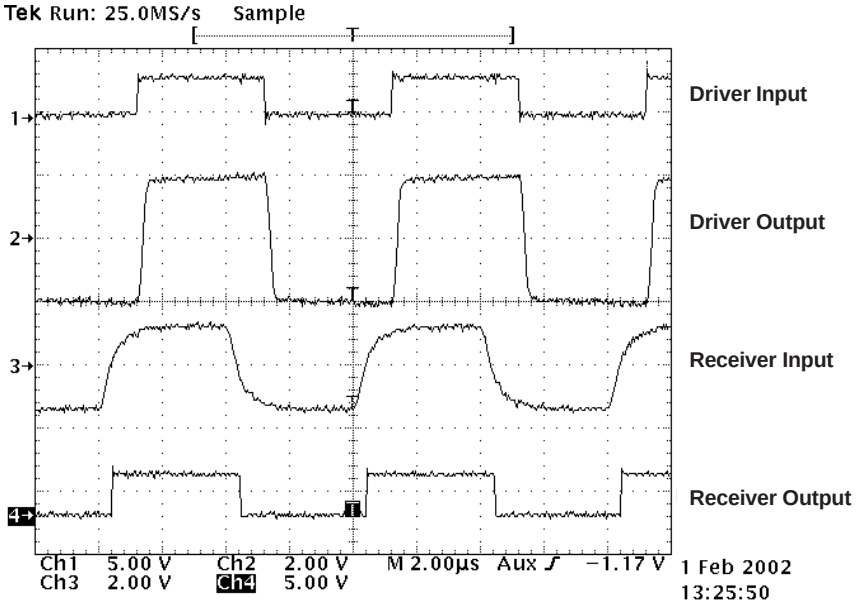


Figure 22. HVD12 Input and Output Through 2000 Feet of Cable

An example application for the HVD12 is illustrated in Figure 21. Two HVD12 transceivers are used to communicate data through a 2000 foot (600 m) length of Commscope 5524 category 5e+ twisted pair cable. The bus is terminated at each end by a 100-Ω resistor, matching the cable characteristic impedance. Figure 22 illustrates operation at a signaling rate of 250 kbps.

THERMAL CHARACTERISTICS OF IC PACKAGES

θ_{JA} **(Junction-to-Ambient Thermal Resistance)** is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is *not* a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-k board gives *best case* in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in θ_{JA} can be measured between these two test cards

θ_{JC} **(Junction-to-Case Thermal Resistance)** is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is *not* a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} **(Junction-to-Board Thermal Resistance)** is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 23).

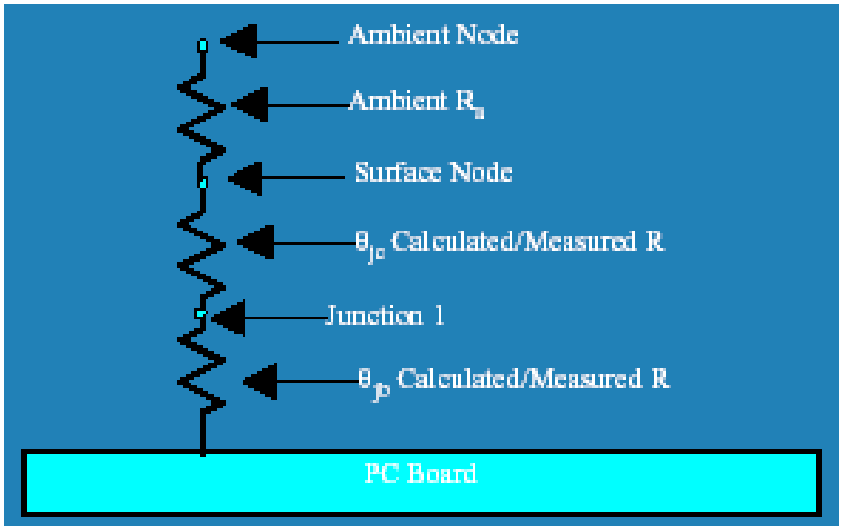
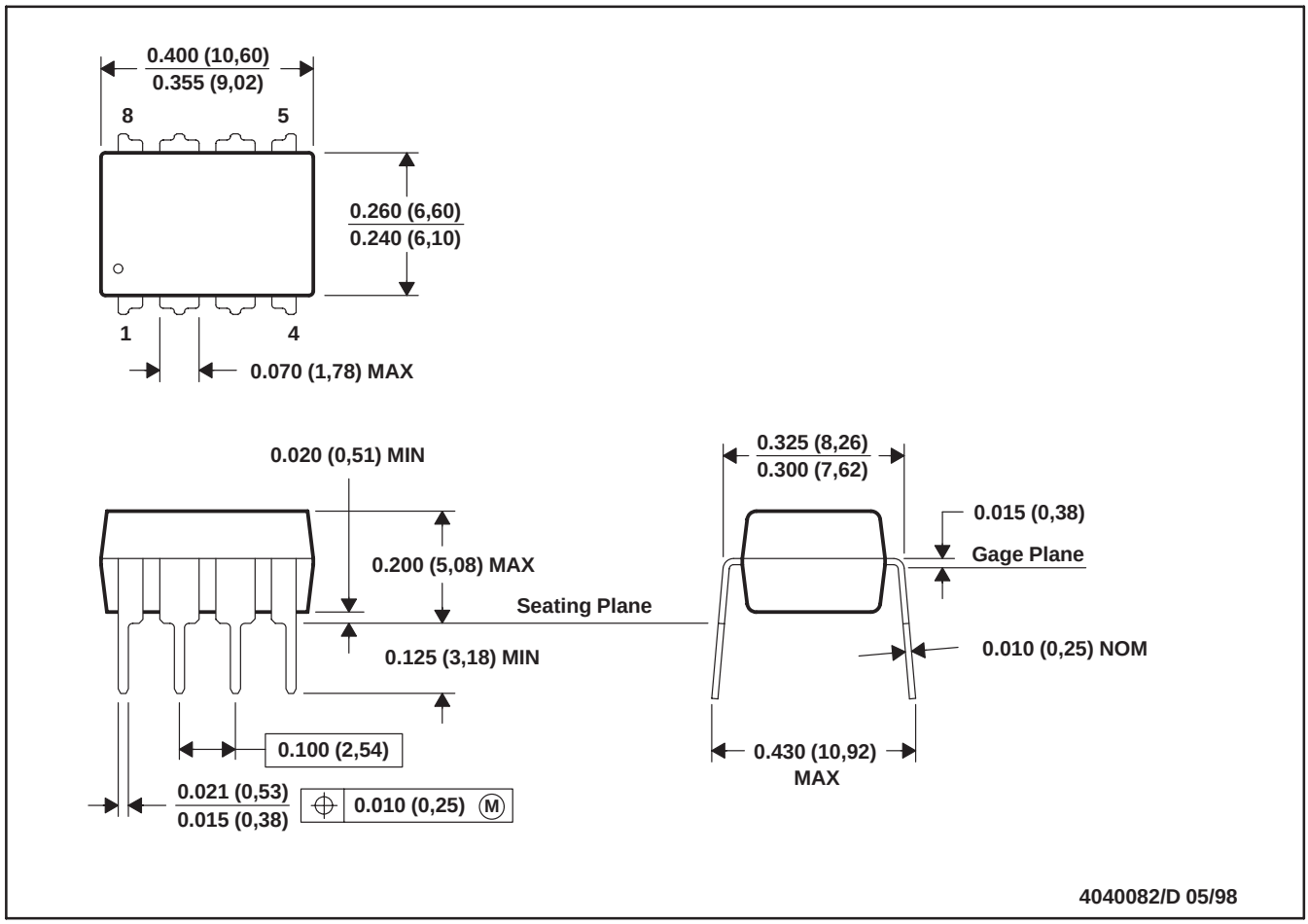


Figure 23. Thermal Resistance

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

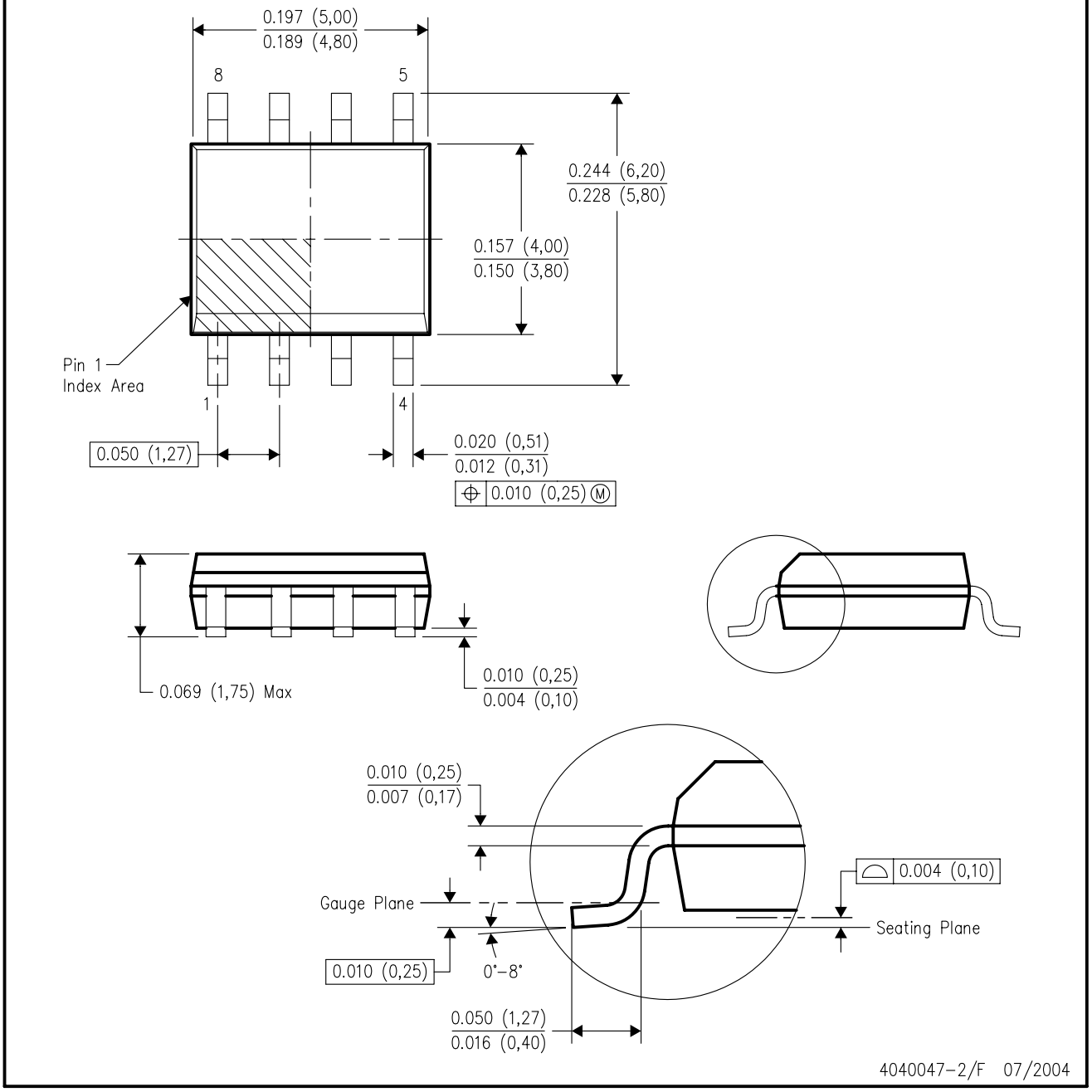
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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