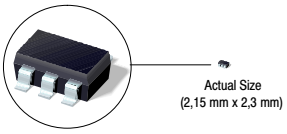


50 mA, 24 V, 3.2µA Supply Current Low-Dropout Linear Regulator in SC70 Package

FEATURES

- **24-V Maximum Input Voltage**
- **Low 3.2-µA Quiescent Current at 50 mA**
- **Stable With Any Capacitor (> 0.47 µF)**
- **50-mA Low-Dropout Regulator**
- **Available in 2.5 V, 3.0 V, 3.3 V, 5.0 V, and Adjustable (12 V to 15 V)**
- **Minimum/Maximum Specified Current Limit**
- **5-Pin SC70/SOT-323 (DCK) Package**
- **-40°C to 125°C Specified Junction Temperature Range**

APPLICATIONS

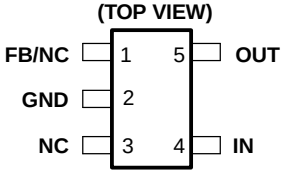
- **Ultra Low Power Microcontrollers**
- **Cellular/Cordless Handsets**
- **Portable/Battery-Powered Equipment**

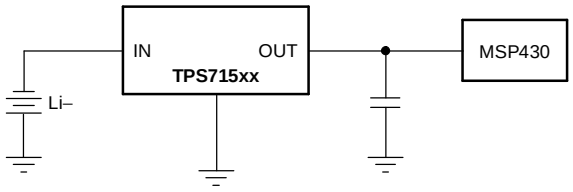
DESCRIPTION

The TPS715xx low-dropout (LDO) voltage regulators offer the benefits of high input voltage, low-dropout voltage, low-power operation, and miniaturized packaging. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any capacitor (> 0.47 µF). The low dropout voltage and low quiescent current allow operations at extremely low power levels. Therefore, the devices are ideal for powering battery management ICs. Specifically, since the devices are enabled as soon as the applied voltage reaches the minimum input voltage, the output is quickly available to power continuously operating battery charging ICs.

The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the low dropout voltage, typically 415 mV at 50 mA of load current, is directly proportional to the load current. The low quiescent current (3.2 µA typically) is stable over the entire range of output load current (0 mA to 50 mA).

DCK PACKAGE
(TOP VIEW)





AVAILABLE OPTIONS(1)

T_J	VOLTAGE	PACKAGE	PART NUMBER	SYMBOL
-40°C to 125°C	2.5 V	SC70/SOT-323 (DCK)	TPS71525DCKR	AQL
	3.0 V	SC70/SOT-323 (DCK)	TPS71530DCKR	AQM
	3.3 V	SC70/SOT-323 (DCK)	TPS71533DCKR	AQI
	5.0 V	SC70/SOT-323 (DCK)	TPS71550DCKR	T48
	(Adjustable) 1.2 V-15 V	SC70/SOT-323 (DCK)	TPS71501DCKR	ARB

(1) Contact the factory for other voltage options between 1.25 V and 5.85 V.

ABSOLUTE MAXIMUM RATINGS

over operating temperature range (unless otherwise noted)(1)(2)

	UNIT
V_{IN} range	-0.3 V to 24 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Rating Table
Junction temperature range, T_J	-40°C to 150°C
Storage temperature range, T_{stg}	-65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JC}$°C/W	$R_{\theta JA}$°C/W	DERATING FACTOR ABOVE T_A = 25°C	$T_A \leq 25$°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low-K(1)	DCK	165	395	2.52 mW/°C	250 mW	140 mW	100 mW
High-K(2)	DCK	165	315	3.18 mW/°C	320 mW	175 mW	130 mW

(1) The JEDEC Low-K (1s) board design used to derive this data was a 3 inch x 3 inch, two-layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

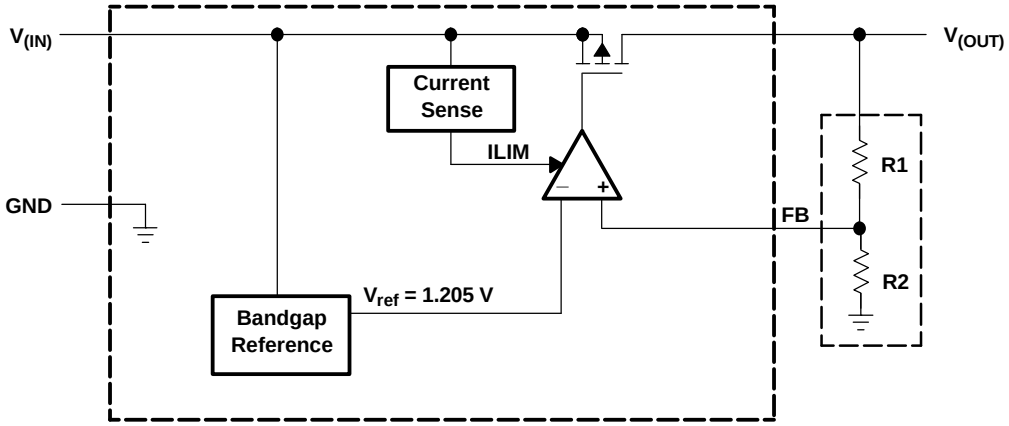
ELECTRICAL CHARACTERISTICS

over operating junction temperature range (T_J = -40°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 1 µF unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage(1)		V_{IN}	I_O = 10 mA	2.5		24	V
			I_O = 50 mA	3		24	
V_{OUT} voltage range (TPS71501)				1.2		15	V
V_{OUT} accuracy(1)	Over V_{IN}, I_{OUT}, and T		V_{IN} + 1.0 V ≤ V_{IN} ≤ 24 V 100 µA ≤ I_{OUT} ≤ 50 mA	-4.0		+4.0	%
Ground pin current		I_{GND}	0 ≤ I_{OUT} ≤ 50 mA, T_J = -40°C to +85°C		3.2	4.2	µA
			0 mA ≤ I_{OUT} ≤ 50 mA		3.2	4.8	
			0 mA ≤ I_{OUT} ≤ 50 mA, V_{IN} = 24 V			5.8	
Load regulation	$\Delta V_{OUT}/\Delta I_{OUT}$		I_{OUT} = 100 µA to 50 mA		22		mV
Output voltage line regulation (1)	$\Delta V_{OUT}/\Delta V_{IN}$		V_{OUT} + 1 V < V_{IN} ≤ 24 V		20	60	mV
Output noise voltage		V_n	BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		575		µVrms
Output current limit		I_{CL}	V_O = 0 V	125		750	mA
Power-supply ripple rejection		PSRR	f = 100 kHz, C_{OUT} = 10 µF		60		dB
Dropout voltage V_{IN} = $V_{OUT(NOM)}$ - 1 V		V_{DO}	I_{OUT} = 50 mA		415	750	mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or the value shown for *Input voltage* in this table, whichever is greater.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION

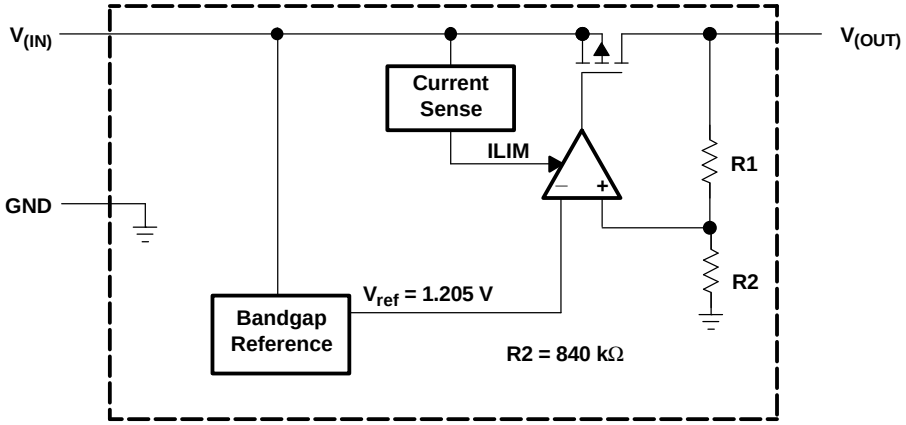


Table 1. Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.		
	FIXED	ADJ.	
FB		1	Adjustable version. This terminal is used to set the output voltage.
NC	1		No connection
GND	2	2	Ground
NC	3	3	No connection
IN	4	4	Unregulated input supply.
OUT	5	5	Output of the regulator, any output capacitor ≥ 0.47 µF can be used for stability.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs OUTPUT CURRENT

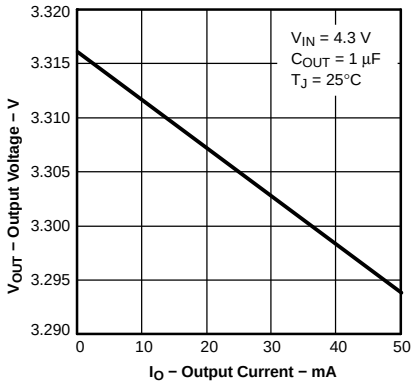


Figure 1.

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

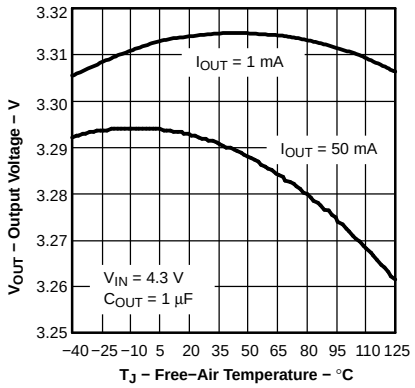


Figure 2.

QUIESCENT CURRENT vs FREE-AIR TEMPERATURE

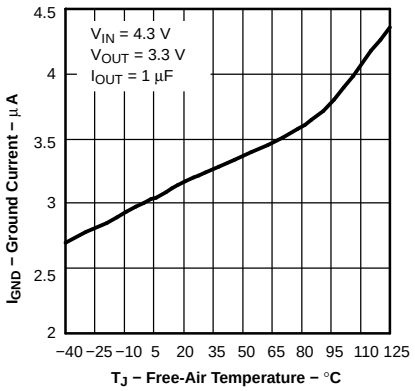


Figure 3.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

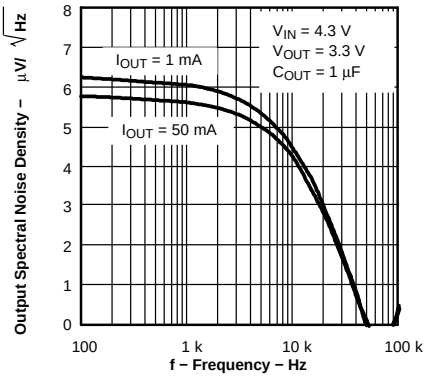


Figure 4.

OUTPUT IMPEDANCE vs FREQUENCY

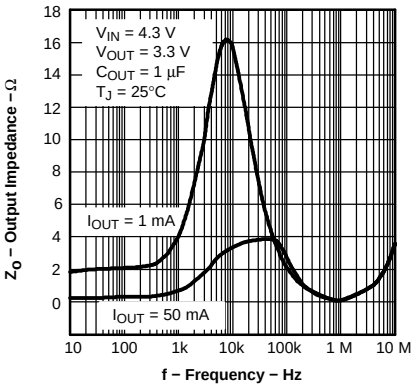


Figure 5.

DROPOUT VOLTAGE vs OUTPUT CURRENT

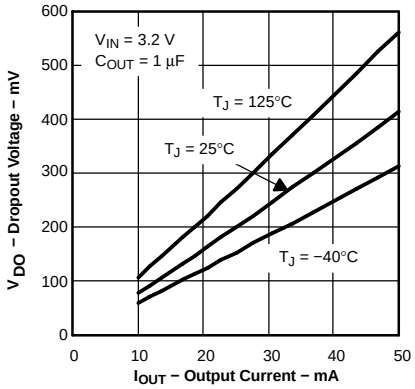


Figure 6.

TPS71501 DROPOUT VOLTAGE vs INPUT VOLTAGE

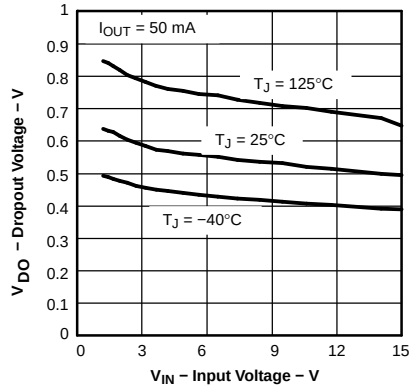


Figure 7.

DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

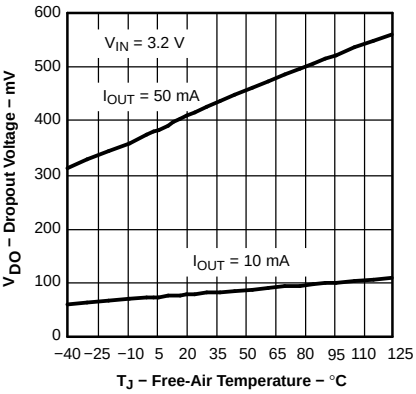


Figure 8.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

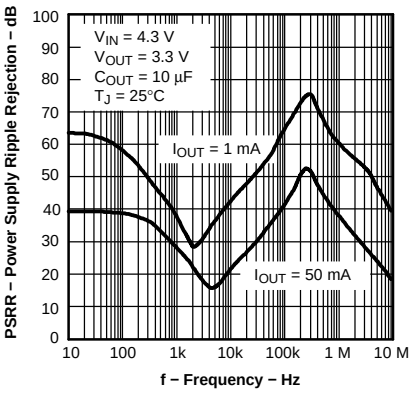


Figure 9.

TYPICAL CHARACTERISTICS (continued)

POWER UP / POWER DOWN

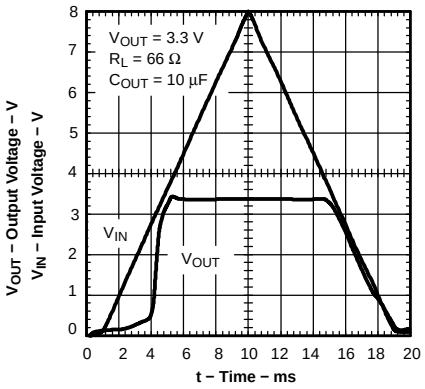


Figure 10.

LINE TRANSIENT RESPONSE

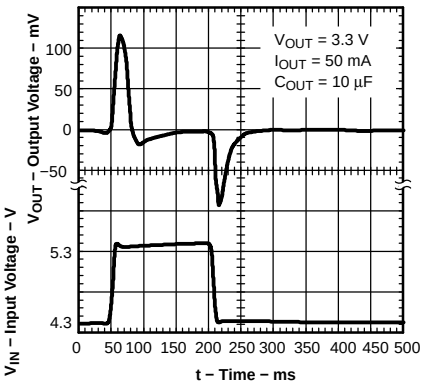


Figure 11.

LOAD TRANSIENT RESPONSE

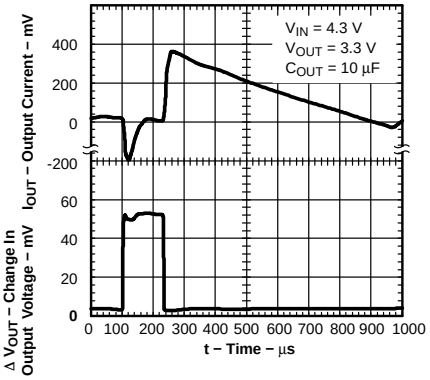


Figure 12.

APPLICATION INFORMATION

The TPS715xx family of LDO regulators has been optimized for ultra-low power applications such as the MSP430 microcontroller. Its ultralow supply current maximizes efficiency at light loads, and its high input voltage range makes it suitable for supplies such as unconditioned solar panels.

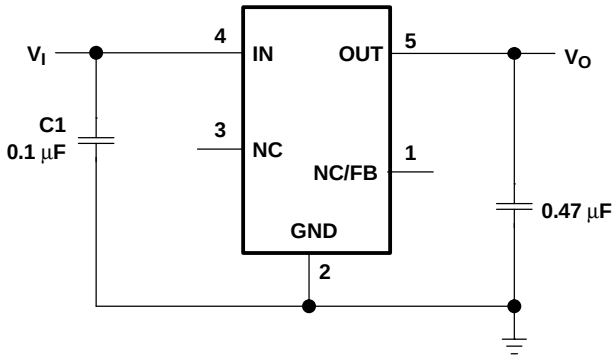


Figure 13. Typical Application Circuit (Fixed Voltage Version)

External Capacitor Requirements

Although not required, a 0.047-μF or larger input bypass capacitor, connected between IN and GND and located close to the device, is recommended to improve transient response and noise rejection of the power supply as a whole. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

The TPS715xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. Any capacitor (including ceramic and tantalum) ≥ 0.47 μF properly stabilizes this loop.

Power Dissipation and Junction Temperature

To ensure reliable operation, worst-case junction temperature should not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the Dissipation Ratings table).
- T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible.

Regulator Protection

The TPS715xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

APPLICATION INFORMATION (continued)

The TPS715xx features internal current limiting. During normal operation, the TPS715xx limits output current to approximately 500 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the power dissipation ratings of the package.

Programming the TPS71501 Adjustable LDO Regulator

The output voltage of the TPS71501 adjustable regulator is programmed using an external resistor divider as shown in Figure 14. The output voltage is calculated using:

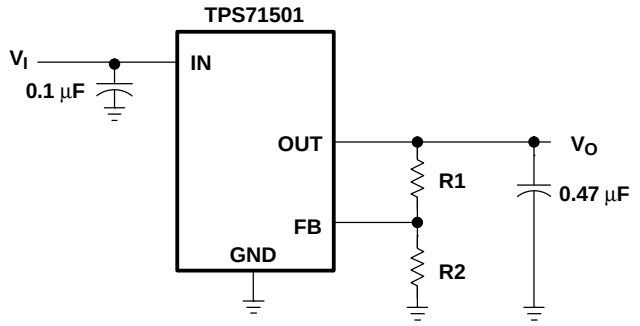
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

where:

- V_{REF} = 1.205 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 1.5-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_O. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (4)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2
1.8 V	0.499 MΩ	1 MΩ
2.8 V	1.33 MΩ	1 MΩ
5.0 V	3.16 MΩ	1 MΩ

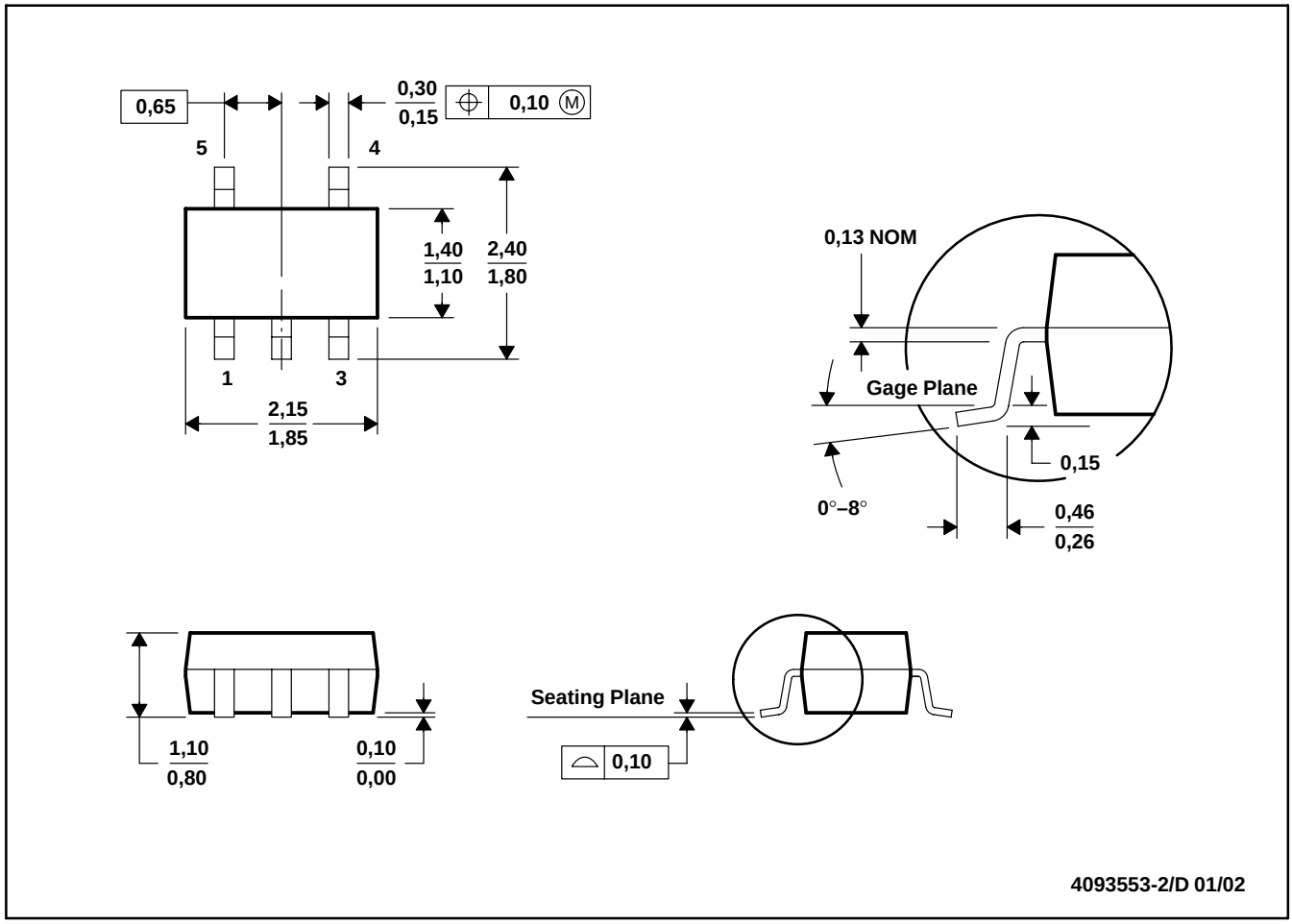
Figure 14. TPS71501 Adjustable LDO Regulator Programming

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
BQ71525DCKR	ACTIVE	SOP	DCK	5	3000
BQ71533DCKR	ACTIVE	SOP	DCK	5	3000
TPS71501DCKR	ACTIVE	SOP	DCK	5	3000
TPS71525DCKR	ACTIVE	SOP	DCK	5	3000
TPS71530DCKR	ACTIVE	SOP	DCK	5	3000
TPS71533DCKR	ACTIVE	SOP	DCK	5	3000
TPS71550DCKR	ACTIVE	SOP	DCK	5	3000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

DCK (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-203

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