

N-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY

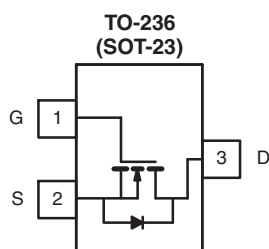
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.060 at $V_{GS} = 4.5$ V	2.4
	0.115 at $V_{GS} = 2.5$ V	2.0

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available



Top View

Si2302ADS (2A)*

* Marking Code

Ordering Information: Si2302ADS-T1-E3 (Lead (Pb)-free)
Si2302ADS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter		Symbol	5 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	20		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	2.4	2.1	A
	T _A = 70 °C		1.9	1.7	
Pulsed Drain Current ^a		I _{DM}	10		
Continuous Source Current (Diode Conduction) ^a		I _S	0.94	0.6	
Power Dissipation ^a	T _A = 25 °C	P _D	0.9	0.7	W
	T _A = 70 °C		0.57	0.46	
Operating Junction and Storage Temperature Range		T _J , T _{sta}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	115	140	°C/W
		140	175	

Notes:

a. Surface mounted on FR4 board.

For SPICE model information via the Worldwide Web: www.vishay.com/www/product/spice.htm

SPECIFICATIONS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = 10\text{ }\mu\text{A}$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	0.65	0.95	1.2	
Gate Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$			0.1	μA
		$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^{\circ}\text{C}$			2.0	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 4.5\text{ V}$	6			A
		$V_{DS} \geq 5\text{ V}$, $V_{GS} = 2.5\text{ V}$	4			
Drain-Source On-Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}$, $I_D = 3.6\text{ A}$		0.045	0.060 ^b	Ω
		$V_{GS} = 2.5\text{ V}$, $I_D = 3.1\text{ A}$		0.070	0.115	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 5\text{ V}$, $I_D = 3.6\text{ A}$		8		S
Diode Forward Voltage	V_{SD}	$I_S = 0.94\text{ A}$, $V_{GS} = 0\text{ V}$		0.76	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 3.6\text{ A}$		4.0	10	nC
Gate-Source Charge	Q_{gs}			0.65		
Gate-Drain Charge	Q_{gd}			1.5		
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		300		pF
Output Capacitance	C_{oss}			120		
Reverse Transfer Capacitance	C_{rss}			80		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.5	1	2	Ω
Switching						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}$, $R_L = 2.8\text{ }\Omega$ $I_D \cong 3.6\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 6\text{ }\Omega$		7	15	ns
Rise Time	t_r			55	80	
Turn-Off Delay Time	$t_{d(off)}$			16	60	
Fall Time	t_f			10	25	

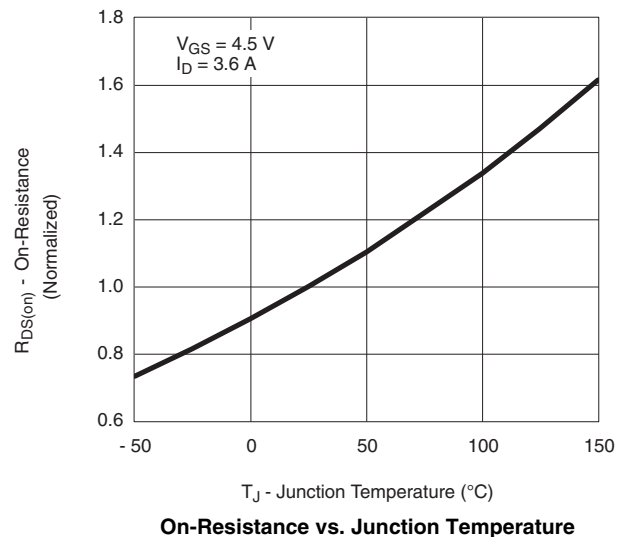
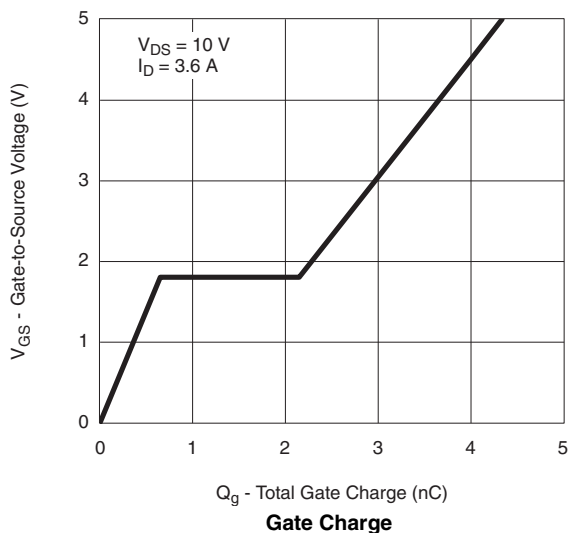
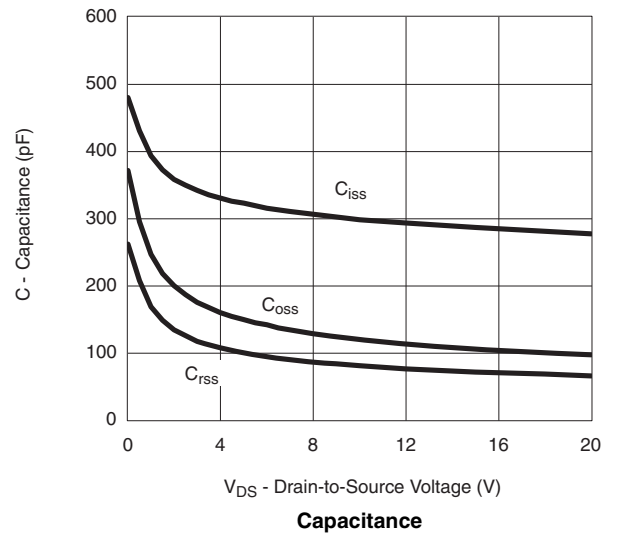
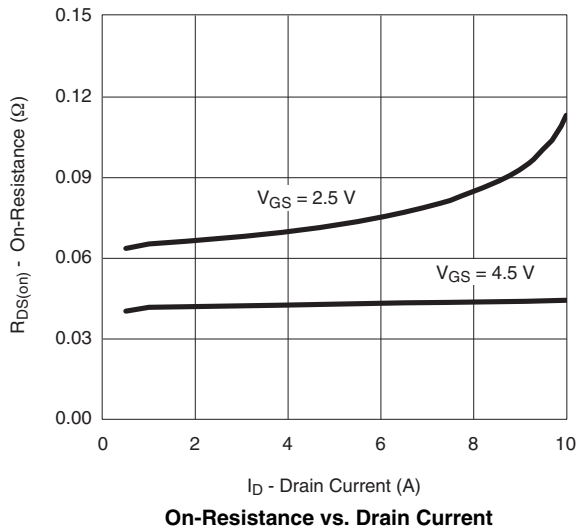
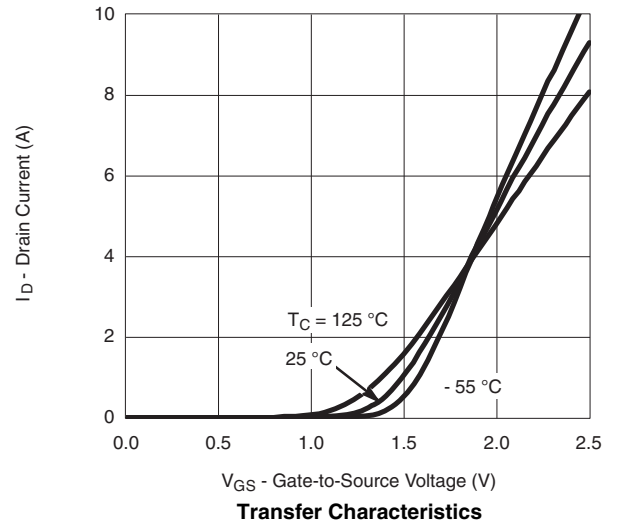
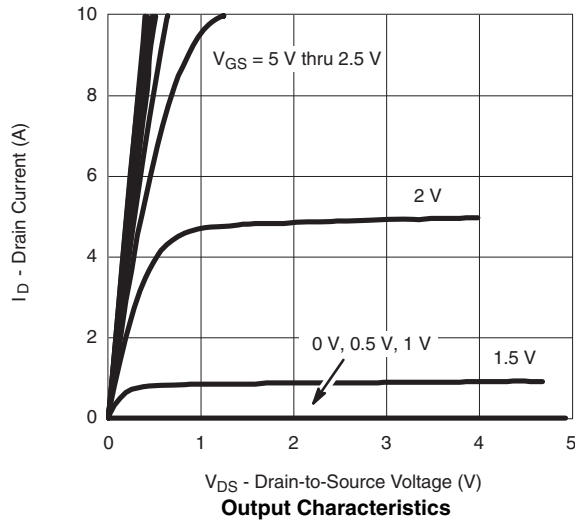
Notes:

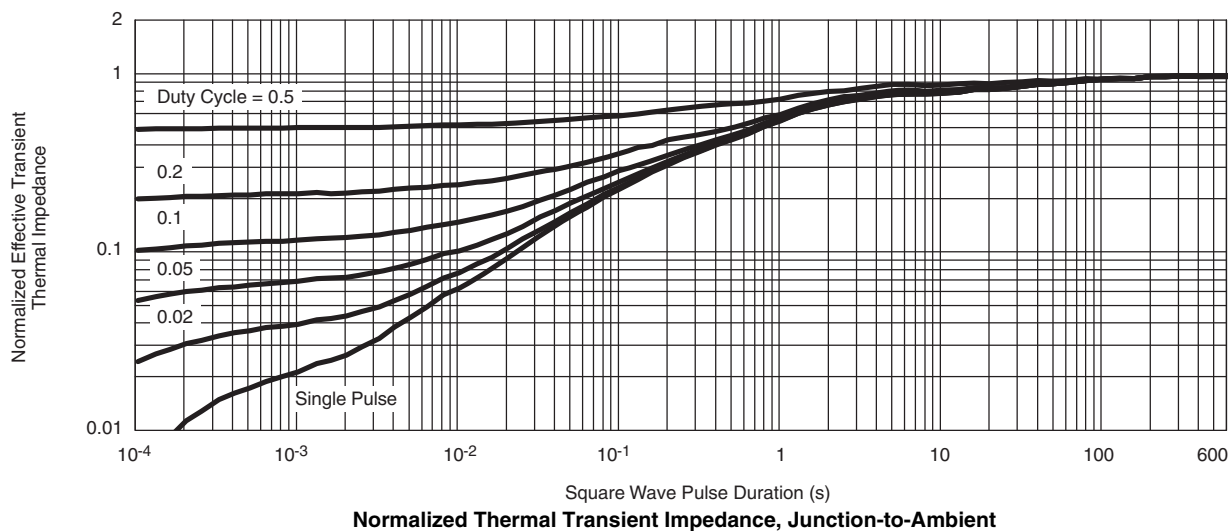
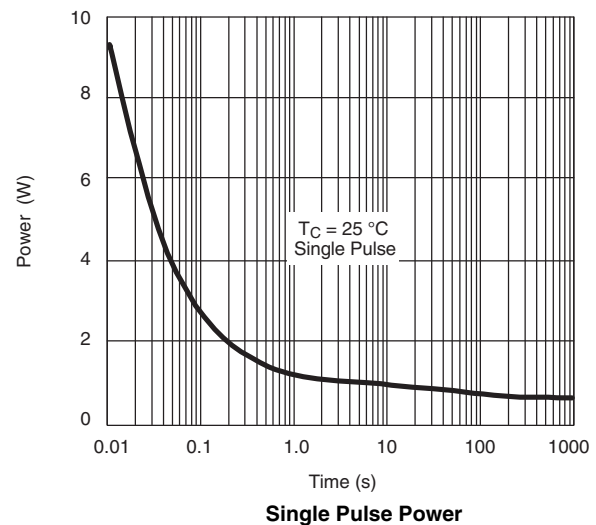
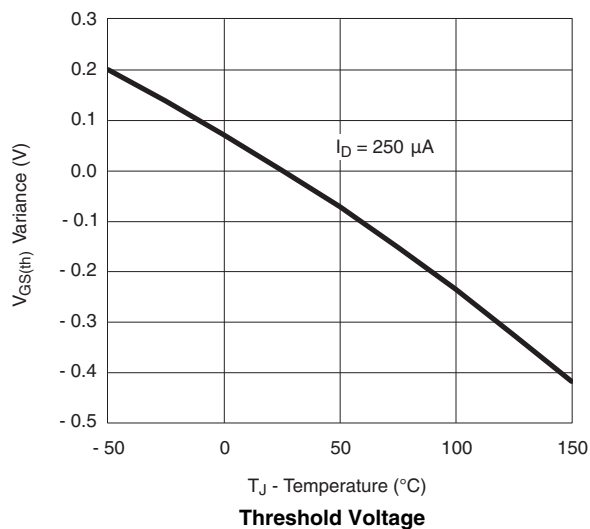
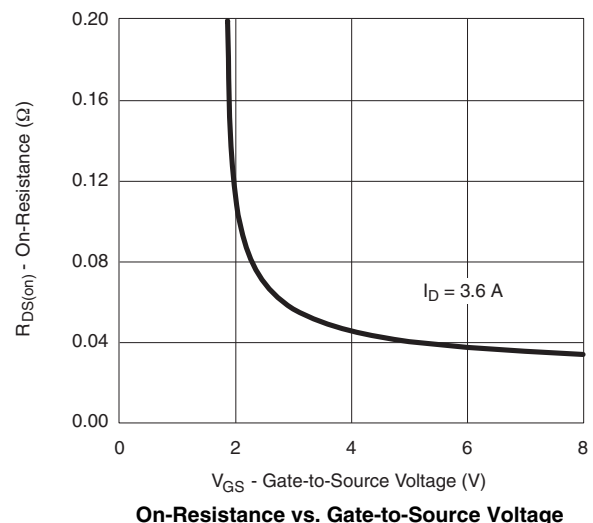
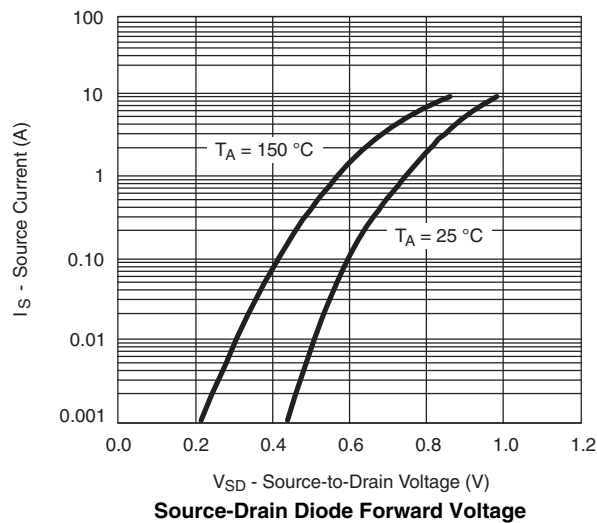
a. Pulse test; $PW \leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Effective for production 10/04.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



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Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71831.

SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A ₁	0.01	0.10	0.0004	0.004
A ₂	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E ₁	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e ₁	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L ₁	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°
ECN: S-03946-Rev. K, 09-Jul-01				
DWG: 5479				

Mounting LITTLE FOOT® SOT-23 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint. In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the

ambient air. This pattern uses all the available area underneath the body for this purpose.



FIGURE 1. Footprint With Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads
Dimensions in Inches/(mm)

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